16K × 8 Dual-Port Static RAM

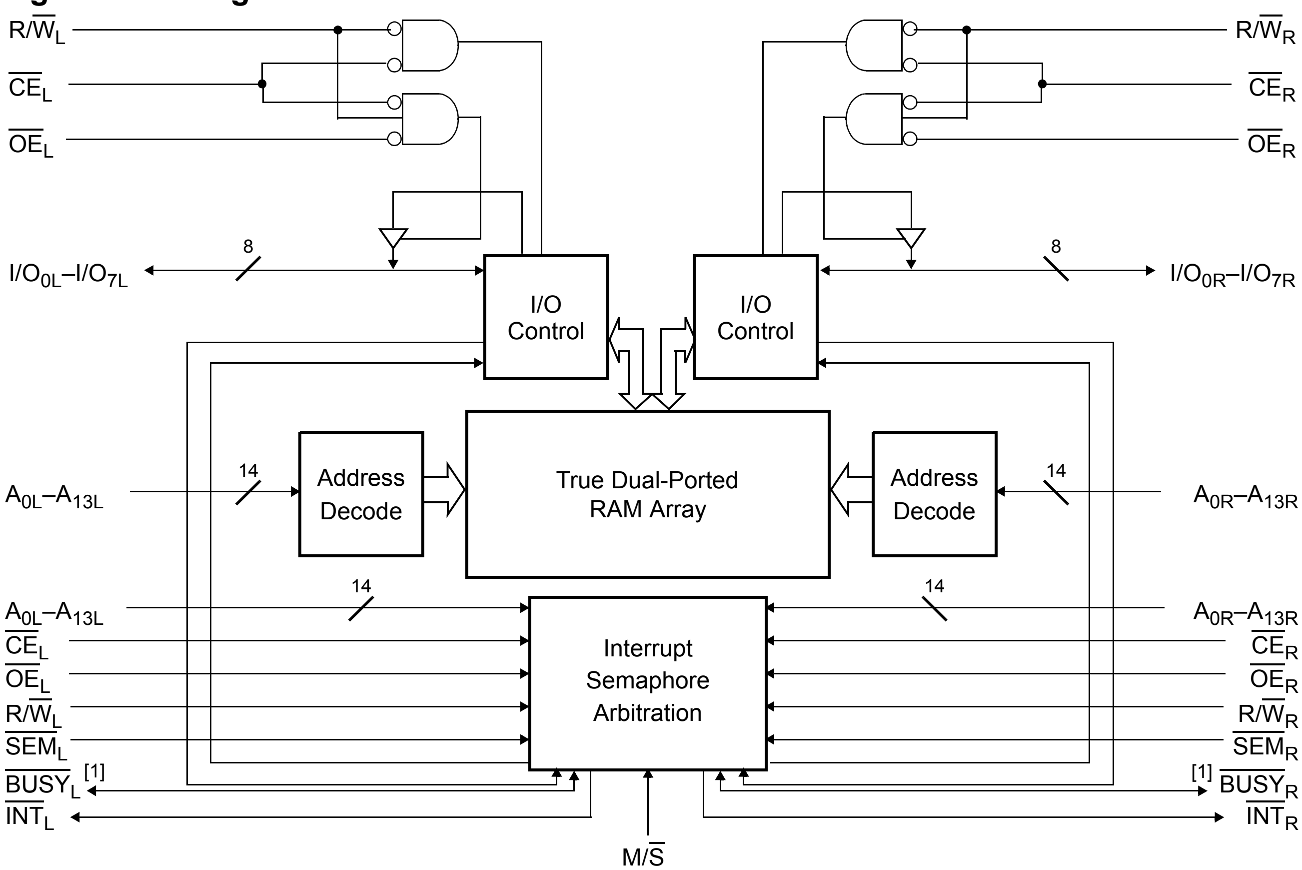
Features

- True dual-ported memory cells which allow simultaneous access of the same memory location
- 16K × 8 organization (CY7C006A)
- 0.35-micron CMOS for optimum speed/power
- High-speed access: 20 ns
- Low operating power
  - Active: I_{CC} = 180 mA (typical)
  - Standby: I_{SB3} = 0.05 mA (typical)
- Fully asynchronous operation
- Automatic power-down
- Expandable data bus to 16 bits or more using Master/Slave chip select when using more than one device
- On-chip arbitration logic
- Semaphores included to permit software handshaking between ports
- $\overline{INT}$ flags for port-to-port communication
- Pin select for Master or Slave
- Commercial temperature range
- Available in 68-pin PLCC (CY7C006A), 64-pin TQFP (CY7C006A)
- Pb-free packages available

Functional Description

For a complete list of related documentation, click here.

Logic Block Diagram



Note
1. $\overline{BUSY}$ is an output in master mode and an input in slave mode.

Contents

Pin Configurations

Figure 1. 68-pin PLCC pinout
Top View

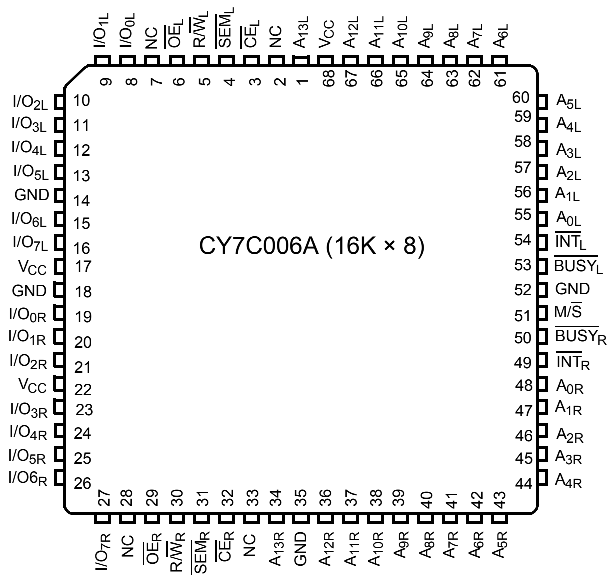
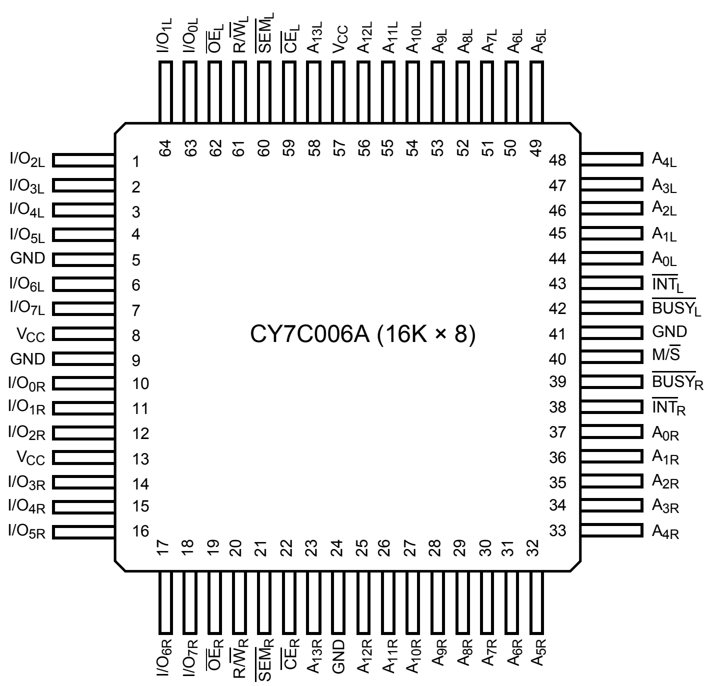


Figure 2. 64-pin TQFP pinout
Top View



Selection Guide

Description	CY7C006A -20	Unit
Maximum Access Time	20	ns
Typical Operating Current	180	mA
Typical Standby Current for I_{SB1} (Both Ports TTL Level)	45	mA
Typical Standby Current for I_{SB3} (Both Ports CMOS Level)	0.05	mA

Pin Definitions

Left Port	Right Port	Description
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L}–A_{13L}	A_{0R}–A_{13R}	Address
I/O_{0L}–I/O_{7L}	I/O_{0R}–I/O_{7R}	Data Bus Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground
NC		No Connect

Architecture

The CY7C006A consists of an array 16K words of 8 bits of dual-port RAM cells, I/O and address lines, and control signals (CE, OE, R/W). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a BUSY pin is provided on each port. Two Interrupt (INT) pins can be utilized for port-to-port communication. Two Semaphore (SEM) control pins are used for allocating shared resources. With the M/S pin, the devices can function as a master (BUSY pins are outputs) or as a slave (BUSY pins are inputs). The devices also have an automatic power-down feature controlled by CE. Each port is provided with its own Output Enable control (OE), which allows data to be read from the device.

Functional Overview

The CY7C006A is low-power CMOS 16K × 8 dual-port static RAMs. Various arbitration schemes are included on the devices to handle situations when multiple processors access the same piece of data. Two ports are provided, permitting independent, asynchronous access for reads and writes to any location in memory. The devices can be utilized as standalone 8-bit dual-port static RAMs or multiple devices can be combined in order to function as a 16-bit or wider master/slave dual-port static RAM. An M/S pin is provided for implementing 16-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: Chip Enable (CE), Read or Write Enable (R/W), and Output Enable (OE). Two flags are provided on each port (BUSY and INT). BUSY signals that the port is trying to access the same location currently being accessed by the other port. The Interrupt flag (INT) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a Chip Select (CE) pin.

The CY7C006A is available in 68-pin PLCC package, the CY7C006A is also available in 64-pin TQFP package.

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/W in order to guarantee a valid write. A write operation is controlled by either the R/W pin (see Write Cycle No. 1 waveform) or the CE pin (see Write Cycle No. 2 waveform). Required inputs for non-contention operations are summarized in Non-Contending Read/Write on page 16.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ is asserted. If the user wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin, and $\overline{OE}$ must also be asserted.

Interrupts

The upper two memory locations may be used for message passing. The highest memory location (3FFF) is the mailbox for the right port and the second-highest memory location (3FFE) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and, thus, resetting the interrupt to it.

If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin. The operation of the interrupts and their interaction with Busy are summarized in Interrupt Operation Example on page 16.

Busy

The CY7C006A provides on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other, the busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not predictable which port will get that permission. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW.

Master/Slave

A M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the $\overline{BUSY}$ input has settled (t_{BLC} or t_{BLA}), otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the M/$\overline{S}$ pin allows the device to be used as a master and, therefore, the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C006A provides eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available t_{SWRD} + t_{DOE} after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip select for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). $A_{0–2}$ represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a zero is written to the left port of an available semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. Semaphore Operation Example on page 16 shows sample semaphore operations.

When reading a semaphore, all data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Maximum Ratings

Exceeding maximum ratings [2] may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .... –65 °C to +150 °C

Ambient Temperature with Power Applied .... –55 °C to +125 °C

Supply Voltage to Ground Potential ....–0.3 V to +7.0 V

DC Voltage Applied to Outputs in High Z State ....–0.5 V to +7.0 V

DC Input Voltage [3] ....–0.5 V to +7.0 V

Output Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage .... > 2001V

Latch-Up Current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description		CY7C006A -20 Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (V_{CC} = Min, I_{OH} = –4.0 mA)		2.4	–	–	V
V_{OL}	Output LOW Voltage (V_{CC} = Min, I_{OH} = +4.0 mA)		–		0.4	V
V_{IH}	Input HIGH Voltage		2.2		–	V
V_{IL}	Input LOW Voltage		–		0.8	V
I_{OZ}	Output Leakage Current		–10		10	µA
I_{CC}	Operating Current (V_{CC} = Max, I_{OUT} = 0 mA), Outputs Disabled	Commercial	–	180	275	mA
		Industrial		–		mA
I_{SB1}	Standby Current (Both Ports TTL Level), $\overline{CE}_L$ & $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Commercial		45	65	mA
		Industrial		–		mA
I_{SB2}	Standby Current (One Port TTL Level), $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Commercial		110	160	mA
		Industrial		–		mA
I_{SB3}	Standby Current (Both Ports CMOS Level), $\overline{CE}_L$ & $\overline{CE}_R \geq V_{CC} - 0.2$ V, f = 0	Commercial		0.05	0.5	mA
		Industrial		–		mA
I_{SB4}	Standby Current (One Port CMOS Level), $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX} [3, 4]	Commercial		100	140	mA
		Industrial		–		mA

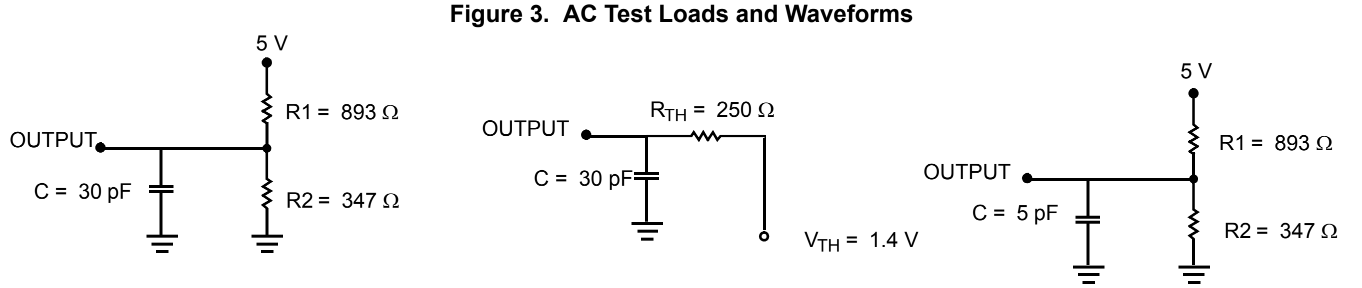
Notes
2. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
3. Pulse width < 20 ns.
4. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

Capacitance

Parameter [5]	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	$T_A = 25\ °C$, f = 1 MHz, $V_{CC} = 5.0\ V$	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



(a) Normal Load (Load 1)

(b) Thévenin Equivalent (Load 1)

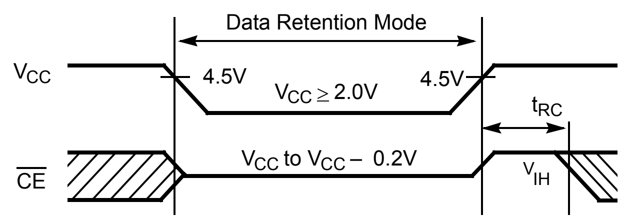
(c) Three-State Delay (Load 2)
(Used for t_{LZ}, t_{HZ}, t_{HZWE}, & t_{LZWE} including scope and jig)

Data Retention Mode

The CY7C006A is designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip Enable ($\overline{CE}$) must be held HIGH during data retention, within V_{CC} to $V_{CC} – 0.2$ V.
2. $\overline{CE}$ must be kept between $V_{CC} – 0.2$ V and 70% of V_{CC} during the power-up and power-down transitions.
3. The RAM can begin operation >t_{RC} after V_{CC} reaches the minimum operating voltage (4.5 V).

Timing



Parameter	Test Conditions [6]	Max	Unit
ICC_{DR1}	@ VCC_{DR} = 2 V	1.5	mA

Notes
5. Tested initially and after any design or process changes that may affect these parameters.
6. $\overline{CE} = V_{CC}$, V_{in} = GND to V_{CC}, T_A = 25°C. This parameter is guaranteed but not tested.

Switching Characteristics

Over the Operating Range

Parameter [7]	Description	CY7C006A		Unit
		-20		
		Min	Max	
READ CYCLE				
t_{RC}	Read Cycle Time	20	–	ns
t_{AA}	Address to Data Valid	–	20	ns
t_{OHA}	Output Hold From Address Change	3	–	ns
t_{ACE}[8]	$\overline{CE}$ LOW to Data Valid	–	20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	12	ns
t_{LZOE}[9, 10, 11]	$\overline{OE}$ LOW to Low Z	3	–	ns
t_{HZOE}[9, 10, 11]	$\overline{OE}$ HIGH to High Z	–	12	ns
t_{LZCE}[9, 10, 11]	$\overline{CE}$ LOW to Low Z	3	–	ns
t_{HZCE}[9, 10, 11]	$\overline{CE}$ HIGH to High Z	–	12	ns
t_{PU}[11]	$\overline{CE}$ LOW to Power-Up	0	–	ns
t_{PD}[11]	$\overline{CE}$ HIGH to Power-Down	–	20	ns
WRITE CYCLE				
t_{WC}	Write Cycle Time	20	–	ns
t_{SCE}[8]	$\overline{CE}$ LOW to Write End	15	–	ns
t_{AW}	Address Valid to Write End	15	–	ns
t_{HA}	Address Hold From Write End	0	–	ns
t_{SA}[8]	Address Set-Up to Write Start	0	–	ns
t_{PWE}	Write Pulse Width	15	–	ns
t_{SD}	Data Set-Up to Write End	15	–	ns
t_{HD}[12]	Data Hold From Write End	0	–	ns
t_{HZWE}[10, 11]	R/$\overline{W}$ LOW to High Z	–	12	ns
t_{LZWE}[10, 11]	R/$\overline{W}$ HIGH to Low Z	3	–	ns
t_{WDD}[13]	Write Pulse to Data Delay	–	45	ns
t_{DDD}[13]	Write Data Valid to Read Data Valid	–	30	ns

Notes

7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OI}/I_{OH} and 30-pF load capacitance.
8. To access RAM, $\overline{CE}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire t_{SCE} time.
9. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
10. Test conditions used are Load 3.
11. This parameter is guaranteed but not tested.
12. For 15 ns industrial parts t_{HD} Min. is 0.5 ns.
13. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.

Switching Characteristics *(continued)*

Over the Operating Range

Parameter [7]	Description	CY7C006A -20 Min	CY7C006A -20 Max	Unit
BUSY TIMING [14]				
t_{BLA}	$\overline{BUSY}$ LOW from Address Match	–	20	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch	–	20	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW	–	20	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH	–	17	ns
t_{PS}	Port Set-Up for Priority	5	–	ns
t_{WB}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ (Slave)	0	–	ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave)	15	–	ns
t_{BDD}[15]	$\overline{BUSY}$ HIGH to Data Valid	–	20	ns
INTERRUPT TIMING [14]				
t_{INS}	$\overline{INT}$ Set Time	–	20	ns
t_{INR}	$\overline{INT}$ Reset Time	–	20	ns
SEMAPHORE TIMING				
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	–	ns
t_{SWRD}	SEM Flag Write to Read Time	5	–	ns
t_{SPS}	SEM Flag Contention Window	5	–	ns
t_{SAA}	SEM Address Access Time	–	20	ns

Notes
14. Test conditions used are Load 2.
15. t_{BDD} is a calculated parameter and is the greater of t_{WDD}–t_{PWE} (actual) or t_{DDD}–t_{SD} (actual).

Switching Waveforms

Figure 4. Read Cycle No. 1 (Either Port Address Access) [16, 17, 18]

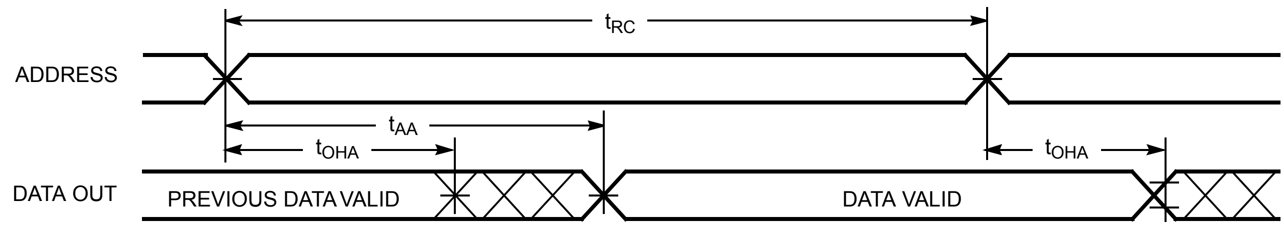


Figure 5. Read Cycle No. 2 (Either Port $\overline{CE}$/$\overline{OE}$ Access) [16, 19, 20]

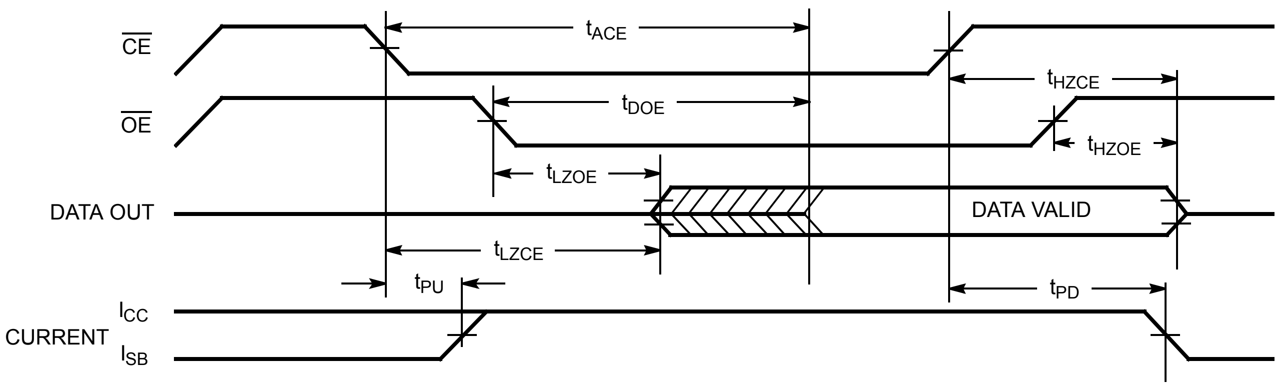
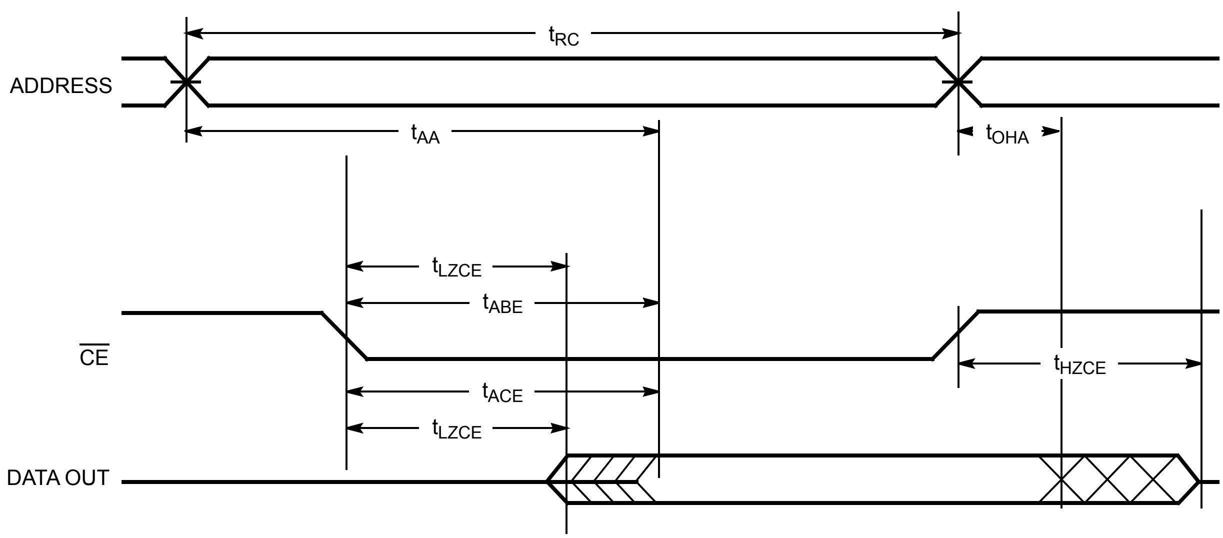


Figure 6. Read Cycle No. 3 (Either Port) [16, 18, 19, 20]



Notes

16. R/$\overline{W}$ is HIGH for read cycles.
17. Device is continuously selected $\overline{CE}$ = V_{IL}. This waveform cannot be used for semaphore reads.
18. $\overline{OE}$ = V_{IL}.
19. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
20. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH}, $\overline{SEM}$ = V_{IL}.

Switching Waveforms *(continued)*

Figure 7. Write Cycle No. 1 (R/W Controlled Timing) [21, 22, 23, 24]

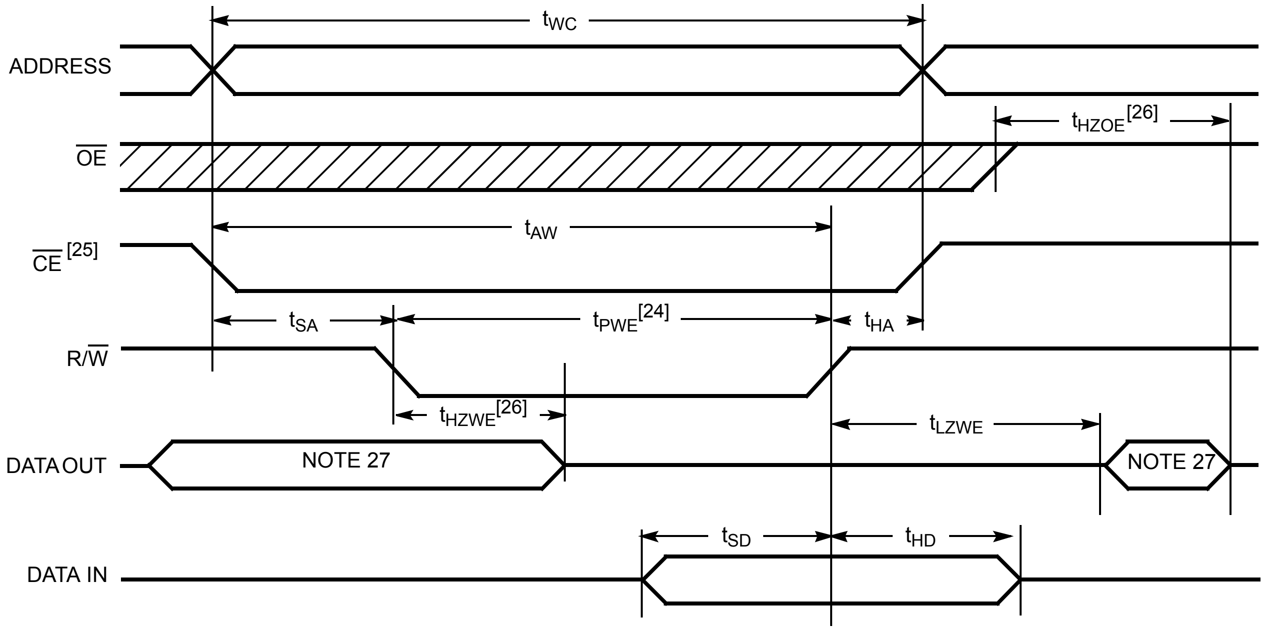
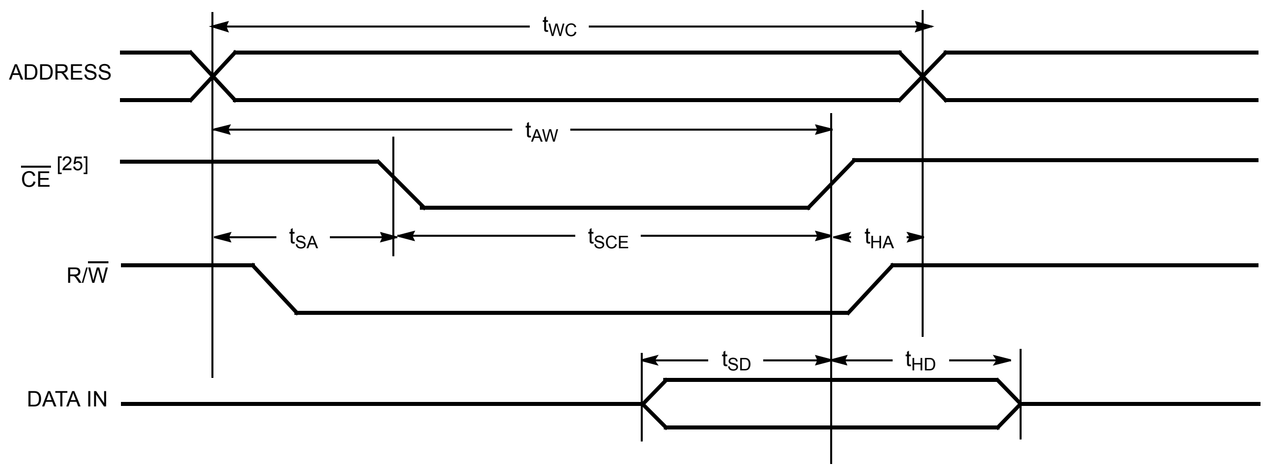


Figure 8. Write Cycle No. 2 (CE Controlled Timing) [21, 22, 23, 28]



Notes

21. R/W or CE must be HIGH during all address transitions.
22. A write occurs during the overlap (t_{SCE} or t_{PWE}) of a LOW CE or SEM.
23. t_{HA} is measured from the earlier of CE or R/W or (SEM or R/W) going HIGH at the end of write cycle.
24. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If OE is HIGH during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
25. To access RAM, CE = V_{IL}, SEM = V_{IH}.
26. Transition is measured ±500 mV from steady state with a 5-pF load (including scope and jig). This parameter is sampled and not 100% tested.
27. During this period, the I/O pins are in the output state, and input signals must not be applied.
28. If the CE or SEM LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the high-impedance state.

Switching Waveforms *(continued)*

Figure 9. Semaphore Read After Write Timing, Either Side [29]

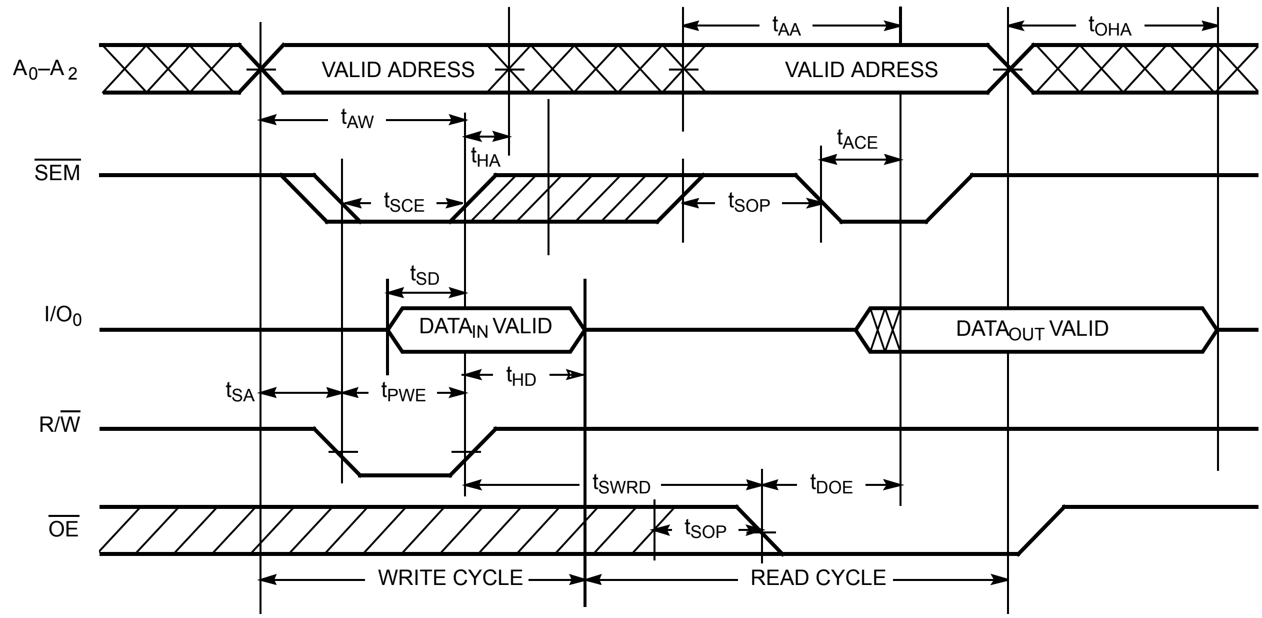
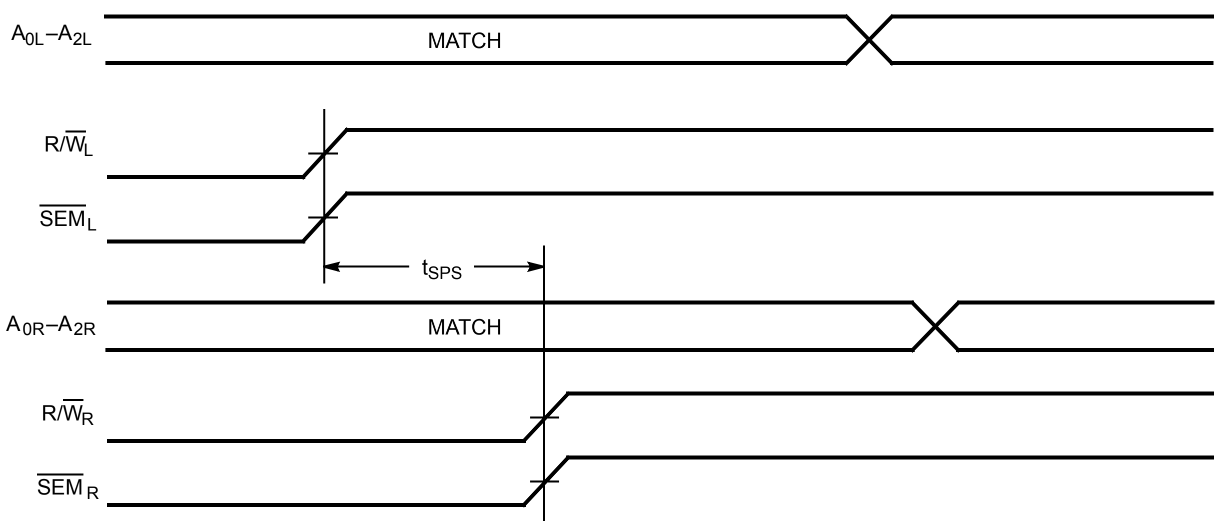


Figure 10. Timing Diagram of Semaphore Contention [30, 31, 32]



Notes
29. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
30. I/O_{0R} = I/O_{0L} = LOW (request semaphore); $\overline{CE}_R$ = $\overline{CE}_L$ = HIGH.
31. Semaphores are reset (available to both ports) at cycle start.
32. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but which side will get the semaphore is unpredictable.

Switching Waveforms *(continued)*

Figure 11. Timing Diagram of Read with BUSY (M/S = HIGH) [33]

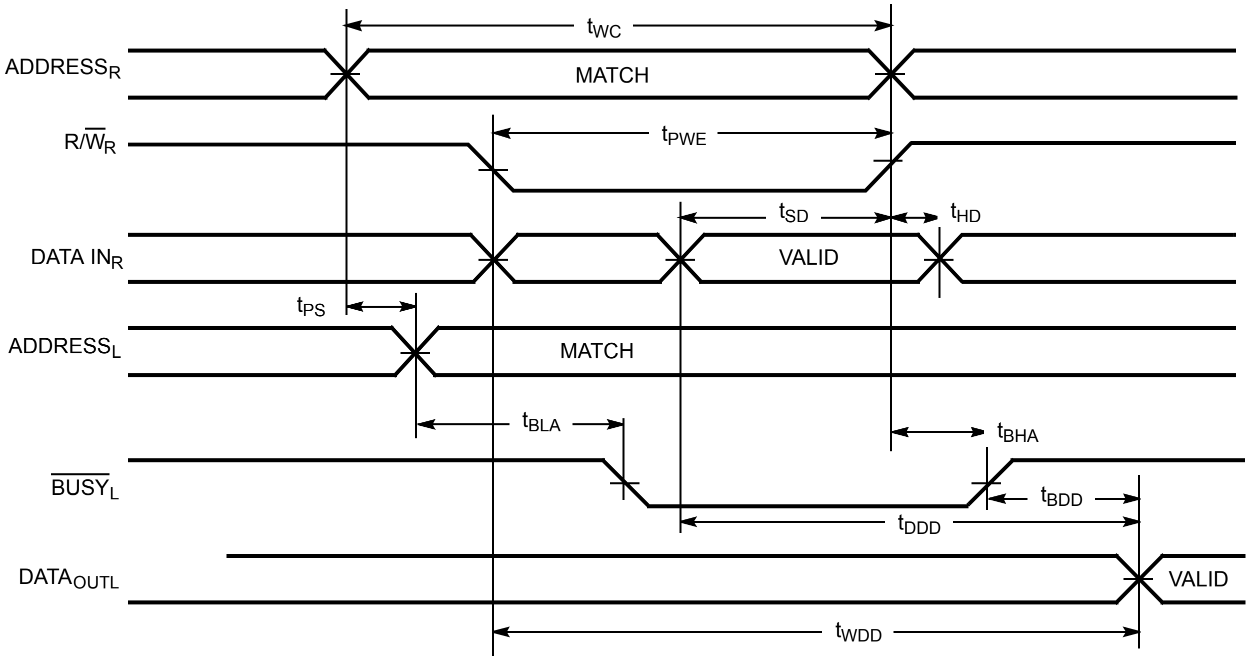
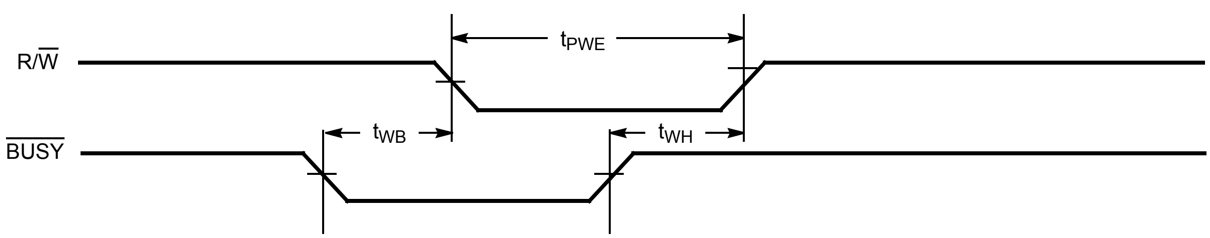


Figure 12. Write Timing with Busy Input (M/S = LOW)



Note

33. $\overline{CE}_L = \overline{CE}_R$ = LOW.

Switching Waveforms *(continued)*

Figure 13. Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration) [34]

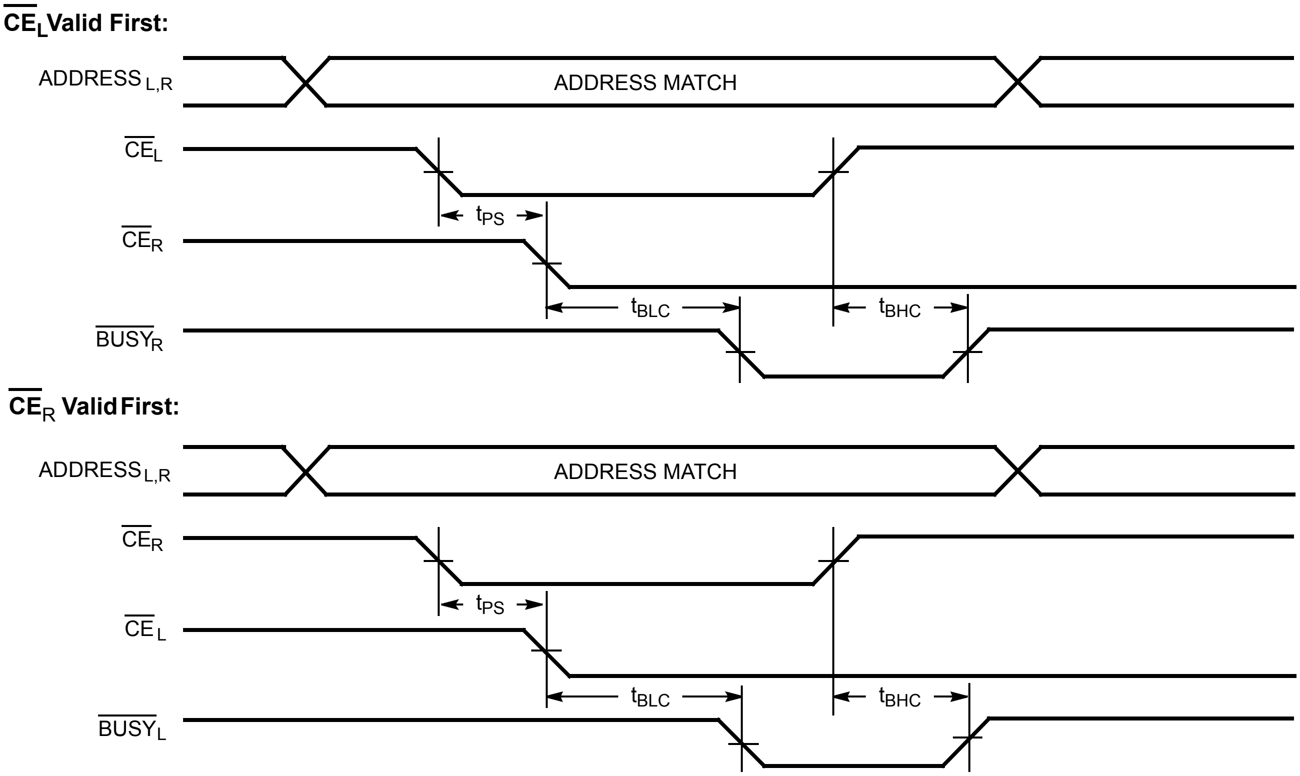
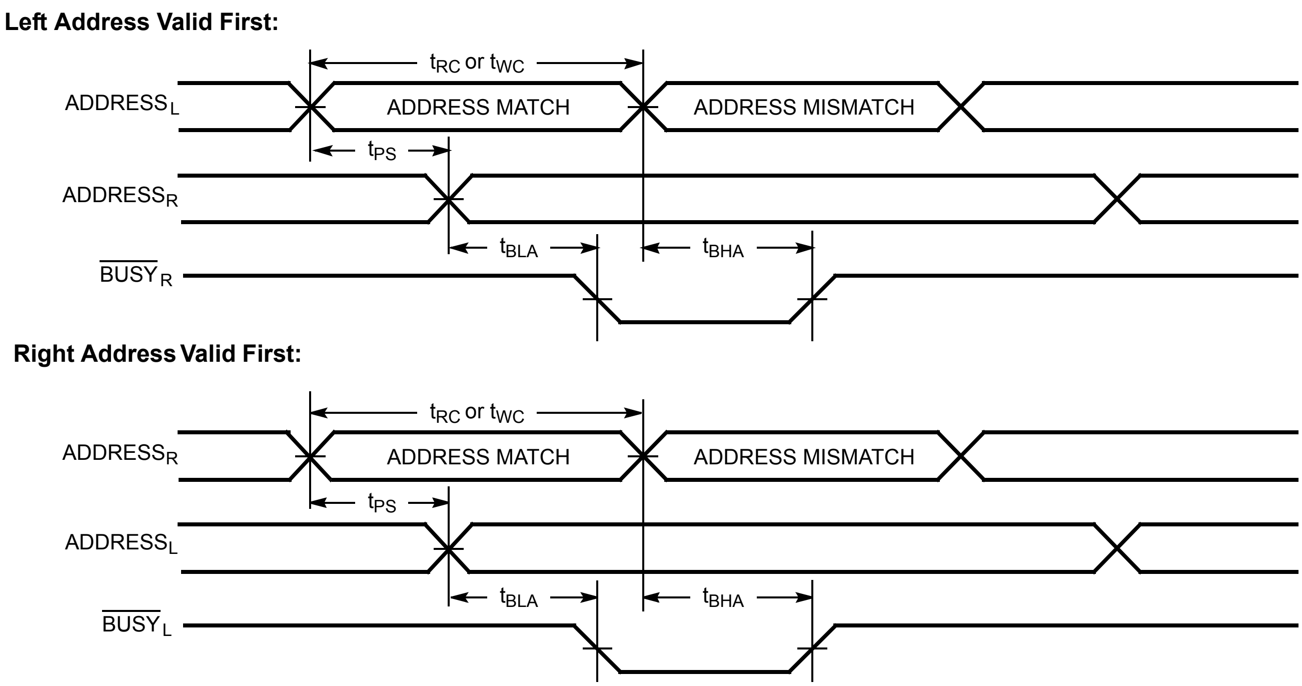


Figure 14. Busy Timing Diagram No. 2 (Address Arbitration) [34]

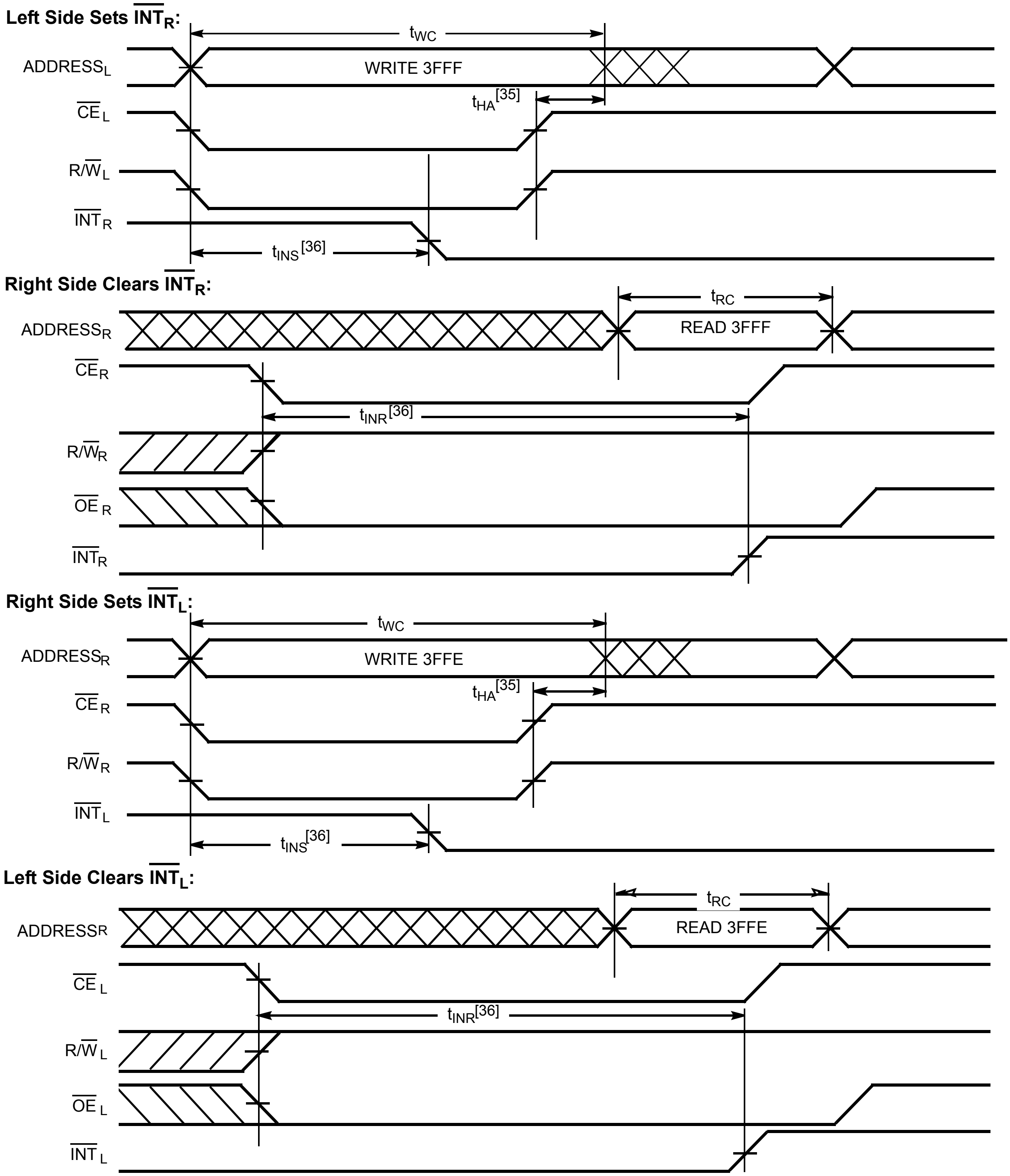


Note

34. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee to which side $\overline{BUSY}$ will be asserted.

Switching Waveforms *(continued)*

Figure 15. Interrupt Timing Diagrams



Notes

35. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
36. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

Non-Contending Read/Write

Inputs				Outputs	
$\overline{\text{CE}}$	R/$\overline{\text{W}}$	$\overline{\text{OE}}$	$\overline{\text{SEM}}$	I/O_0–I/O_8	Operation
H	X	X	H	High Z	Deselected: Power-Down
H	H	L	L	Data Out	Read Data in Semaphore Flag
X	X	H	X	High Z	I/O Lines Disabled
H	_/‾	X	L	Data In	Write into Semaphore Flag
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Not Allowed

Interrupt Operation Example

(Assumes $\overline{\text{BUSY}}_L$ = $\overline{\text{BUSY}}_R$ = HIGH)

	Left Port					Right Port				
Function	R/$\overline{\text{W}}_L$	$\overline{\text{CE}}_L$	$\overline{\text{OE}}_L$	$A_{0L–14L}$	$\overline{\text{INT}}_L$	R/$\overline{\text{W}}_R$	$\overline{\text{CE}}_R$	$\overline{\text{OE}}_R$	$A_{0R–14R}$	$\overline{\text{INT}}_R$
Set Right $\overline{\text{INT}}_R$ Flag	L	L	X	3FFF	X	X	X	X	X	L[37]
Reset Right $\overline{\text{INT}}_R$ Flag	X	X	X	X	X	X	L	L	3FFF	H[38]
Set Left $\overline{\text{INT}}_L$ Flag	X	X	X	X	L[38]	L	L	X	3FFE	X
Reset Left $\overline{\text{INT}}_L$ Flag	X	L	L	3FFE	H[37]	X	X	X	X	X

Semaphore Operation Example

Function	I/O_0–I/O_8 Left	I/O_0–I/O_8 Right	Status
No action	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left Port has semaphore token
Right port writes 0 to semaphore	0	1	No change. Right side has no write access to semaphore
Left port writes 1 to semaphore	1	0	Right port obtains semaphore token
Left port writes 0 to semaphore	1	0	No change. Left port has no write access to semaphore
Right port writes 1 to semaphore	0	1	Left port obtains semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free
Right port writes 0 to semaphore	1	0	Right port has semaphore token
Right port writes 1 to semaphore	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free

Notes

37. If $\overline{\text{BUSY}}_L$ = L, then no change.
38. If BUSY_R = L, then no change.

Ordering Information

16K × 8 Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C006A-20AXC	A65	64-pin TQFP (Pb-free)	Commercial
	CY7C006A-20AXI	A65	64-pin TQFP (Pb-free)	Industrial
	CY7C006A-20JXC	J81	68-pin PLCC (Pb-free)	Commercial

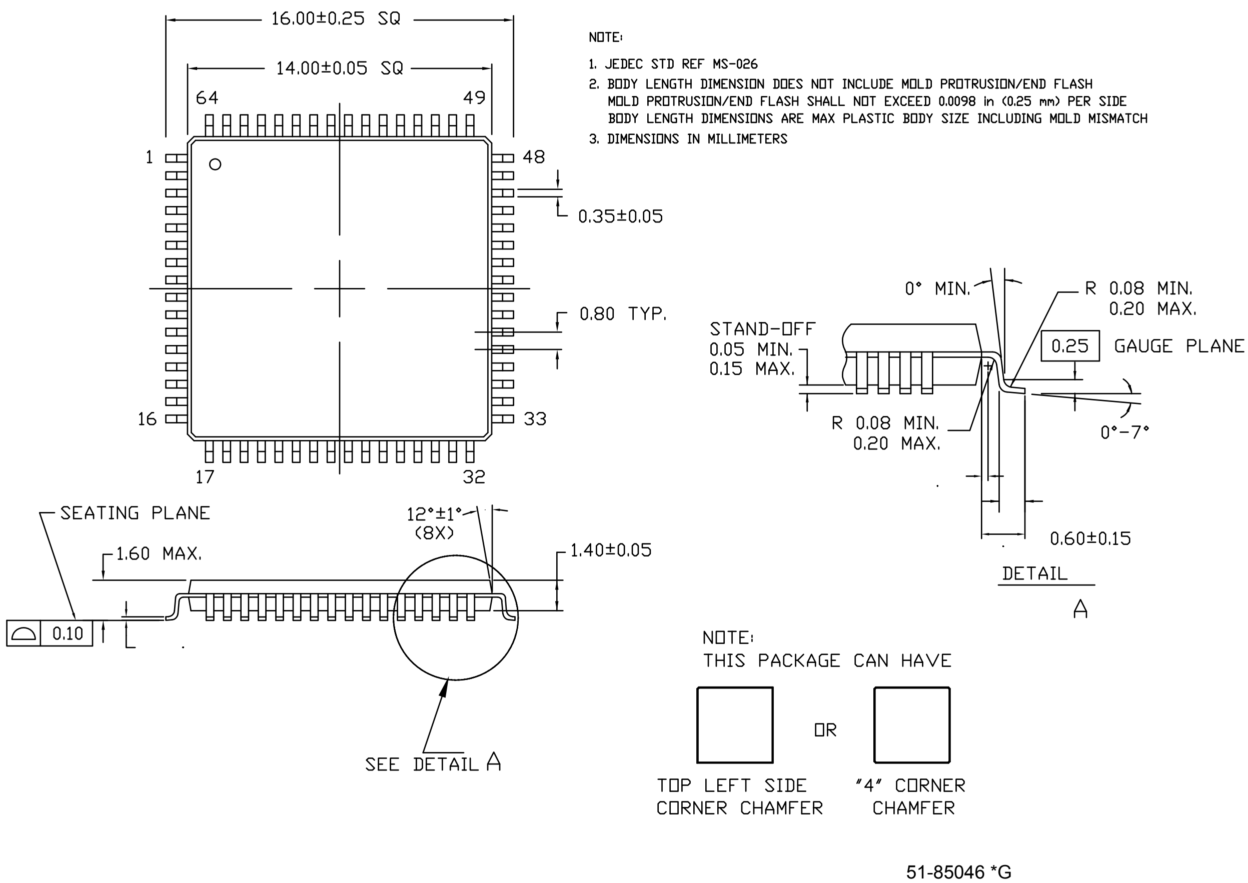
Ordering Code Definitions

CY 7 C 0 06A - 20 X X X

- Temperature Range: X = C or I
  C = Commercial; I = Industrial
- X = Pb-free (RoHS Compliant)
- Package Type: X = A or J
  A = 64-pin TQFP
  J = 68-pin PLCC
- Speed Grade: 20 ns
- Depth: 06A = 16K
- Width: 0 = × 8
- Technology Code: C = CMOS
- Marketing Code: 7 = Dual Port SRAM
- Company ID: CY = Cypress

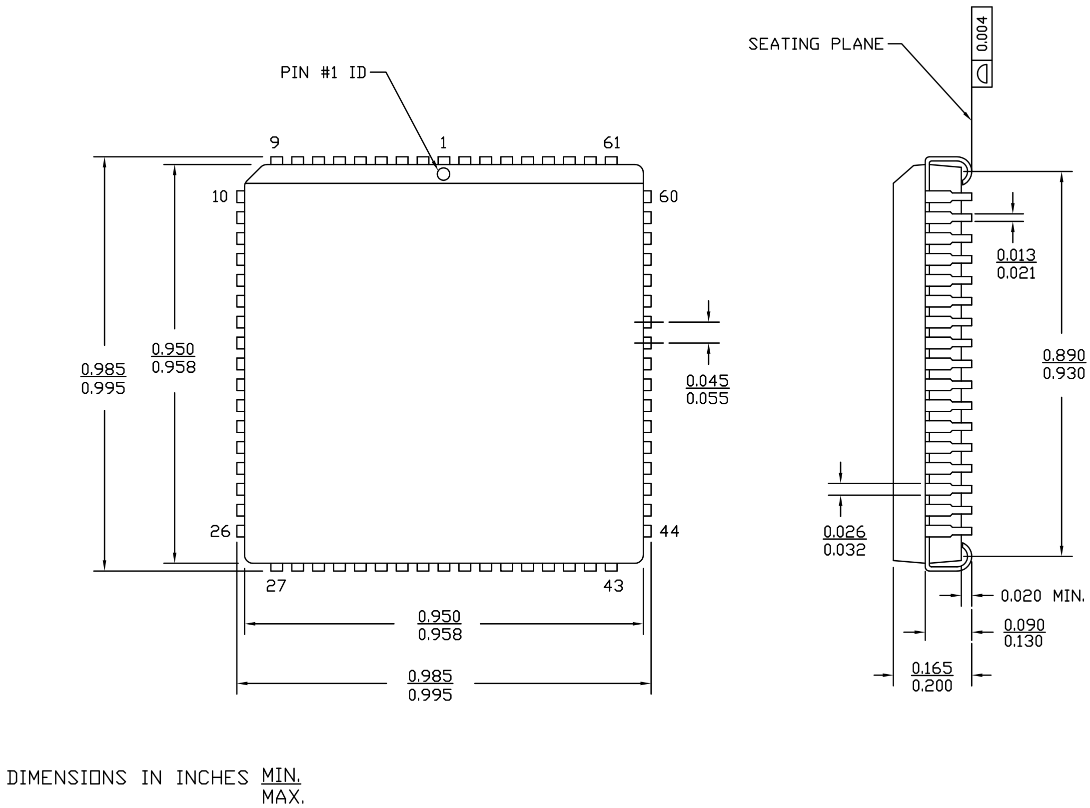
Package Diagrams

Figure 16. 64-pin TQFP (14 × 14 × 1.4 mm) A64SA Package Outline, 51-85046



Package Diagrams *(continued)*

Figure 17. 68-pin PLCC (0.958 × 0.958 Inches) Package Outline, 51-85005



51-85005 *D

Acronyms

Acronym	Description
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{INT}}$	Interrupt
$\overline{\text{OE}}$	Output Enable
PLCC	Plastic Leaded Chip Carrier
R/$\overline{\text{W}}$	Read/Write
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C006A, 16K × 8 Dual-Port Static RAM Document Number: 38-06045				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110197	09/29/01	SZV	Change from Spec number: 38-00831 to 38-06045
*A	122295	12/27/02	RBI	Updated Maximum Ratings: Added Note 2 and referred the same note in “maximum ratings” in description below the heading.
*B	237620	See ECN	YDT	Updated Features: Removed “Pin-compatible and functionally equivalent to IDT7006 and IDT7007”.
*C	345376	See ECN	AEQ	Removed Industrial Temperature Range related information across the document. Updated Ordering Information: Updated part numbers.
*D	387333	See ECN	PCX	Included Pb-Free Logo at the top of the document. Added Industrial Temperature Range related information across the document. Updated Ordering Information: Updated part numbers.
*E	2896210	03/22/2010	RAME	Updated Ordering Information: Updated part numbers. Updated Package Diagrams: spec 51-85046 – Changed revision from *B to *D. spec 51-85065 – Changed revision from *B to *C. spec 51-85005 – Changed revision from *A to *B.
*F	3110296	12/14/2010	EYB	Updated Ordering Information: Updated part numbers. Added Ordering Code Definitions. Minor edits. Updated to new template.
*G	3889996	01/30/2013	SMCH	Removed CY7C007A, CY7C016A, CY7C017A related information across the document. Updated Package Diagrams: spec 51-85046 – Changed revision from *D to *E. Removed spec 51-85065 *C (corresponding to 80-pin TQFP package). spec 51-85005 – Changed revision from *B to *C. Added Acronyms and Units of Measure.
*H	4227411	12/20/2013	SMCH	Updated Ordering Information (Updated part numbers). Updated to new template. Completing Sunset Review.
*I	4580622	11/26/2014	SMCH	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Diagrams: spec 51-85046 – Changed revision from *E to *F.
*J	5553780	12/14/2016	NILE	Updated Package Diagrams: spec 51-85046 – Changed revision from *F to *G. spec 51-85005 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.

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