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Datasheet

DS-CoreControl-TDA21302

TDA21302

Authors: Edward Chang

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http://www.infineon.com/DCDC

Power Management & Supply

Never stop thinking.

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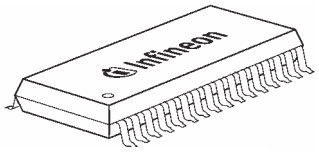
Multi-Phase PWM Controller for CPU Core Power Supply



P-DSO-32

Features :

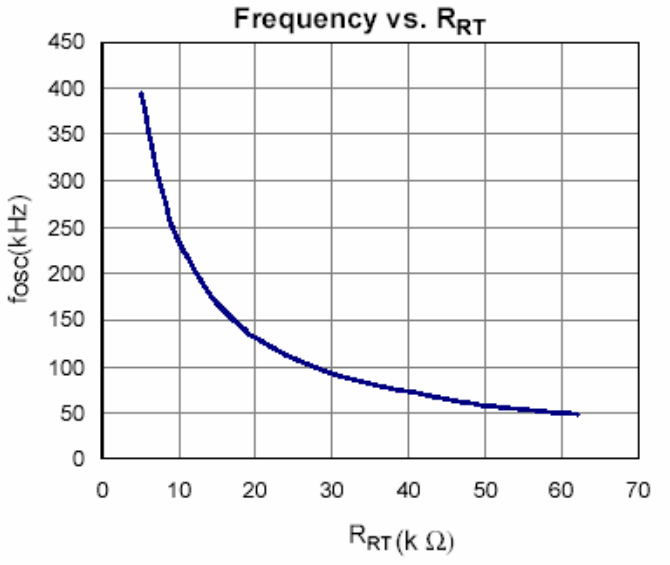
- Multi-Phase PWM Conversion with Automatically Phase Selection
- VRD10.X Compliant
- Active Droop Compensation For Fast Load Response
- Smooth V_{CORE} Voltage Transition during the VID On The Fly
- Power Stage Thermal Balance By Sync FET Rds(on) Current Sense Technique
- Hiccup Mode Over Current Protection
- Programmable Switching Frequency (50KHz ~ 400KHz per Phase), Under Voltage Lockout, and Soft-Start
- High Output Ripple Frequency times numbers of working Channels

Application :

- Intel Processor Voltage Regulator : VRM10.X
- Low Output Voltage High Output Current DC-DC Converters
- Voltage Regulator Modules

Type	Package	Marking	Ordering Code
TDA21302	P-DSO-32	21302	Q67042-S4229

Pinout Drawing and Description :



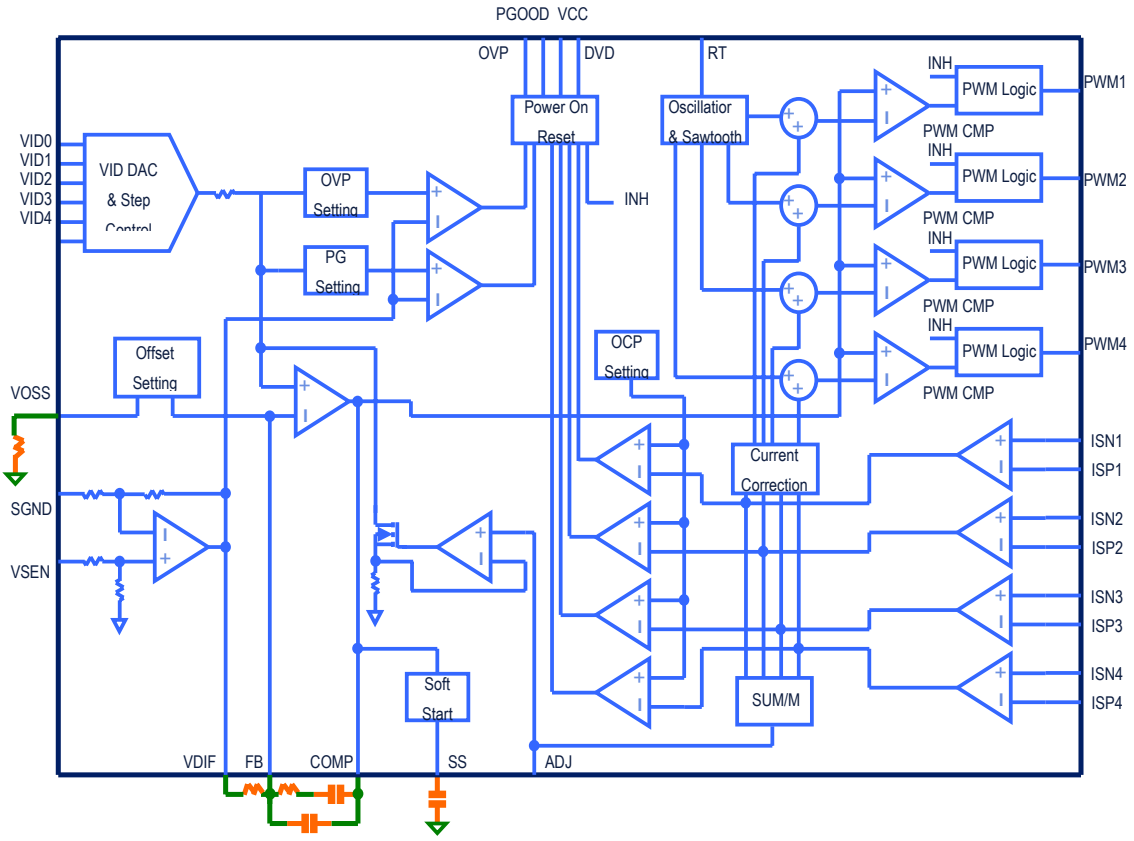
Number	Name	Description
1	OVP	Over voltage trip output
2	PGOOD	Open drain power good signal output pin
3	VID4	Voltage Identification DAC Input. Internally pull up to 3V.
4	VID3	Voltage Identification DAC Input. Internally pull up to 3V.
5	VID2	Voltage Identification DAC Input. Internally pull up to 3V.
6	VID1	Voltage Identification DAC Input. Internally pull up to 3V.
7	VID0	Voltage Identification DAC Input. Internally pull up to 3V.
8	VID125	Voltage Identification DAC Input. Internally pull up to 3V.
9	VOSS	Connect a resistor to GND to set the initial offset voltage.
10	ADJ	Connect a resistor to GND to set the Droop Voltage.
11	SS	Soft-Start. Connect with a capacitor to GND to set the Soft-Start Interval. Pulling down this pin below 1V shall shut the converter down.
12	FB	Internal error amplifier inverting input pin
13	COMP	Output of the error amplifier and input of the PWM comparator
14	VDIF	Output pin of the differential converter output voltage sense
15	ISN4	Differential current sense negative input pin connects to the drain pin of channel 4 Sync FET
16	ISN3	Differential current sense negative input pin connects to the drain pin of channel 3 Sync FET
17	ISN2	Differential current sense positive input pin connects to the drain pin of channel 2 Sync FET
18	ISN1	Differential current sense positive input pin connects to the drain pin of channel 1 Sync FET
19	VSEN	The positive input pin of the differential converter output voltage sense amplifier
20	SGND	The negative input pin of the differential converter output voltage sense amplifier
21	GND	Ground pin of the IC
22	PWM3	Channel 3 PWM output pin. Connect to high level for 2 phase operation.
23	ISP3	Differential current sense positive input pin connects to the source pin of channel 3 Sync FET
24	ISP1	Differential current sense positive input pin connects to the source pin of channel 1 Sync FET
25	PWM1	Channel 1 PWM output pin
26	PWM2	Channel 2 PWM output pin
27	ISP2	Differential current sense positive input pin connects to the source pin of channel 2 Sync FET
28	ISP4	Differential current sense positive input pin connects to the source pin of channel 4 Sync FET
29	PWM4	Channel 4 PWM output pin. Connect to high level for 2 or 3 phase operation.
30	VCC	IC power supply pin connects to 5V
31	DVD	Connect the external voltage divider to program the controller under voltage lockout based on the input voltage of the power stage voltage
32	RT	Connect a resistor to GND to set the channel switching frequency

General Description

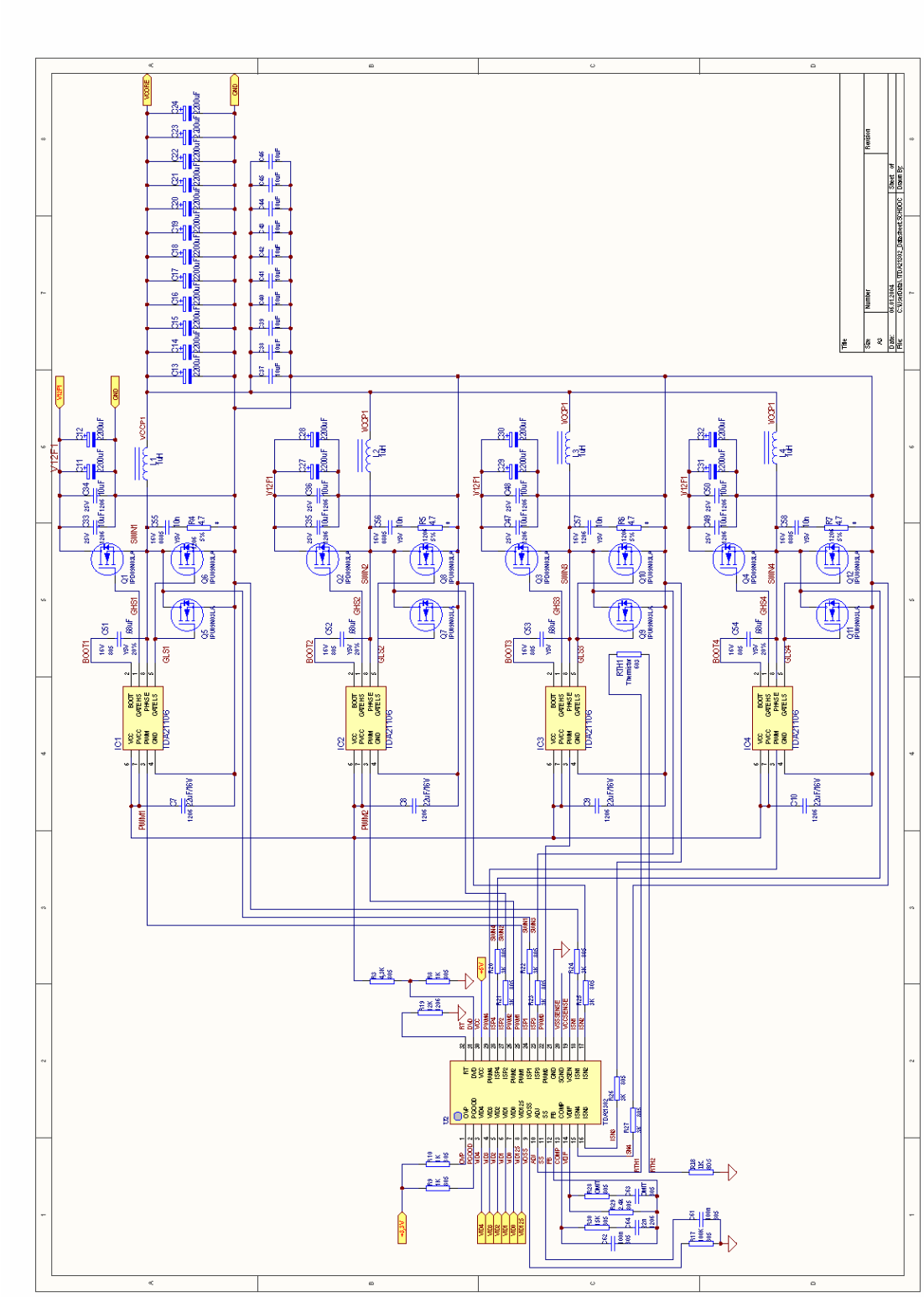
TDA21302 is a multi-phase DC-DC buck converter controller integrated all control functions for the next generation GHz CPU voltage regulator. TDA21302 automatically controls 2 to 4 interleaved buck switching power stage operation. The multi-phase architecture is able to provide high output current with lower power dissipation on the switching devices and minimizing the input ripple current and output ripple voltage. The equivalent high operation frequency optimizes the voltage regulator design for better transient response and thermal performance.

TDA21302 utilizes the Sync FET Rds(on) in every channel as the current sense element. The differential current sense in every channel results precious channel current information to the controller for good droop adjustment, channel current balance, channel switching devices thermal balance and over current protection.

Block Diagram



Reference Schmatic



Absolute Maximum Ratings

At Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Value		Unit
		Min.	Max.	
Voltage supplied to 'VCC' pin; DC	V_{CC}	-0.3	7	V
Input, Output or I/O Pin		-0.3	Vcc+0.3	
Junction temperature	T_J	0	125	°C
Storage temperature	T_S	-65	150	
ESD Rating; Human Body Model		2		KV
ESD Rating; Machine M Model		200		V
IEC climatic category; DIN EN 60068-1		55/150/56		-

Thermal Characteristic

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Thermal resistance, junction-soldering point					K/W
Thermal resistance, junction-ambient				50	

Electrical Characteristic

At Vcc=5V, Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Supply Characteristic						
Bias supply current	I_{CC}	PWM1,2,3,4 Open		12	16	mA
Power On Reset Characteristic						
POR Threshold	V_{CCRTH}	V_{CC} rising threshold	4,0	4,2	4,5	V
Hysteresis	V_{CCHYS}		0,2	0,5		
V_{DVD} Threshold	V_{DVDTP}	Low to High Enable	1,9	2	2,1	
V_{DVD} Hysteresis	V_{DVDHYS}	V_{VCC} falling threshold		0,1		
Oscillator						

Oscillator Frequency Accuracy	f_{OSC}	R_{RT} = 12 KΩ	170	200	230	KHz
Oscillator Frequency Adjustable Range	f_{OSC_ADJ}		50		400	
Ramp Amplitude	ΔV_{OSC}	R_{RT} = 12 KΩ		1,9		V
Ramp Valley	V_{RV}		0,7	1,0		V
Maximum Duty Cycle		Every Phase	62	66	75	%
RT Pin Voltage	V_{RT}	R_{RT} = 12 KΩ	0,55	0,6	0,65	V
Reference and DAC						
DACOUT Voltage Accuracy	ΔV_{DAC}	V_{DAC} ≥ 1V	-1		+1	%
		V_{DAC} < 1V	-10		+10	mV
DAC (VID0~VID125) Input Low		R_{RT} = 12 KΩ			0,4	V
DAC (VID0~VID125) Input High	V_{RV}		0,8			V
DAC (VID0~VID125) Bias Current	I_{BIAS_DAC}		60	120	180	uV
VOSS Pin Voltage	V_{VOSS}	R_{VOSS} = 100 KΩ	0,95	1,0	1,05	V
Error Amplifier						
Open Loop Gain				85		dB
Gain Bandwidth	GBW			10		MHz
Slew Rate	SR	COMP = 10 pF		3		V/uS
Differential Sense Amplifier						
Input Impedance	Z_{IMP}			16		KΩ
Gain Bandwidth	GBW			10		MHz
Slew Rate	SR	COMP = 10 pF		3		V/uS
Differential Current Sense GM Amplifier						
ISP1, 2, 3, 4 Full Scale Source Current	I_{ISPFSS}		60			uA
ISP1, 2, 3, 4 Current for OCP	I_{ISPOCP}			100		uA

At Vcc=5V, Tj = 25 °C, unless otherwise specified

Protection						
SS Current	Iss	Vss = 1V	8	13	18	uA
Over Voltage Trip (V_{SENSE} / DACOUT)	ΔV_{OVT}		130	140	150	%
OVP Voltage	V_{OVP}	I_{OVP} = 10mA	2,2	3,28	4,0	V
Power Good						
Power Good Rising Threshold (V_{SENSE} / DACOUT)	V_{PG}	V_{SENSE} Rising		92		%
Power Good Low Voltage	V_{PGL}	I_{PG} = 4mA			0,2	V

Operating Conditions

At Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Voltage supplied to 'VCC' pins	V_{VCC}		4,5	5,0	5,5	V
Ambient temperature	T_A		0		70	°C
Junction temperature	T_J		0		125	°C

VRD10,X VID Table

Pin Names								Pin Names						
VID125	VID4	VID3	VID2	VID1	VID0	Vcore		VID125	VID4	VID3	VID2	VID1	VID0	Vcore
0	0	1	0	1	0	0,8375		0	1	1	0	1	0	1,2125
1	0	1	0	0	1	0,8500		1	1	1	0	0	1	1,2250
0	0	1	0	0	1	0,8625		0	1	1	0	0	1	1,2375
1	0	1	0	0	0	0,8750		1	1	1	0	0	0	1,2500
0	0	1	0	0	0	0,8875		0	1	1	0	0	0	1,2625
1	0	0	1	1	1	0,9000		1	1	0	1	1	1	1,2750
0	0	0	1	1	1	0,9125		0	1	0	1	1	1	1,2875
1	0	0	1	1	0	0,9250		1	1	0	1	1	0	1,3000
0	0	0	1	1	0	0,9375		0	1	0	1	1	0	1,3125
1	0	0	1	0	1	0,9500		1	1	0	1	0	1	1,3250
0	0	0	1	0	1	0,9625		0	1	0	1	0	1	1,3375
1	0	0	1	0	0	0,9750		1	1	0	1	0	0	1,3500
0	0	0	1	0	0	0,9875		0	1	0	1	0	0	1,3625
1	0	0	0	1	1	1,0000		1	1	0	0	1	1	1,3750
0	0	0	0	1	1	1,0125		0	1	0	0	1	1	1,3875
1	0	0	0	1	0	1,0250		1	1	0	0	1	0	1,4000
0	0	0	0	1	0	1,0375		0	1	0	0	1	0	1,4125
1	0	0	0	0	1	1,0500		1	1	0	0	0	1	1,4250
0	0	0	0	0	1	1,0625		0	1	0	0	0	1	1,4375
1	0	0	0	0	0	1,0750		1	1	0	0	0	0	1,4500
0	0	0	0	0	0	1,0875		0	1	0	0	0	0	1,4625
1	1	1	1	1	1	OFF		1	0	1	1	1	1	1,4750
0	1	1	1	1	1	OFF		0	0	1	1	1	1	1,4875
1	1	1	1	1	0	1,1000		1	0	1	1	1	0	1,5000
0	1	1	1	1	0	1,1125		0	0	1	1	1	0	1,5125
1	1	1	1	0	1	1,1250		1	0	1	1	0	1	1,5250
0	1	1	1	0	1	1,1375		0	0	1	1	0	1	1,5375
1	1	1	1	0	0	1,1500		1	0	1	1	0	0	1,5500
0	1	1	1	0	0	1,1625		0	0	1	1	0	0	1,5625
1	1	1	0	1	1	1,1750		1	0	1	0	1	1	1,5750
0	1	1	0	1	1	1,1875		0	0	1	0	1	1	1,5875
1	1	1	0	1	0	1,2000		1	0	1	0	1	0	1,6000

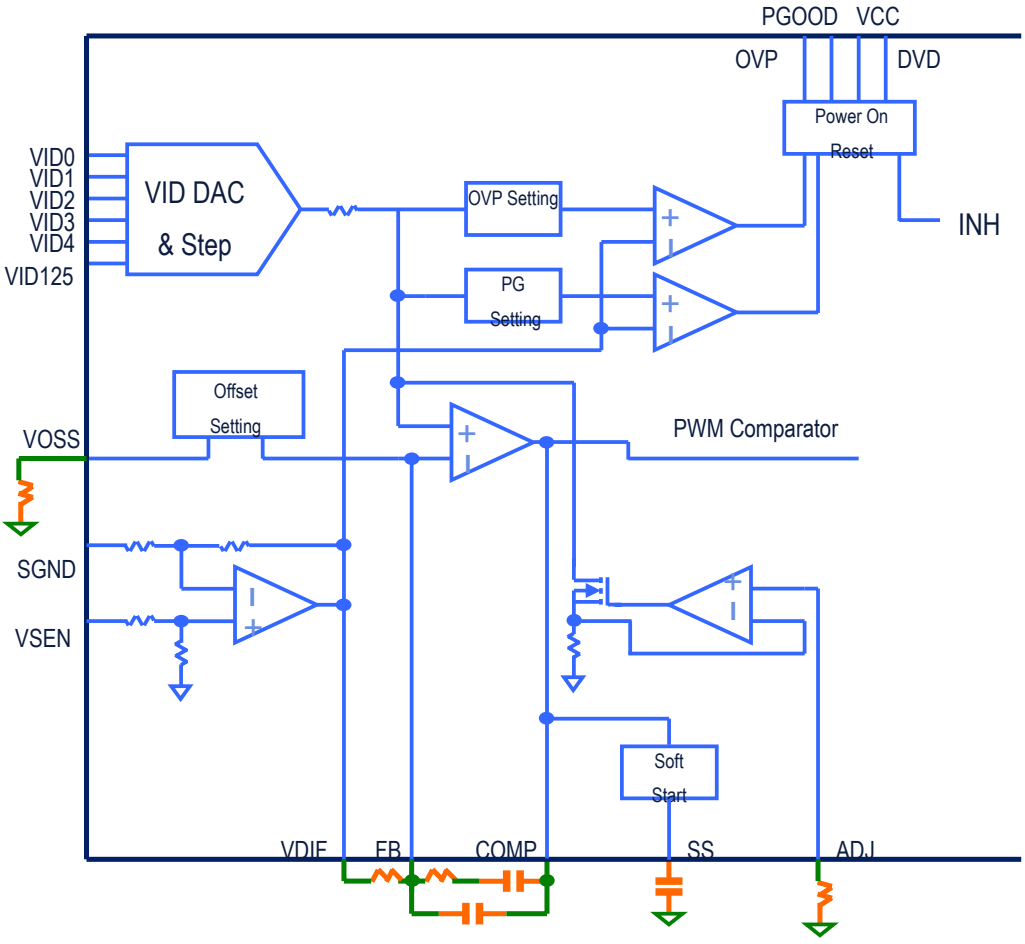
Note : “ 1 “ is open and “ 0 “ is connecting to ground.

Application Information :

TDA21302 is a multi-phase DC/DC controller that precisely regulates CPU core voltage and balances the current of different power channels. The converter consisting of TDA21302 and its companion drivers, TDA21106 and TDA21102, provides high quality CPU power and all the protection functions to meet the requirement of the latest VRMs.

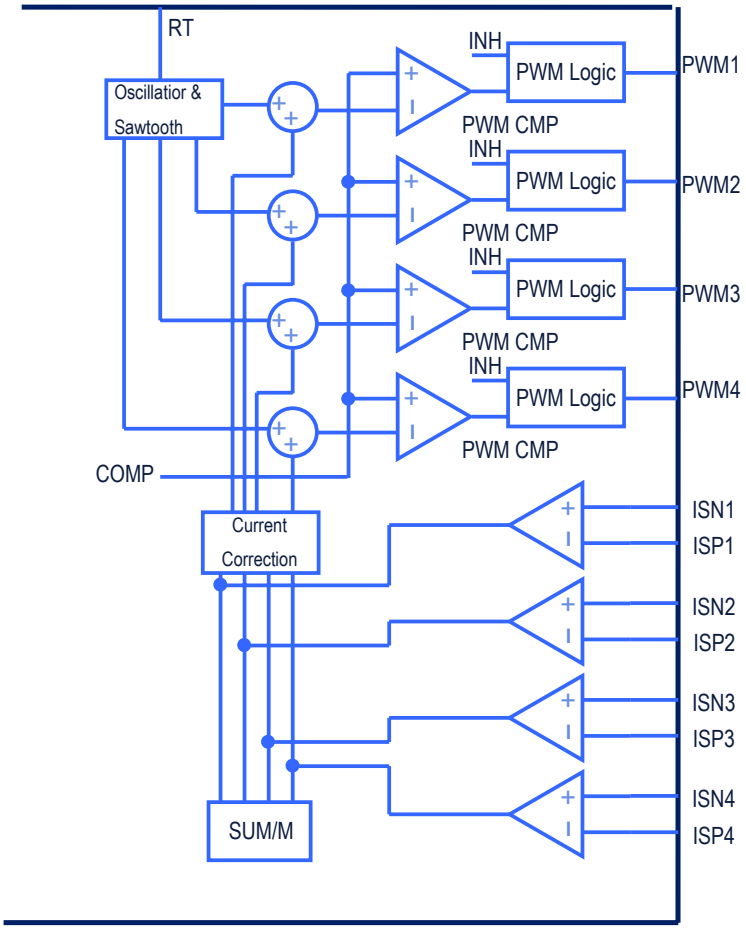
Voltage Control

The TDA21302 senses the CPU V_{CORE} by an precise instrumental amplifier to minimize the voltage drop on the PCB trace at heavy load condition. VSEN & SGND are the differential input pins for V_{CORE} and their output, VDIF, is the input of the PGOOD & OVP sense. The internal highly accurate VID DAC provides the reference voltage for VRD10,X compliance. Control loop consists of error amplifier, pulse width modulator, external driver ICs and power components. Like conventional voltage mode controller, the output voltage is locked at the V_{REF} of the error amplifier and the error signal is used as the control signal Vc of the pulse width modulator. The PWM signals of different channels are generated by comparison of EA output and split-phase saw-tooth wave. Power stage transforms V_{IN} to output by PWM signal on-time ratio.



Current Balance

TDA21302 senses the current of the Sync FET in each phase when it is conducting for channel balance and droop tuning. The differential sensing GM amplifier converts the voltage on the sense components which can be sense resistors or the Rds(on) of the Sync FET to current signal into internal balance circuit. The current balance circuit sums and averages the current signals and then generates the balancing signals injected to pulse signal modulator. If some of the channel current is higher than average, the balancing signal shall decrease the pulse width to keep the current balance.



Load Droop

The sensed channel current signals regulated the reference of DAC to form a output voltage droop proportional to the load current. The droop or so-called “ Active Voltage Positioning “ can reduce the output voltage ripple during the load transient and the size of the LC filters.

Fault Detection

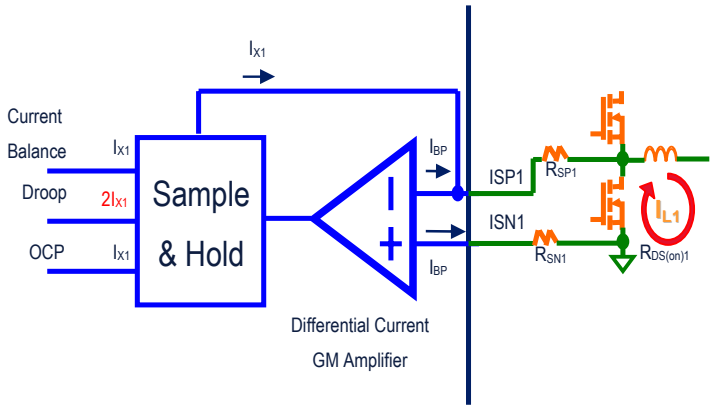
The chip detects V_{CORE} for over voltage and power good detection. The “ hiccup mode “ operation of over-current protection is adopted to reduce the short circuit current. The inrush current at the start up is suppressed by the soft start circuit through clamping the pulse width and output voltage.

Phase Setting and Converter Start Up

The TDA21302 interfaces with companion MOSFET drivers, TDA21106 (Single Channel) and TDA21102 (Dual Channel), for correct converter initialization. The tri-state PWM output pins sense the interface voltage at IC POR period (both VCC and DVD trip). The channel is enabled if the voltage at the pin is 1,2V less than VCC. Please tie the PWM outputs to VCC and the current sense pins to GND or leave them floating if the channel is unused. For 3 Phase application, connect PWM4 high.

Current Sensing Setting

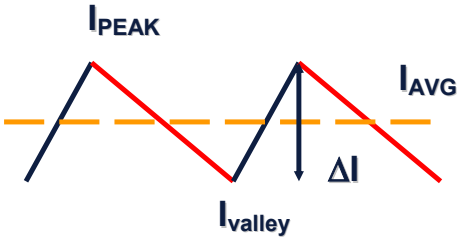
TDA21302 senses the current of the Sync FET in each phase when it is conducting for channel balance and droop tuning. The differential sensing GM amplifier converts the voltage on the sense components which can be sense resistors or the Rds(on) of the Sync FET to current signal into internal balance circuit.



Basic Theory

$$V_+ = I_{BP} \times R_{SN1} \ , \ V_- = (I_{BP}+I_{X1}) \times R_{SP1} - I_{L1\_VALLEY} \times R_{DS(on)1}$$

$$\because V_+ = V_- \ \text{and} \ R_{SN1} = R_{SP1} \quad \Rightarrow \quad \therefore I_{X1} = I_{L1\_VALLEY} \times \frac{R_{DS(on)1}}{R_{SP1}}$$



$$\Delta I = \frac{V_O \times T_{OFF}}{L}$$

The sensing circuit gets $I_X = \frac{I_L \times R_S}{R_{SP}}$ by local feedback. R_{SP} = R_{SN} to cancel the voltage drop caused by GM amplifier input bias current. I_X is sampled and held just before low side MOSFET turns off. Therefore,

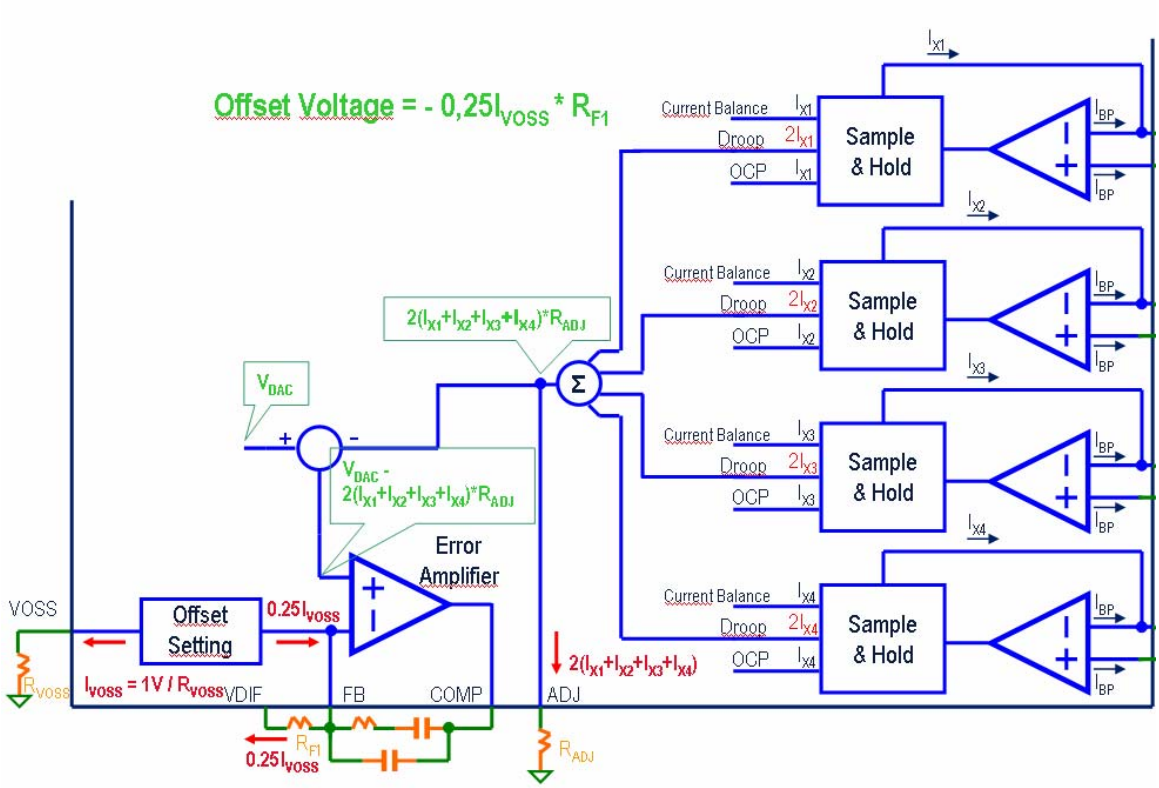
$$I_{X\,(S/H)}=\frac{I_{L\,(S/H)}\times R_S}{R_{SP}},\ I_{L\,(S/H)}=I_{L\,(AVG)}-\frac{V_O\times T_{OFF}}{2L},\ T_{OFF}=\left[\frac{V_{IN}-V_O}{V_{IN}}\right]\times 3{,}3uS \text{ for } F_{OSC}=300\text{ KHz}$$

$$\therefore\ I_{X\,(S/H)}=\left[I_{L\,(AVG)}-\frac{V_O\times\left[\frac{V_{IN}-V_O}{V_{IN}}\right]\times 3{,}3uS}{2L}\right]\times\frac{R_S}{R_{SP}}$$

DAC Offset Voltage & Droop Setting

The DAC offset voltage is set by compensation network & external resistor at VOSS pin by $\frac{1V}{R_{VOSS}}\times\frac{R_{f1}}{4}$

The S/H current signals from power channel are injected to ADJ pin to establish the droop voltage. V_{ADJ} = R_{ADJ} X $\sum 2I_X$. The DAC output voltage decreased by V_{ADJ} to generate the V_{CORE} load droop.

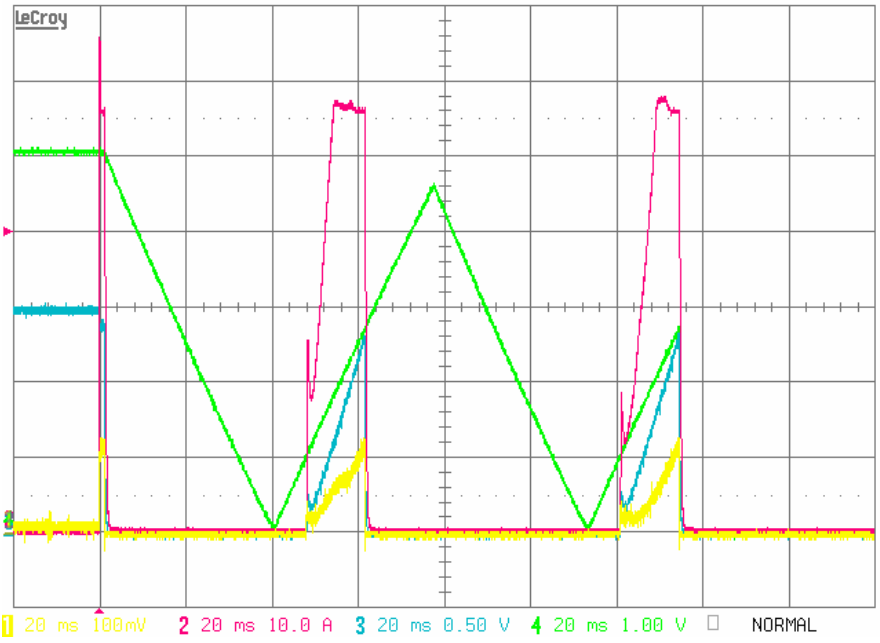


Protection and SS Function

For OVP, the TDA21302 detects the VCORE by VDIF pin voltage that is the output of the differential amplifier. This is to eliminate the delay caused by the compensation network for faster and more accurate detection. The trip point of OVP is 140% of the normal V_{CORE} voltage level. The PWM outputs are pulled low to turn on the Sync FET and to turn off the control FET while OVP is detected. The OVP latch can only be reset by either VCC or DVD. The PGOOD trip point is set at the 92% of the normal V_{CORE} voltage level. The open drain PGOOD pin shall be pulled low while V_{CORE} is lower than this point. During the VID on the fly condition, there is nothing able to change the status of the PGOOD.

Soft-start circuit generates a ramp by charging an external capacitor with a 13uA constant current source after the POR of IC is active. The pulse width of PWM signal and V_{CORE} are clamped by rising ramp to reduce the inrush current and protect the power devices.

Over-current protection trip point is internally set at around 100uA for each channel. OCP is triggered if one channel S/H current signal. Controller forces PWM output latched at high impedance to turn off both control and Sync FETs in the power stage and initial the hiccup mode protection. The SS pin voltage is pulled low with a 13uA current after it is less than 90% VCC. The converter restarts after SS pin voltage is lower than 0,2V. Three times of OCP disable the converter and only release the latch by POR acts.



CH1 : V_{ADJ}

CH2 : Short Circuit Current

CH3 : V_{CORE}

CH4 : V_{SS}

Design Process Suggestion :

Voltage Loop Setting

- Pole and Zero of output filter : Output inductor value, the capacitance and ESR value of the output capacitors
- Compensation Network : Error amplifier compensation & sawtooth wave amplitude.
- Kelvin sense for V_{CORE}

Current Loop Setting

- GM amplifier S/H current setting : Current sensing components (Rds(on)), the value of the resistors connecting to ISPx & ISNx. Do keep ISPx current < 60uA at full load condition for better load line linearity.
- Over current protection trip point : This has been set internally and please keep ISPx < 100uA at OCP condition for better accuracy.

VRM Load Line Setting

- Droop amplitude : External ADJ pin resistor.
- No load offset : Additional resistor in compensation network.
- DAC offset voltage seeting : VOSS pin & compensation network resistor.

PCB Layout

- Kelvin sense for current sense GM amplifier input.
- Refer to layout guide for other item.

Design Example :

Given

Apply for four phase converter

V_{IN} = 12V
V_{CORE} = 1,35V
I_{LOAD} = 100A
V_{DROOP} = 100 mV at full load
OCP set at 35A for each channel (S/H)
Rds(on) = 3 mΩ for Sync FET at 25°C (2 X IPU06N03LA in parallel)
L_{OUT} = 0,6uH
C_{OUT} = 17,600 uH with 1 mΩ ESR

1. Compensation Setting

- ***Modulator Gain, Pole and Zero :***

From the following formula ;

Modulator Gain = $\frac{V_{IN}}{V_{RAMP}} = \frac{12V}{1,9V \times \frac{3}{2}} = 4,2$ (12,46 dB)

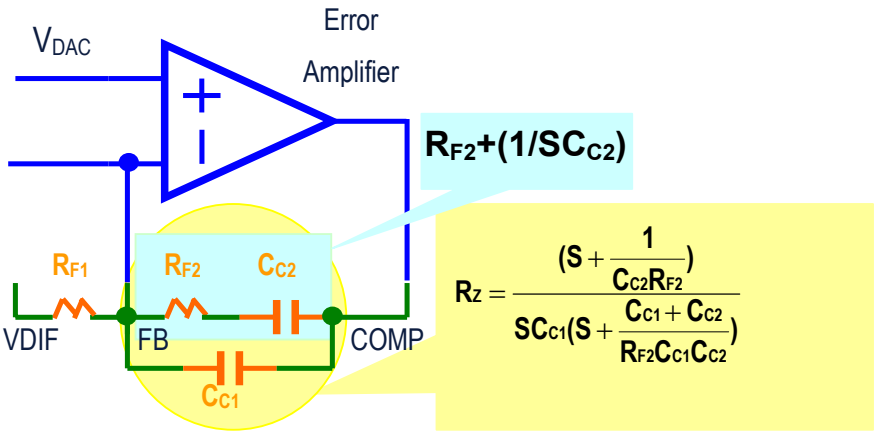
Where V_{RAMP} : ramp amplitude of the sawtooth waveform

LC Filter Pole = $\frac{1}{2\pi \times \sqrt{LC}}$ = 1,549 KHz and

ESR Zero = $\frac{1}{2\pi \times ESR \times COUT}$ = 9,0429 KHz

- ***EA Compensation Network :***

Select R_{F1} = 2,4 KΩ , R_{F2} = 24 KΩ , C_{C2} = 6,6 nF, C_{C1} = 33 pF and Use type 2 compensation scheme shown in Figure 5.

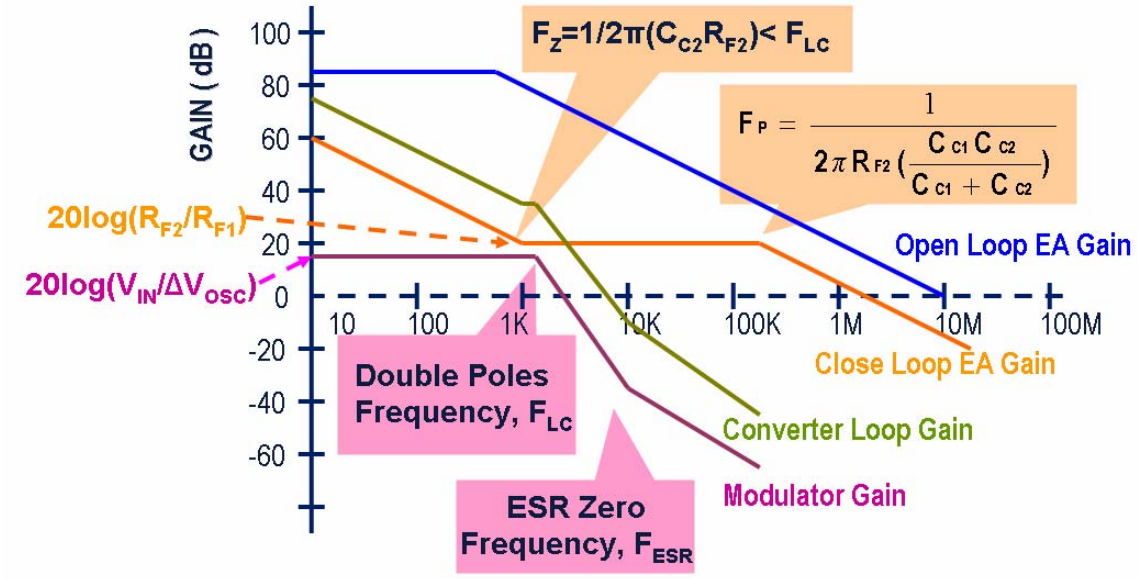


From the following formulas :

$$F_Z = \frac{1}{2\pi \times R_{F2} \times C_{C1}} = 1\ \text{KHz}, \quad F_P = \frac{1}{2\pi \times R_{F2} \times \frac{C_{C1} \times C_{C2}}{C_{C1}+C_{C2}}} = 200\ \text{KHz}$$

$$\text{Middle Band Gain} = \frac{R_{F2}}{R_{F1}} = 10\ (20\ \text{dB})$$

The asymptotic bode plot of EA compensation and PWM loop gain is shown as below.



2. Droop & DAC Offset Setting

For each channel the load current is 100A / 4 = 25A and the ripple current, ΔI_L , is given as

$$3{,}33uS \times \frac{1{,}35V}{0{,}6uH} \times \left(1 - \frac{1{,}35V}{12V}\right) = 6{,}65\ A$$

The load current, IL, at S/H is 25A - $\frac{\Delta I}{2}$ = 21,675 A.

Using the following formula to select the appropriate $I_{X(MAX)}$ for the S/H of GM amplifier :

$$I_{X(MAX)} = \frac{R_{DS(ON)} \times 21{,}675A}{R_{SP}}$$

The suggested I_X is in the range of 50 uA ± 5uA, select R_{SP} = R_{SN} = 1,5 KΩ, then $I_{X(MAX)}$ would be 43,35 uA. V_{DROOP} = 100 mV = 43,35 uA X 2 X 4 X R_{ADJ}, therefore R_{ADJ} = 287 Ω.

The $R_{DS(ON)}$ of MOSFET varies with temperature rise. When the Sync FETs are working at 100°C junction temperature, the $R_{DS(ON)}$ of MOSFET at 100°C is given as 7,3 mΩ. So the R_{ADJ} at 100°C is given as :

$$R_{ADJ\_100°C} \text{ X } (R_{DS(ON)\_25°C} / \ R_{DS(ON)\_100°C}) = \ 236\ \Omega$$

3. Over Current Protection Setting

OCP trip point is internally set at around 100 uA of I_X for each channel. As above selected R_{SP} = R_{SN} = 1,5 KΩ, the OCP trip point is found using :

$$I_{X(OCP)} = \frac{R_{DS(ON)} \times I_{L(TRIP)}}{R_{SP}} = \frac{3m\Omega \times I_{L(TRIP)}}{1{,}5K\Omega} = 100uA$$

4. Soft-start Capacitor Selection

C_{SS} = 100 nF is the suitable value for most application.

$$I_{SS} \times t_{SS} = V_{SS} \times C_{SS} \Rightarrow C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{SS}}$$

I_{SS} = 13 uA , V_{SS} = 2V , t_{SS} = 10 mS

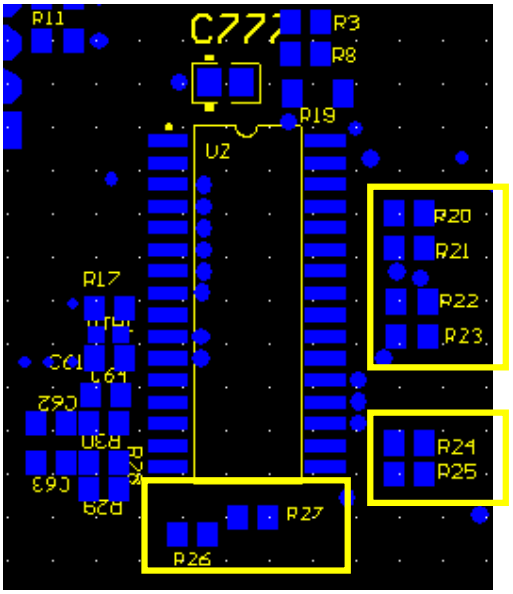
C_{SS} = 65 nF

Layout Guide :

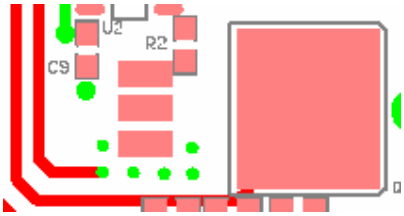
Place the high-power switching components first, and separate them from the sensitive nodes.

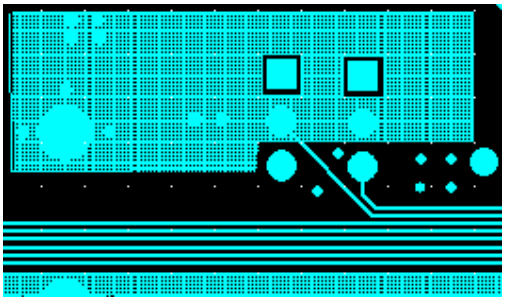
1. Most Critical Path :

The current sense circuit is the most sensitive part of the converter. The current sense resistor tied to ISP1,2,3,4 and ISN1,2,3,4 should be located not more than 0,5 inch from the IC and away from the noise switching nodes. The PCB trace of sense nodes should be parallel and as short as possible. Kelvin connection of the sense component, additional current sense resistor or the $R_{DS(ON)}$ of MOSFETs, ensures the accurate and stable current sensing signals.



DPAK or
D^2PAK

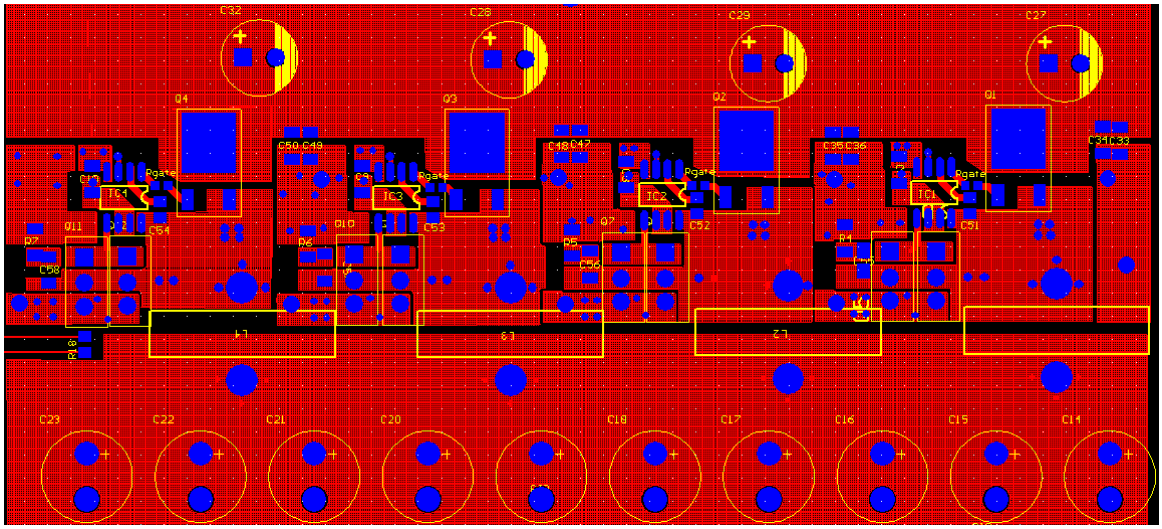




IPAK

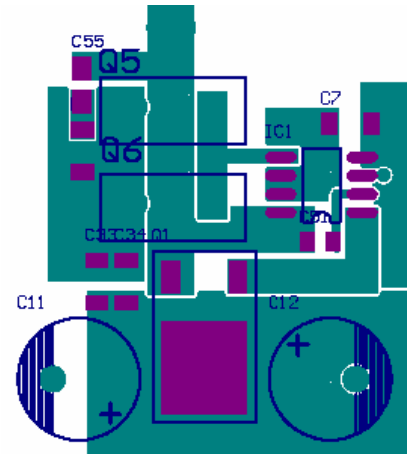
2. Switching Ripple Path :

- The best connection of the input capacitors is to place at the drain of the high side MOSFET and the source of the low side MOSFET.
- Low side MOSFET to the output capacitor.
- The return path of input and output capacitor.
- Separate the power and signal GND.
- The PHASE node, the conjunction of the high / low side MOSFETs and inductor, is the nosiy node. Keep them away from the sensitive small-signal node.
- Reducing the parasitic impedance and inductance is done by minimizing the length of the traces, offering enough copper area and avoiding the vias.



3. MOSFET drivers :

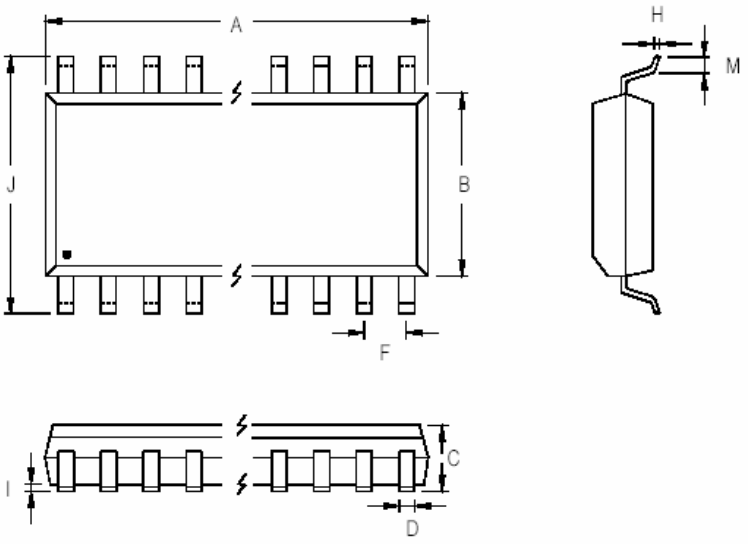
- Both of the decoupling capacitors for VCC and PVCC should be placed as close to the driver IC as possible.
- The bootstrap capacitor should be placed close to the **BOOT** pin.
- The traces of **$GATE_{HS}$** and **PHASE** should be routed in parallel and to keep it short and wide. The width of the trances should be no less than 40mils.
- High current loops from the input capacitor, high side MOSFET, output inductors and output capacitors back to the input capacitor negative terminal should be kept the distance minimized.
- The conjunction of high side MOSFET, low side MOSFET and output inductor should be kept as close as possible.



4. Other Path :

- The components from the compensation network, high frequency bypass capacitors and the setting resistors should be placed near controller IC and away from the noisy power path.
- The thermal compensation thermistor should be placed at the hottest point which is normally the MOSFETs located at the inner part of the power stage.

Outline Dimension :



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	20.32	20.73	0.800	0.816
B	7.39	7.59	0.291	0.299
C	2.36	2.64	0.093	0.104
D	0.33	0.51	0.013	0.020
F	1.27		0.050	
H	0.23	0.33	0.009	0.013
I	0.10	0.30	0.004	0.012
J	10.01	10.64	0.394	0.419
M	0.38	1.27	0.015	0.050

32-Lead SOP Plastic Package

Revision History			
Datasheet DS-CoreControl-TDA21302			
Actual Release: V1.2 Date: 10.04.2004		Previous Release: V1.1	Date: 10.01.04
Page of actual Rel.	Page of prev. Rel.	Subjects changed since last release	
17	17	C_{C1} = 6,6 nF, C_{C2} = 33 pF => C_{C2} = 6,6 nF, C_{C1} = 33 pF	
10	10	**VID table correction VID4 1→ 0 from 1,0375V to 1,0875v**	

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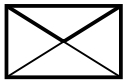

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