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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

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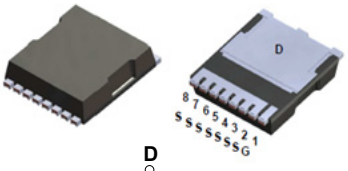
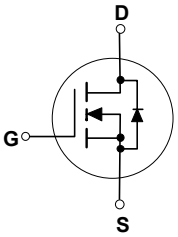
ON Semiconductor®

FDBL0200N100

N-Channel PowerTrench® MOSFET

100 V, 300 A, 2.0 mΩ





Features

- Typical $R_{DS(on)}$ = 1.5 mΩ at V_{GS} = 10V, I_D = 80 A
- Typical $Q_{g(tot)}$ = 95 nC at V_{GS} = 10V, I_D = 80 A
- UIS Capability
- RoHS Compliant

Applications

- Industrial Motor Drive
- Industrial Power Supply
- Industrial Automation
- Battery Operated tools
- Battery Protection
- Solar Inverters
- UPS and Energy Inverters
- Energy Storage
- Load Switch

For current package drawing, please refer to the Fairchild website at http://www.fairchildsemi.com/dwg/PS/PSOF08A.pdf.

MOSFET Maximum Ratings T_J = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-to-Source Voltage		100	V
V_{GS}	Gate-to-Source Voltage		±20	V
I_D	Drain Current - Continuous (V_{GS}=10) (Note 1)	T_C = 25°C	300	A
	Pulsed Drain Current	T_C = 25°C	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy	(Note 2)	352	mJ
P_D	Power Dissipation		429	W
	Derate Above 25°C		2.9	W/°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 3)	0.35	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 3a)	43	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 3b)	62.5	°C/W

Notes:
1: Current is limited by silicon.
2: Starting T_J = 25°C, L = 0.1mH, I_{AS} = 84A, V_{DD} = 100V during inductor charging and V_{DD} = 0V during time in avalanche.
3: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design.
a) 43 °C/W when mounted on a 1 in^2 pad of 2 oz copper
b) 62.5 °C/W when mounted on a minimum pad of 2 oz copper

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDBL0200N100	FDBL0200N100	MO-299A	13"	24mm	2000 units

Semiconductor Components Industries, LLC, 2016
December, 2016, Rev. 1.1

Publication Order Number:
FDBL0200N100/D

Electrical Characteristics T_J = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
B_{VDSS}	Drain-to-Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	100	-	-	V
I_{DSS}	Drain-to-Source Leakage Current	V_{DS}=100V, V_{GS} = 0V, T_J = 25°C	-	-	5	μA
		V_{DS}=100V, V_{GS} = 0V, T_J = 175°C (Note 4)	-	-	2	mA
I_{GSS}	Gate-to-Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	2.0	3.1	4.5	V
$R_{DS(on)}$	Drain to Source On Resistance	I_D = 80A, V_{GS}= 10V, T_J = 25°C	-	1.5	2.0	mΩ
		I_D = 80A, V_{GS}= 10V, T_J = 175°C (Note 4)	-	3.3	4.3	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 50V, V_{GS} = 0V, f = 1MHz	-	6970	9760	pF
C_{oss}	Output Capacitance		-	3950	5530	pF
C_{rss}	Reverse Transfer Capacitance		-	29	41	pF
R_g	Gate Resistance	f = 1MHz	-	0.45	1	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10V	V_{GS} = 0 to 10V, V_{DD} = 80V, I_D = 80A	-	95	133	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2V, V_{DD} = 80V, I_D = 80A	-	13	-	nC
Q_{gs}	Gate-to-Source Gate Charge	V_{DD} = 80V, I_D = 80A	-	31	-	nC
Q_{gd}	Gate-to-Drain “Miller“ Charge	V_{DD} = 80V, I_D = 80A	-	20	-	nC
Switching Characteristics						
t_{on}	Turn-On Time	V_{DD} = 50V, I_D = 80A, V_{GS} = 10V, R_{GEN} = 6Ω	-	-	73	ns
$t_{d(on)}$	Turn-On Delay		-	31	50	ns
t_r	Rise Time		-	25	40	ns
$t_{d(off)}$	Turn-Off Delay		-	36	58	ns
t_f	Fall Time		-	9	18	ns
t_{off}	Turn-Off Time		-	-	59	ns
Drain-Source Diode Characteristics						
V_{SD}	Source-to-Drain Diode Voltage	I_{SD} =80A, V_{GS} = 0V	-	-	1.25	V
		I_{SD} = 40A, V_{GS} = 0V	-	-	1.2	V
t_{rr}	Reverse-Recovery Time	I_F = 80A, dI_{SD}/dt = 100A/μs, V_{DD}=80V	-	115	184	ns
Q_{rr}	Reverse-Recovery Charge		-	172	273	nC

Note:

4: The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

Typical Characteristics

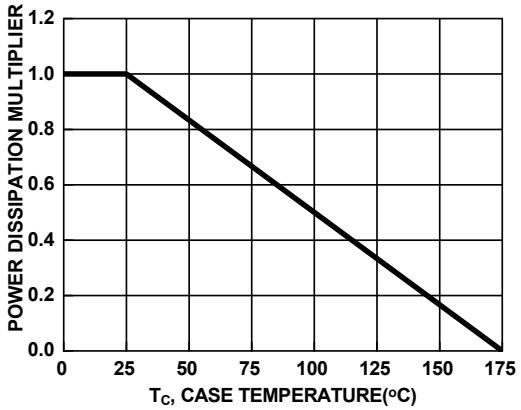


Figure 1. Normalized Power Dissipation vs. Case Temperature

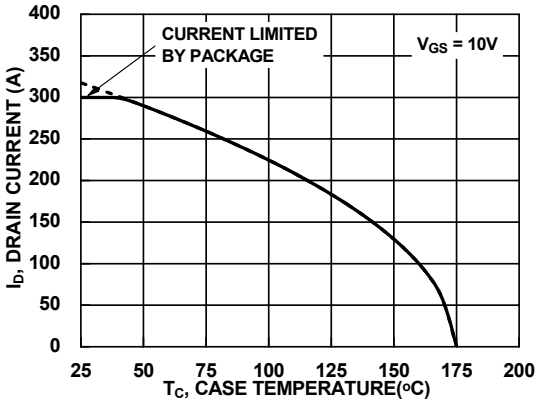


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

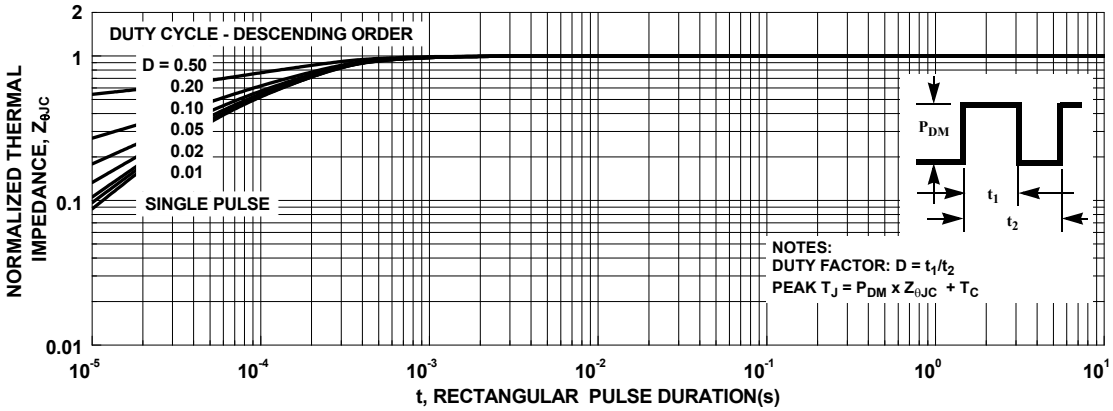


Figure 3. Normalized Maximum Transient Thermal Impedance

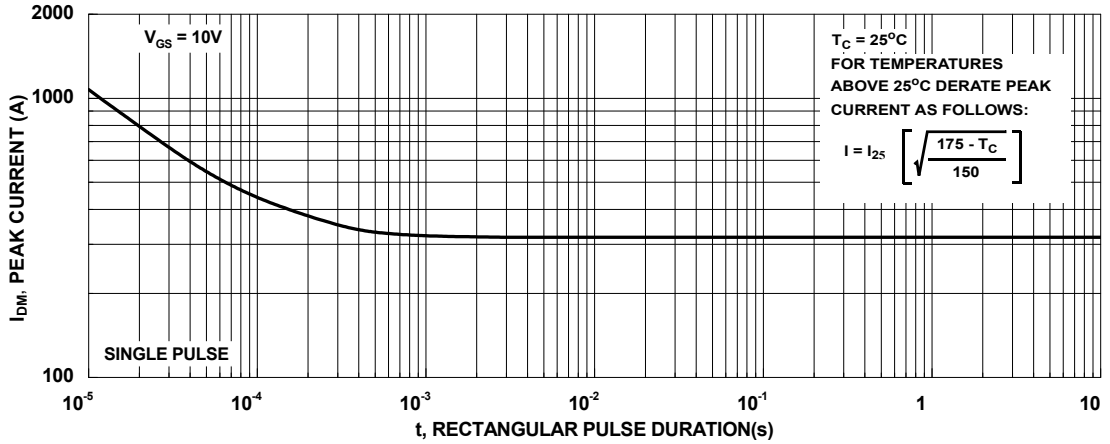


Figure 4. Peak Current Capability

Typical Characteristics

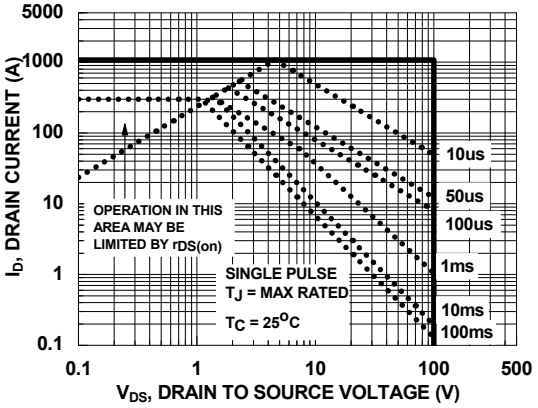
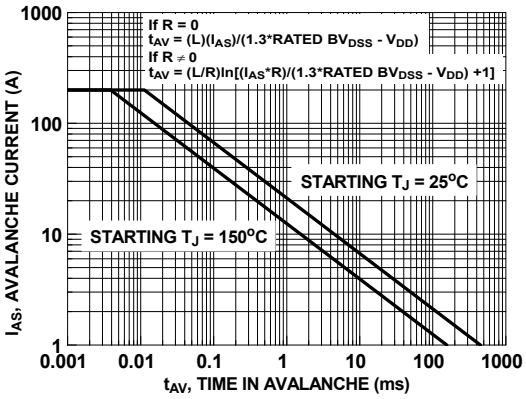


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

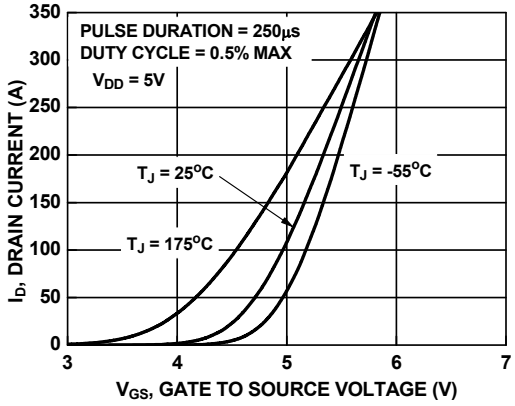


Figure 7. Transfer Characteristics

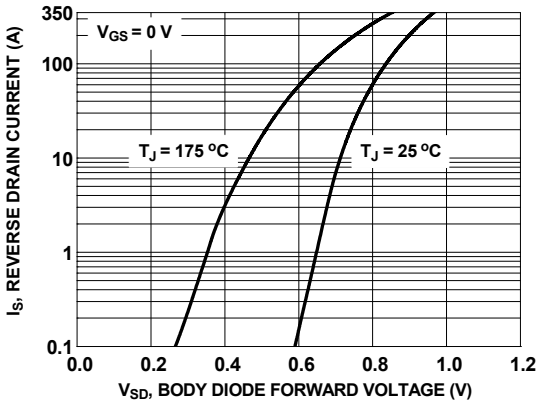


Figure 8. Forward Diode Characteristics

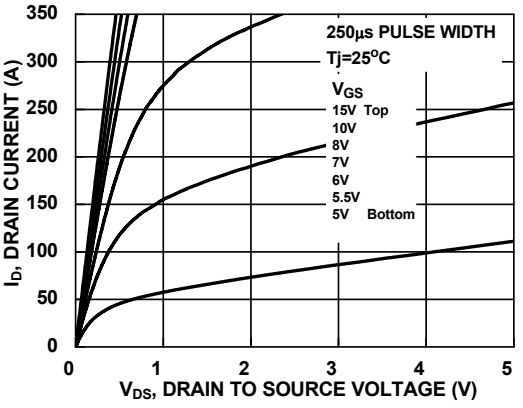


Figure 9. Saturation Characteristics

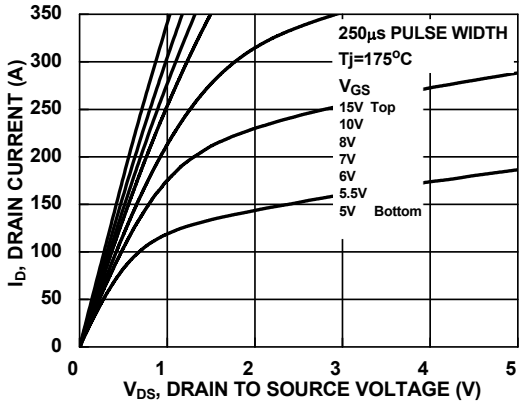


Figure 10. Saturation Characteristics

Typical Characteristics

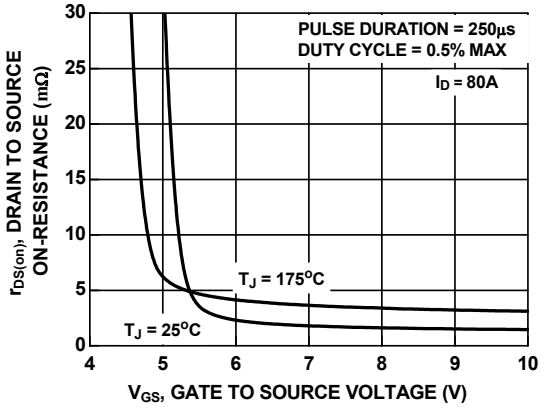


Figure 11. R_{DSON} vs. Gate Voltage

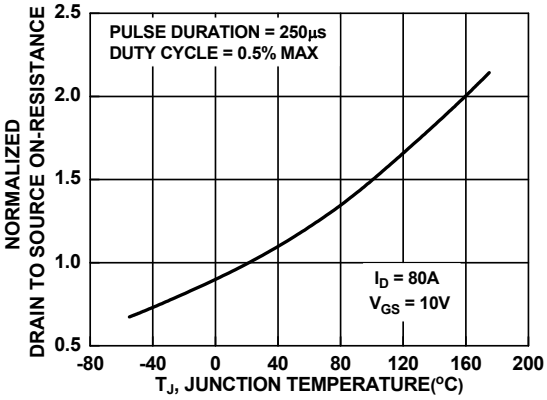


Figure 12. Normalized R_{DSON} vs. Junction Temperature

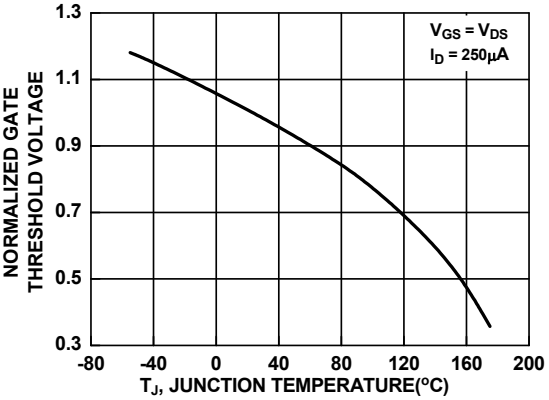


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

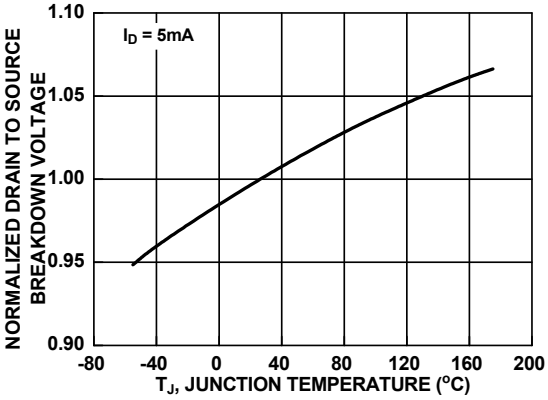


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

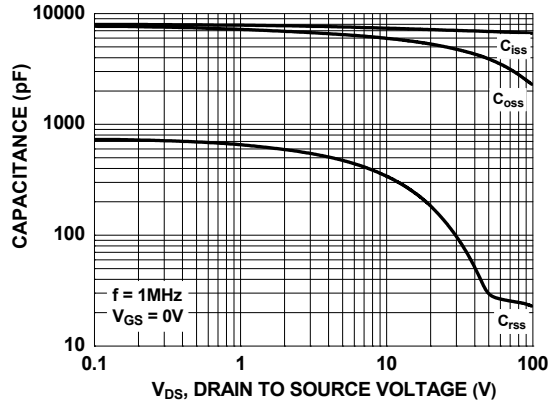


Figure 15. Capacitance vs. Drain to Source Voltage

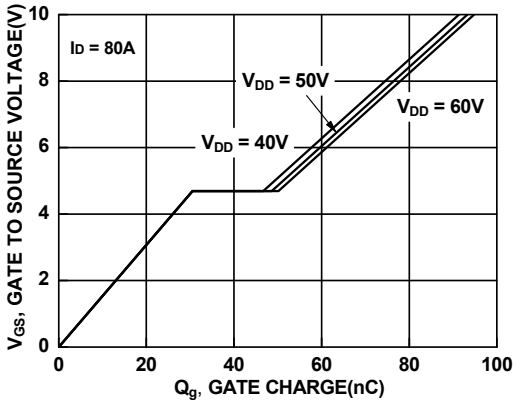
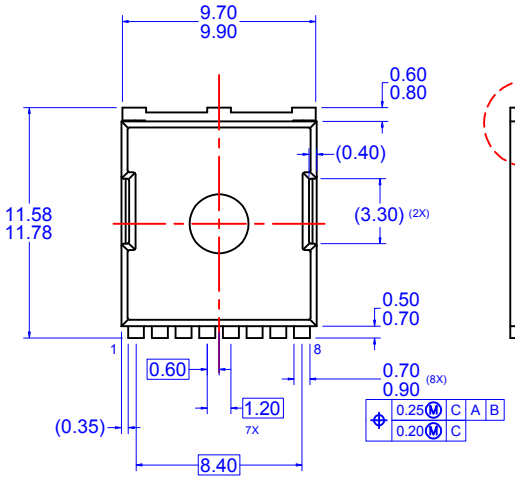
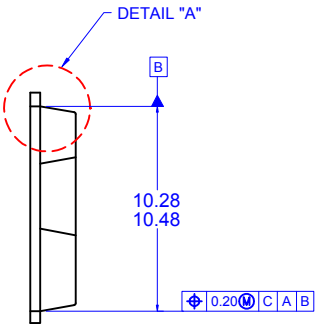
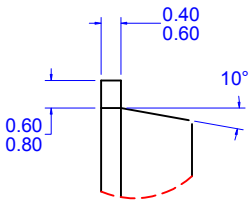


Figure 16. Gate Charge vs. Gate to Source Voltage

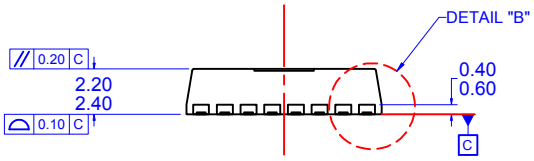


TOP VIEW

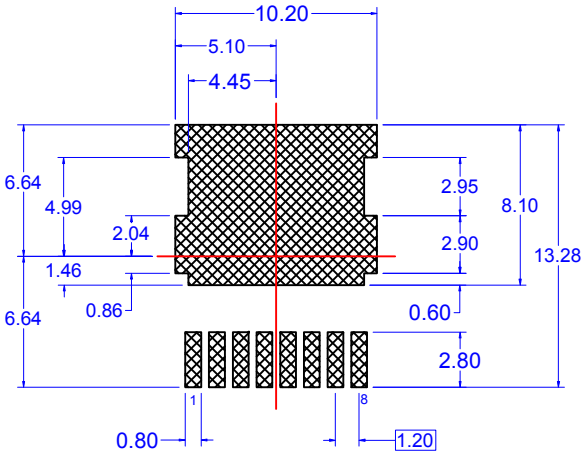




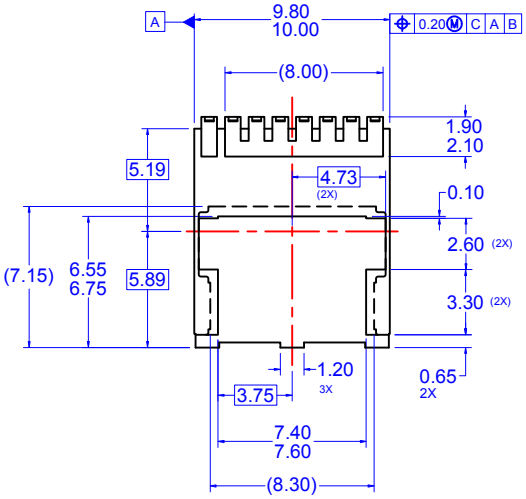
DETAIL "A"



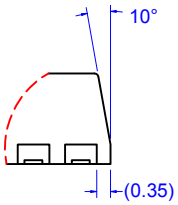
SIDE VIEW



LAND PATTERN
RECOMMENDATION



BOTTOM VIEW



DETAIL "B"

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A, DATED NOVEMBER 2009.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

E) DRAWING FILE NAME: MKT-PSOF08AREV3

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