FLEX 10KE

Embedded Programmable Logic Family

November 1998, ver. 1.01 — Data Sheet

Features...

Preliminary Information

- Embedded programmable logic device (PLD) family, providing system integration in a single device
  - Enhanced embedded array for implementing megafunctions such as efficient memory and specialized logic functions
  - Dual-port capability up to 16-bit width per embedded array block (EAB)
  - Logic array for general logic functions
- Replaces FLEX® 10KB family
- High density
  - 30,000 to 250,000 typical gates (see Tables 1 and 2)
  - Up to 98,304 RAM bits; 4,096 bits per EAB, all of which can be used without reducing logic capacity
- System-level features
  - MultiVolt™ I/O pins can drive or be driven by 2.5-V, 3.3-V, or 5.0-V devices
  - Low power consumption
  - Fully compliant with the peripheral component interconnect Special Interest Group's (PCI-SIG) ***PCI Local Bus Specification, Revision 2.1*** for 3.3-V operation
  - Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990, available without consuming device logic

Table 1. FLEX 10KE Features for EPF10K30E, EPF10K50E, EPF10K100β & EPF10K100E Devices

Feature	EPF10K30E	EPF10K50E	EPF10K100β	EPF10K100E
Typical gates (logic and RAM), *Note (1)*	30,000	50,000	100,000	100,000
Usable gates	22,000 to 119,000	36,000 to 199,000	62,000 to 158,000	62,000 to 257,000
Logic elements (LEs)	1,728	2,880	4,992	4,992
EABs	6	10	12	12
Total RAM bits	24,576	40,960	24,576	49,152
Maximum user I/O pins	220	254	191	338

Note:

(1) For designs that require IEEE Std. 1149.1 JTAG boundary-scan testing, the built-in JTAG circuitry contributes up to 31,250 additional gates.

Table 2 shows FLEX 10KE features for EPF10K130E, EPF10K200E, and EPF10K250E devices.

Table 2. FLEX 10KE Features for EPF10K130E, EPF10K200E & EPF10K250E Devices

Feature	EPF10K130E	EPF10K200E	EPF10K250E
Typical gates (logic and RAM), *Note (1)*	130,000	200,000	250,000
Usable gates	82,000 to 342,000	123,000 to 513,000	149,000 to 474,000
Logic elements (LEs)	6,656	9,984	12,160
EABs	16	24	20
Total RAM bits	65,536	98,304	81,920
Maximum user I/O pins	413	470	470

Note:

(1) For designs that require IEEE Std. 1149.1 JTAG boundary-scan testing, the built-in JTAG circuitry contributes up to 31,250 additional gates.

...and More Features

- Fabricated on advanced processes and operate with a 2.5-V internal supply voltage
- I/O circuits may be powered by 2.5-V or 3.3-V supply voltages
- In-circuit reconfigurability (ICR) via external Configuration EPROM, intelligent controller, or JTAG port
- ClockLock™ and ClockBoost™ options for reduced clock delay/skew and clock multiplication
- Built-in low-skew clock distribution trees
- 100% functional testing of all devices; test vectors or scan chains are not required
- Pull-up on I/O pins before and during configuration
- Supports hot-socketing operation

■ Flexible interconnect
- FastTrack Interconnect™ continuous routing structure for fast, predictable interconnect delays
- Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
- Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
- Tri-state emulation that implements internal tri-state buses
- Up to six global clock signals and four global clear signals

■ Powerful I/O pins
- Individual tri-state output enable control for each pin
- Open-drain option on each I/O pin
- Programmable output slew-rate control to reduce switching noise
- Clamp to V_{CC} user-selectable pin-by-pin

■ Peripheral register for fast setup and clock-to-output delay

- Software design support and automatic place-and-route provided by the Altera MAX+PLUS® II development system for 486- and Pentium-based PCs, Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Flexible package options
  - Available in a variety of packages with 144 to 672 pins, including the innovative FineLine BGA™ packages (see Tables 3 and 4)
  - SameFrame™ pin-compatibility (with other FLEX 10KE devices) across device densities and pin counts
- Additional design entry and simulation support provided by electronic design interchange format (EDIF) 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular electronic design automation (EDA) tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

Table 3. FLEX 10KE Package Options & I/O Pin Count *Notes (1), (2), (3)*

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
EPF10K30E	102	147		176		220			
EPF10K50E	102	147	189	191		254			
EPF10K100B		147	189	191					
EPF10K100E		147	189	191	274	338			
EPF10K130E			186			369			413
EPF10K200E							470	470	470
EPF10K250E							470	470	470

Notes:

(1) Contact Altera Customer Marketing for up-to-date information on package availability.

(2) FLEX 10KE device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), pin-grid array (PGA), and ball-grid array (BGA).

(3) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices. MAX+PLUS II software versions 9.1 and higher provide features to help use only the common pins.

Table 4. FLEX 10KE Package Sizes

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
Pitch (mm)	0.50	0.50	0.50	1.0	1.27	1.0	–	1.27	1.0
Area (mm^2)	484	936	1,197	289	1,225	529	3,904	2,025	729

General Description

Altera FLEX 10KE devices are an enhancement of the FLEX 10K device family. Based on reconfigurable CMOS SRAM elements, the Flexible Logic Element MatriX (FLEX) architecture incorporates all features necessary to implement common gate array megafunctions. With up to 250,000 gates, the FLEX 10KE family provides the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

FLEX 10KE devices are configurable, and they are 100% tested prior to shipment. As a result, the designer is not required to generate test vectors for fault coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different gate array designs; FLEX 10KE devices can be configured on the board for the specific functionality required.

Table 5 shows FLEX 10KE performance for some common designs. All performance values shown were obtained with Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Table 5. FLEX 10KE Performance

Application	Resources Used		Performance			Units
	LEs	EABs	-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	
16-bit loadable counter	16	0	196	182	143	MHz
16-bit accumulator	16	0	196	182	143	MHz
16-to-1 multiplexer, *Note (1)*	10	0	15	17	18	ns
16-bit multiplier with 3 stage pipeline, *Note (2)*	10	0	91	86	70	MHz
256 × 16 RAM read cycle speed, *Note (2)*	0	1	181	142	125	MHz
256 × 16 RAM write cycle speed, *Note (2)*	0	1	135	117	106	MHz

Notes:
(1) This application uses combinatorial inputs and outputs.
(2) This application uses registered inputs and outputs.

Table 6 shows FLEX 10KE performance for more complex designs. These designs are available as Altera MegaCore™ functions.

Table 6. FLEX 10KE Performance for Complex Designs

Application	LEs Used	Performance			Units
		-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	
16-bit, 8-tap parallel finite impulse response (FIR) filter	592	138	128	103	MSPS
8-bit, 512-point fast Fourier transform (FFT) function	1,845	60	72	83	µs
		76	66	56	MHz
a16450 universal asynchronous receiver/transmitter (UART)	479	42	39	34	MHz

The FLEX 10KE architecture is similar to that of embedded gate arrays, which is the fastest-growing segment of the gate array market. As with standard gate arrays, embedded gate arrays implement general logic in a conventional "sea-of-gates" architecture. Additionally, embedded gate arrays have dedicated die areas for implementing large, specialized functions. By embedding functions in silicon, embedded gate arrays provide reduced die area and increased speed compared to standard gate arrays. While embedded megafunctions typically cannot be customized, FLEX 10KE devices are programmable, providing the designer with full control over embedded megafunctions and general logic while facilitating iterative design changes during debugging.

Each FLEX 10KE device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), microcontroller, wide-data-path manipulation, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array: it is used to implement general logic, such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

FLEX 10KE devices are configured at system power-up with data stored in an Altera serial Configuration EPROM device or provided by a system controller. Altera offers the EPC1, EPC2, and EPC1441 Configuration EPROMs, which configure FLEX 10KE devices via a serial data stream. Configuration data can also be downloaded from system RAM or from the Altera BitBlaster™ serial download cable, ByteBlaster™ parallel port download cable, or ByteBlasterMV™ parallel port download cable. After a FLEX 10KE device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 330 ms, real-time changes can be made during system operation.

FLEX 10KE devices contain an optimized interface that permits microprocessors to configure FLEX 10KE devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat a FLEX 10KE device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to reconfigure the device.

For more information, go to the following documents:

- *Configuration EPROMs for FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlaster Parallel Port Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*

FLEX 10KE devices are supported by the Altera MAX+PLUS II development system, a single, integrated package that offers schematic, text—including AHDL—and waveform design entry; compilation and logic synthesis; full simulation and worst-case timing analysis; and device configuration. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The MAX+PLUS II software works easily with common gate array EDA tools for synthesis and simulation. For example, the MAX+PLUS II software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the MAX+PLUS II software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the MAX+PLUS II development system includes DesignWare functions that are optimized for the FLEX 10KE architecture.

The MAX+PLUS II software runs on 486- and Pentium-based PCs, Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.

Go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in the ***1998 Data Book*** for more information.

Functional Description

Each FLEX 10KE device contains an enhanced embedded array to implement memory and specialized logic functions, and a logic array to implement general logic.

The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 4,096 bits, which can be used to create RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions, such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

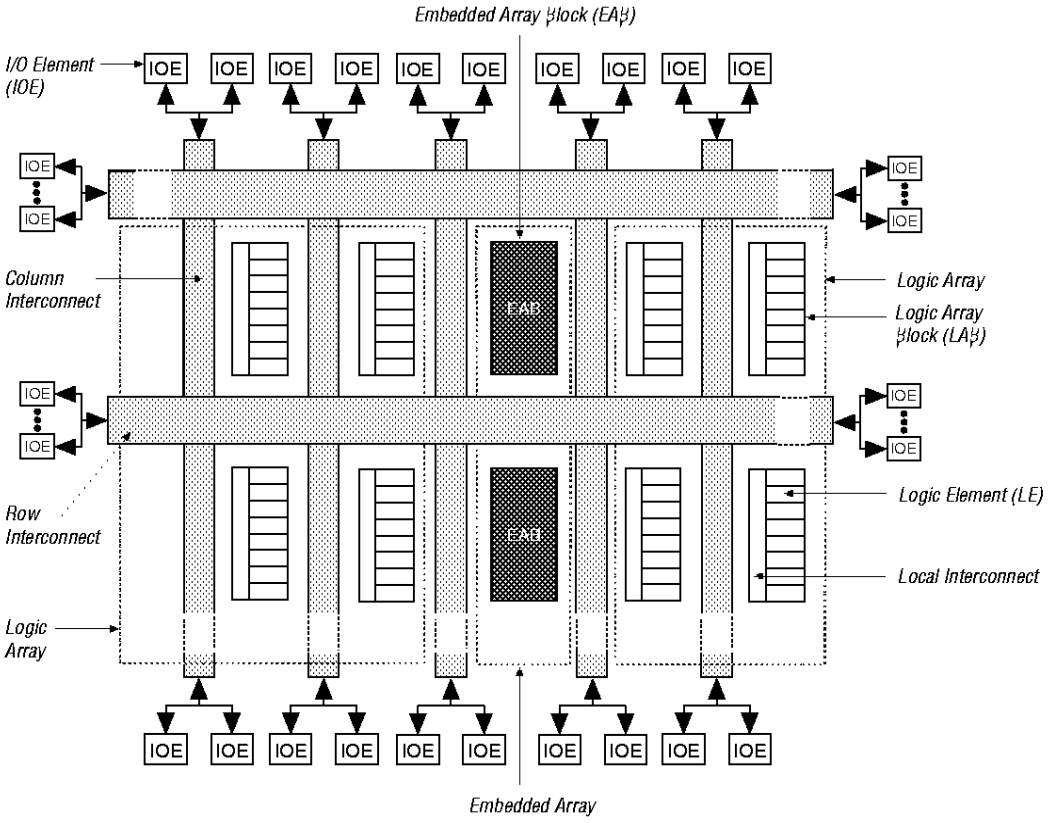
The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a 4-input look-up table (LUT), a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—such as 8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable gates of logic.

Signal interconnections within FLEX 10KE devices (as well as to and from device pins) are provided by the FastTrack Interconnect routing structure, a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect routing structure. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times as low as 2.9 ns and hold times of 0 ns; as outputs, these registers provide clock-to-output times as low as 4.3 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, tri-state buffers, and open-drain outputs.

Figure 1 shows a block diagram of the FLEX 10KE architecture. Each group of LEs is combined into an LAB; LABs are arranged into rows and columns. Each row also contains a single EAB. The LABs and EABs are interconnected by the FastTrack Interconnect routing structure. IOEs are located at the end of each row and column of the FastTrack Interconnect routing structure.

Figure 1. FLEX 10KE Device Block Diagram



FLEX 10KE devices provide six dedicated inputs that drive the control inputs of the flipflops to ensure the efficient distribution of high-speed, low-skew (less than 1.5 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect routing structure. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

Embedded Array Block

The EAB is a flexible block of RAM with registers on the input and output ports, and is used to implement common gate array megafunctions. Because it is large and flexible, the EAB is suitable for functions such as multipliers, vector scalars, and error correction circuits. These functions can be combined in applications such as digital filters and microcontrollers.

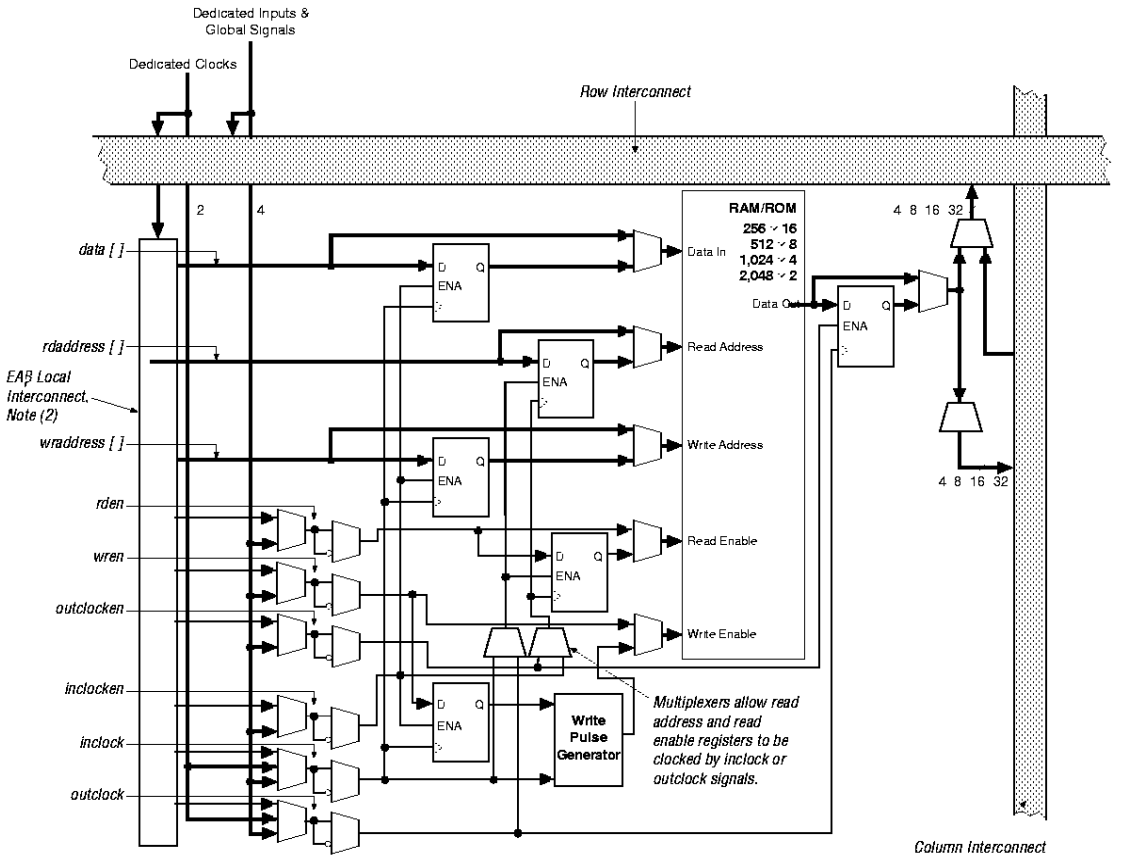
Logic functions are implemented by programming the EAB with a read-only pattern during configuration, thereby creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of EABs. The large capacity of EABs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or field-programmable gate array (FPGA) RAM blocks. For example, a single EAB can implement a 5×4 multiplier or any function with nine inputs and nine outputs. Parameterized functions such as LPM functions can take advantage of the EAB automatically.

The FLEX 10KE EAB provides advantages over FPGAs which implement on-board RAM as arrays of small, distributed RAM blocks. These small FPGA RAM blocks must be connected together to make usably-sized RAM blocks. The RAM blocks are connected together using multiplexers implemented with more logic blocks. These extra multiplexers cause extra delay, which slows down the RAM block. FPGA RAM blocks are also prone to routing problems because small blocks of RAM must be connected together to make larger blocks. In contrast, EABs can be used to implement large, dedicated blocks of RAM that eliminate these timing and routing concerns.

The FLEX 10KE enhanced EAB adds dual-port capability to the existing EAB structure. The dual-port structure is ideal for FIFO buffers with one or two clocks. The FLEX 10KE EAB can also support up to 16-bit-wide RAM blocks and is backward-compatible with any design containing FLEX 10K EABs. The FLEX 10KE EAB can act in dual-port or single-port mode. When in dual-port mode, separate clocks may be used for EAB read and write sections, which allows the EAB to be written and read at different rates. It also has separate synchronous clock enable signals for the EAB read and write sections, which allow independent control of these sections.

Alternatively, one clock and clock enable can be used to control the input registers of the EAB, while a different clock and clock enable control the output registers (see Figure 2).

Figure 2. FLEX 10KE Device in Dual-Port RAM Mode *Notes (1), (3)*

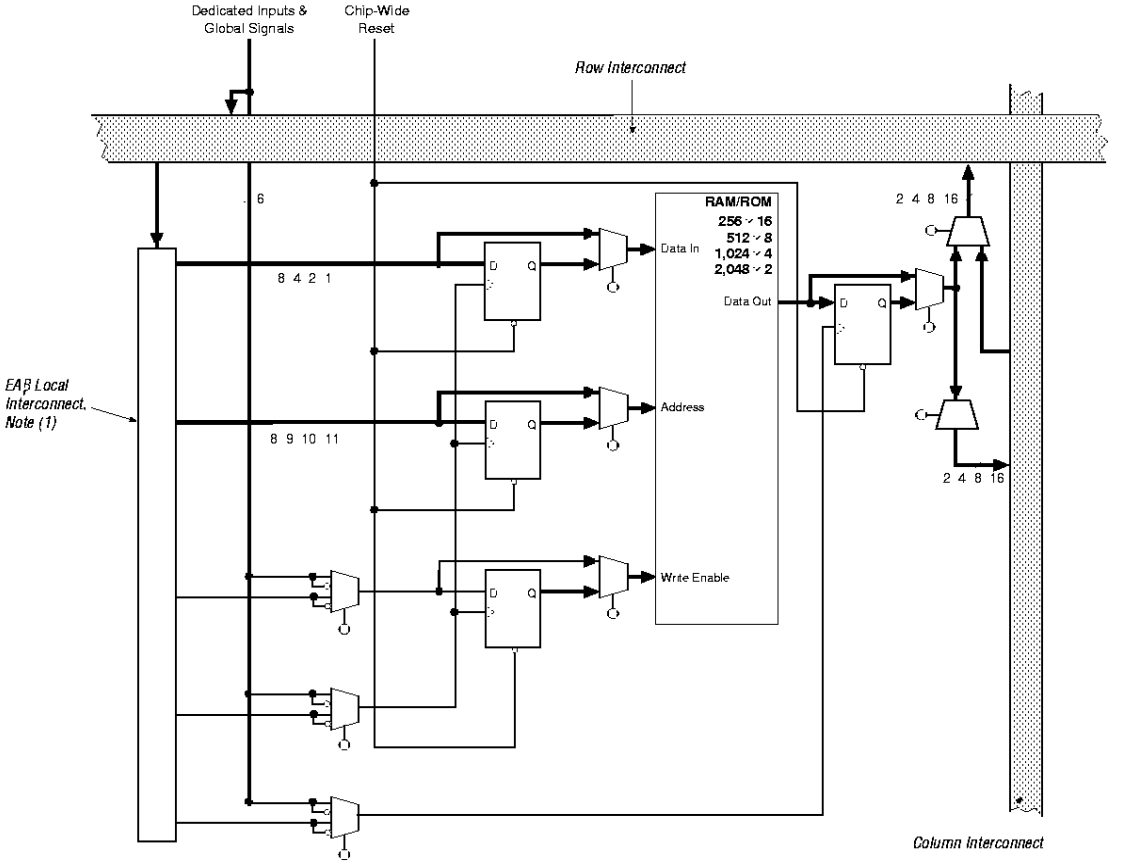


Notes:

(1) All registers can be asynchronously cleared by EAB local interconnect signals, global signals, or the chip-wide reset.
(2) EPF10K30E and EPF10K50E devices have 88 EAB local interconnect channels. EPF10K100E, EPF10K130E, EPF10K200E, and EPF10K250E devices have 104 EAB local interconnect channels.
(3) The EPF10K100B device does not offer dual-port RAM mode.

The FLEX 10KE EAB can be used in a single-port mode, which is useful for backward-compatibility with FLEX 10K designs (see Figure 3).

Figure 3. FLEX 10KE Device in Single-Port EAB



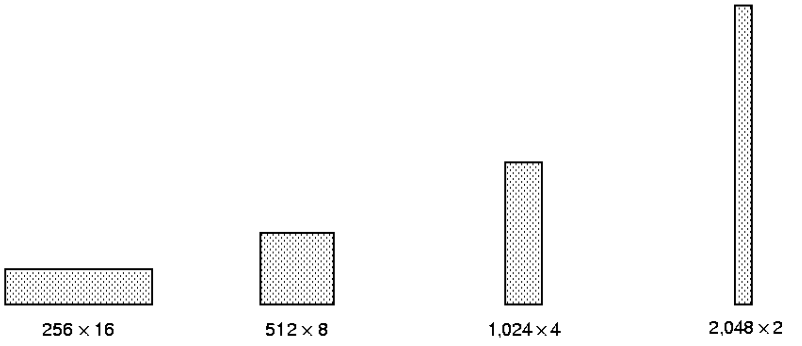
Note:

(1) EPF10K30E and EPF10K50E devices have 88 EAB local interconnect channels. EPF10K100E, EPF10K100B, EPF10K130E, EPF10K200E, and EPF10K250E devices have 104 EAB local interconnect channels.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the EAB's synchronous RAM generates its own WE signal and is self-timed with respect to the input or write clock. A circuit using the EAB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

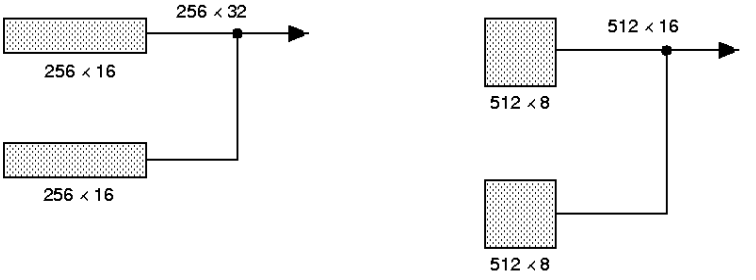
When used as RAM, each EAB can be configured in any of the following sizes: 256 × 16, 512 × 8, 1,024 × 4, or 2,048 × 2 (see Figure 4).

Figure 4. FLEX 10KE EAβ Memory Configurations



Larger blocks of RAM are created by combining multiple EABs. For example, two 256 × 16 RAM blocks can be combined to form a 256 × 32 block; two 512 × 8 RAM blocks can be combined to form a 512 × 16 block (see Figure 5).

Figure 5. Examples of Combining FLEX 10KE EABs



If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. The Altera MAX+PLUS II software automatically combines EABs to meet a designer's RAM specifications.

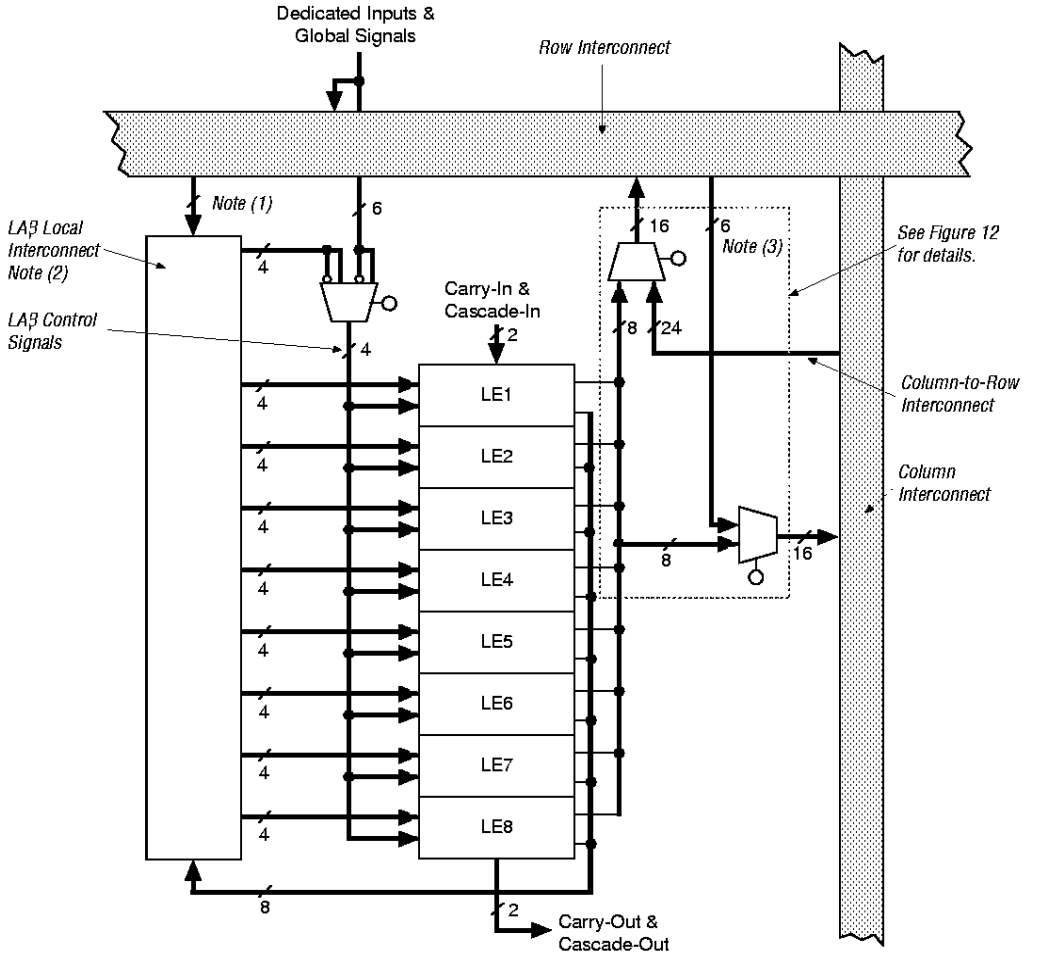
EABs provide flexible options for driving and controlling clock signals. Different clocks and clock enables can be used for reading and writing to the EAB. Registers can be independently inserted on the data input, EAB output, write address, WE signals, read address, and RE signals. The global signals and the EAB local interconnect can drive WE, RE, and clock enable signals. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control WE, RE, clear, clock, and clock enable signals.

An EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs (see Figures 2 and 3). The column interconnect, which is adjacent to the EAB, has twice as many channels as other columns in the device.

Logic Array Block

A LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10KE architecture, facilitating efficient routing with optimum device utilization and high performance (see Figure 6).

Figure 6. FLEX 10KE LAβ



Notes:

(1) EPF10K30E and EPF10K50E devices have 22 inputs to the LAB local interconnect channel from the row; EPF10K100E, EPF10K100B, EPF10K130E, EPF10K200E, and EPF10K250E devices have 26.

(2) EPF10K30E and EPF10K50E devices have 30 LAB local interconnect channels; EPF10K100E, EPF10K100B, EPF10K130E, EPF10K200E, and EPF10K250E devices have 34.

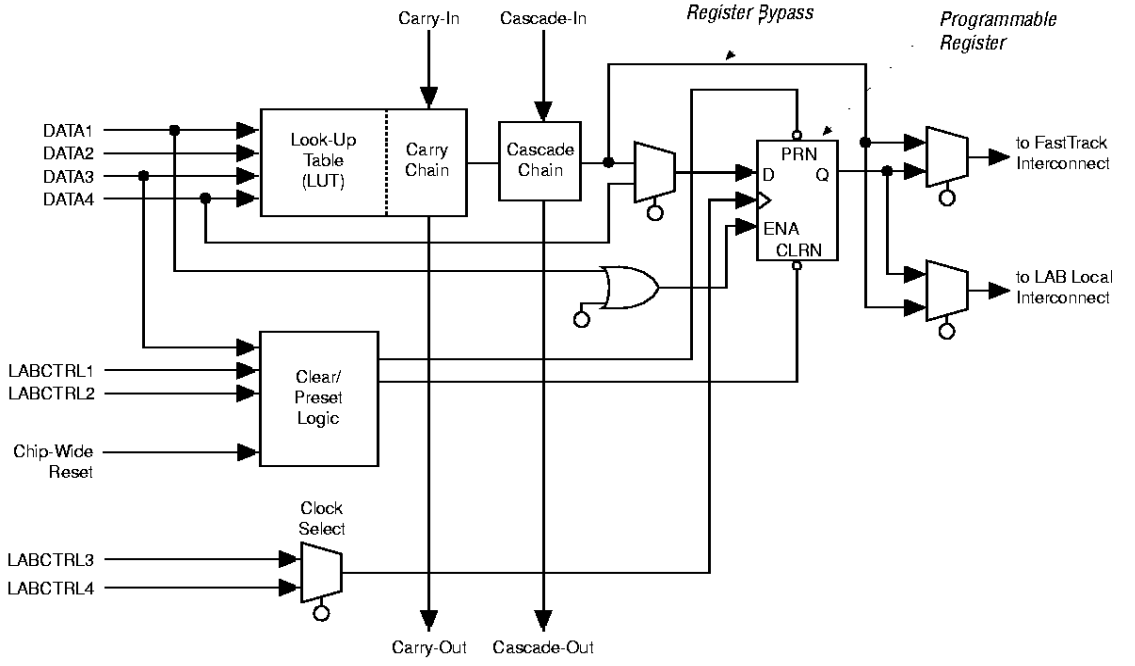
(3) In EPF10K100B devices, four row channels can drive column channels at each intersection.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks; the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

Logic Element

The LE, the smallest unit of logic in the FLEX 10KE architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous clock enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect routing structure (see Figure 7).

Figure 7. FLEX 10KE Logic Element



The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the flipflop is bypassed and the output of the LUT drives the output of the LE.

The LE has two outputs that drive the interconnect; one drives the local interconnect and the other drives either the row or column FastTrack Interconnect routing structure. The two outputs can be controlled independently; for example, the LUT can drive one output while the register drives the other output. This feature, called register packing, can improve LE utilization because the register and the LUT can be used for unrelated functions.

The FLEX 10KE architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in a LAB and all LABs in the same row. Intensive use of carry and cascade chains can reduce routing flexibility. Therefore, the use of these chains should be limited to speed-critical portions of a design.

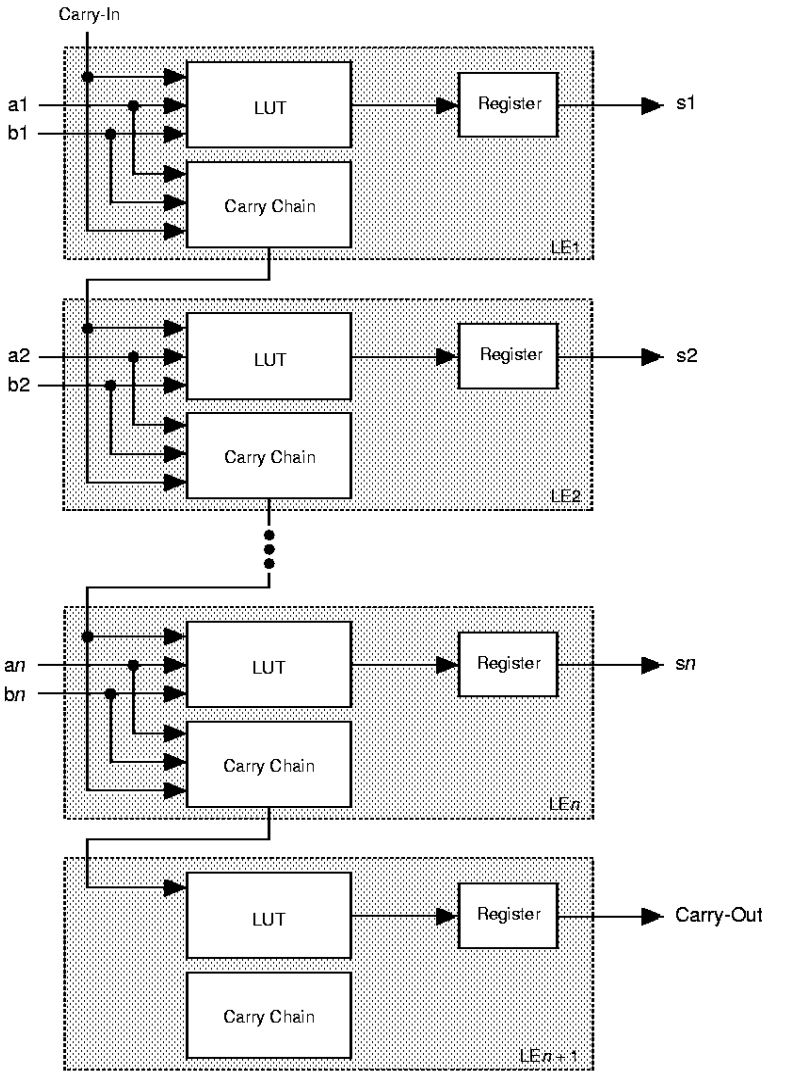
Carry Chain

The carry chain provides a very fast (as low as 0.2 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 10KE architecture to implement high-speed counters, adders, and comparators of arbitrary width efficiently. Carry chain logic can be created automatically by the MAX+PLUS II Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of carry chains.

Carry chains longer than eight LEs are automatically implemented by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB. For example, the last LE of the first LAB in a row carries to the first LE of the third LAB in the row. The carry chain does not cross the EAB at the middle of the row. For instance, in the EPF10K50E device, the carry chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB.

Figure 8 shows how an n-bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

Figure 8. FLEX 10KE Carry Chain Operation (N-bit Full Adder)



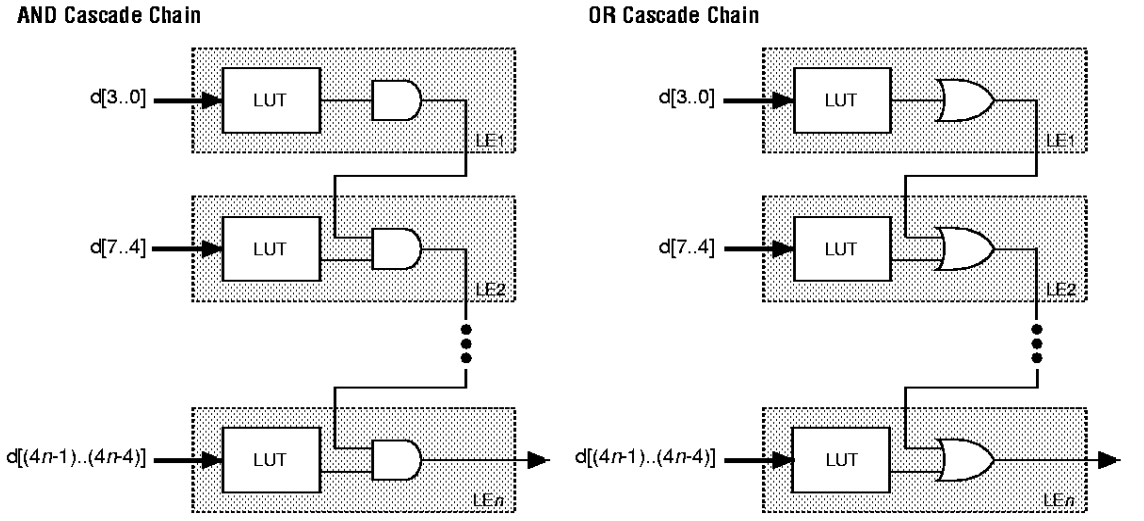
Cascade Chain

With the cascade chain, the FLEX 10KE architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. With a delay as low as 0.6 ns per LE, each additional LE provides four more inputs to the effective width of a function. Cascade chain logic can be created automatically by the MAX+PLUS II Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than eight bits are automatically implemented by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB (e.g., the last LE of the first LAB in a row cascades to the first LE of the third LAB). The cascade chain does not cross the center of the row (e.g., in the EPF10K50E device, the cascade chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB). This break is due to the EAB's placement in the middle of the row.

Figure 9 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of $4n$ variables implemented with n LEs. The LE delay is 1.3 ns; the cascade chain delay is 0.6 ns. With the cascade chain, approximately 3.1 ns are needed to decode a 16-bit address.

Figure 9. FLEX 10KE Cascade Chain Operation



LE Operating Modes

The FLEX 10KE LE can operate in the following four modes:

- Normal mode
- Arithmetic mode
- Up/down counter mode
- Clearable counter mode

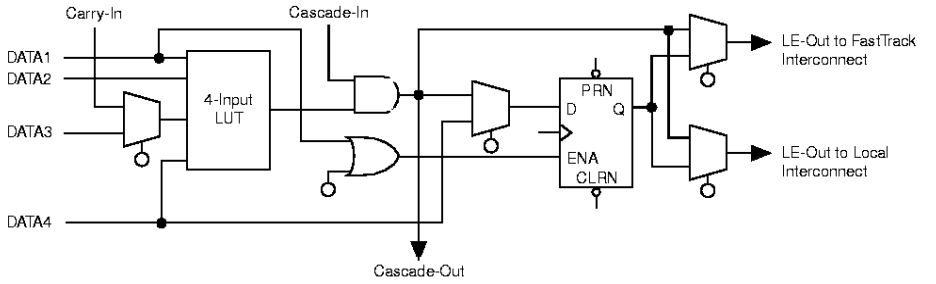
Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. Three inputs to the LE provide clock, clear, and preset control for the register. The MAX+PLUS II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions to use an LE operating mode for optimal performance.

The architecture provides a synchronous clock enable to the register in all four modes. The MAX+PLUS II software can set `DATA1` to enable the register synchronously, providing easy implementation of fully synchronous designs.

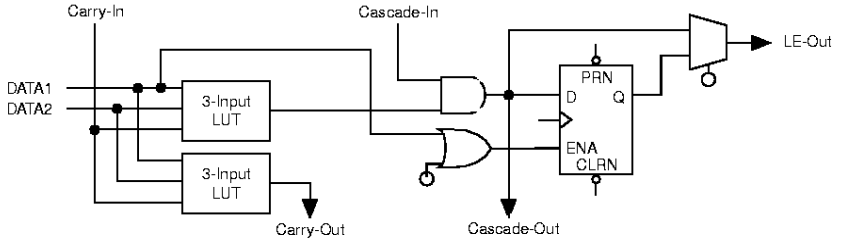
Figure 10 shows the LE operating modes.

Figure 10. FLEX 10KE LE Operating Modes

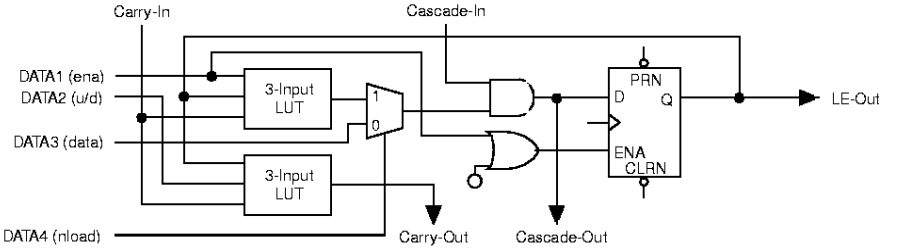
Normal Mode



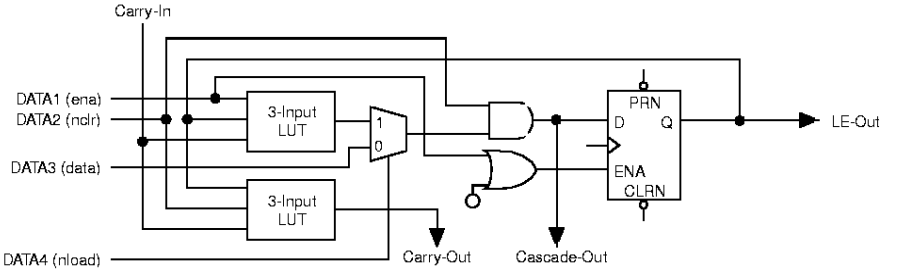
Arithmetic Mode



Up/Down Counter Mode



Clearable Counter Mode



Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a 4-input LUT. The MAX+PLUS II Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect routing structure at the same time.

The LUT and the register in the LE can be used independently; this feature is known as register packing. To support register packing, the LE has two outputs; one drives the local interconnect, and the other drives the FastTrack Interconnect routing structure. The DATA4 signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a 3-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a 4-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear, and preset signals in the LE. In a packed LE, the register can drive the FastTrack Interconnect routing structure while the LUT drives the local interconnect, or vice versa.

Arithmetic Mode

The arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a 3-input function; the other generates a carry output. As shown in Figure 10 on page 20, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: a, b, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

Up/Down Counter Mode

The up/down counter mode offers counter enable, clock enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals, without using the LUT resources.

Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but supports a synchronous clear instead of the up/down control. The clear function is substituted for the cascade-in signal in the up/down counter mode. Two 3-input LUTs are used: one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer. The output of this multiplexer is AND ed with a synchronous clear signal.

Internal Tri-State Emulation

Internal tri-state emulation provides internal tri-stating without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The MAX+PLUS II software automatically implements tri-state bus functionality with a multiplexer.

Clear & Preset Logic Control

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE asynchronously loads signals into a register. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear. Alternatively, the register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

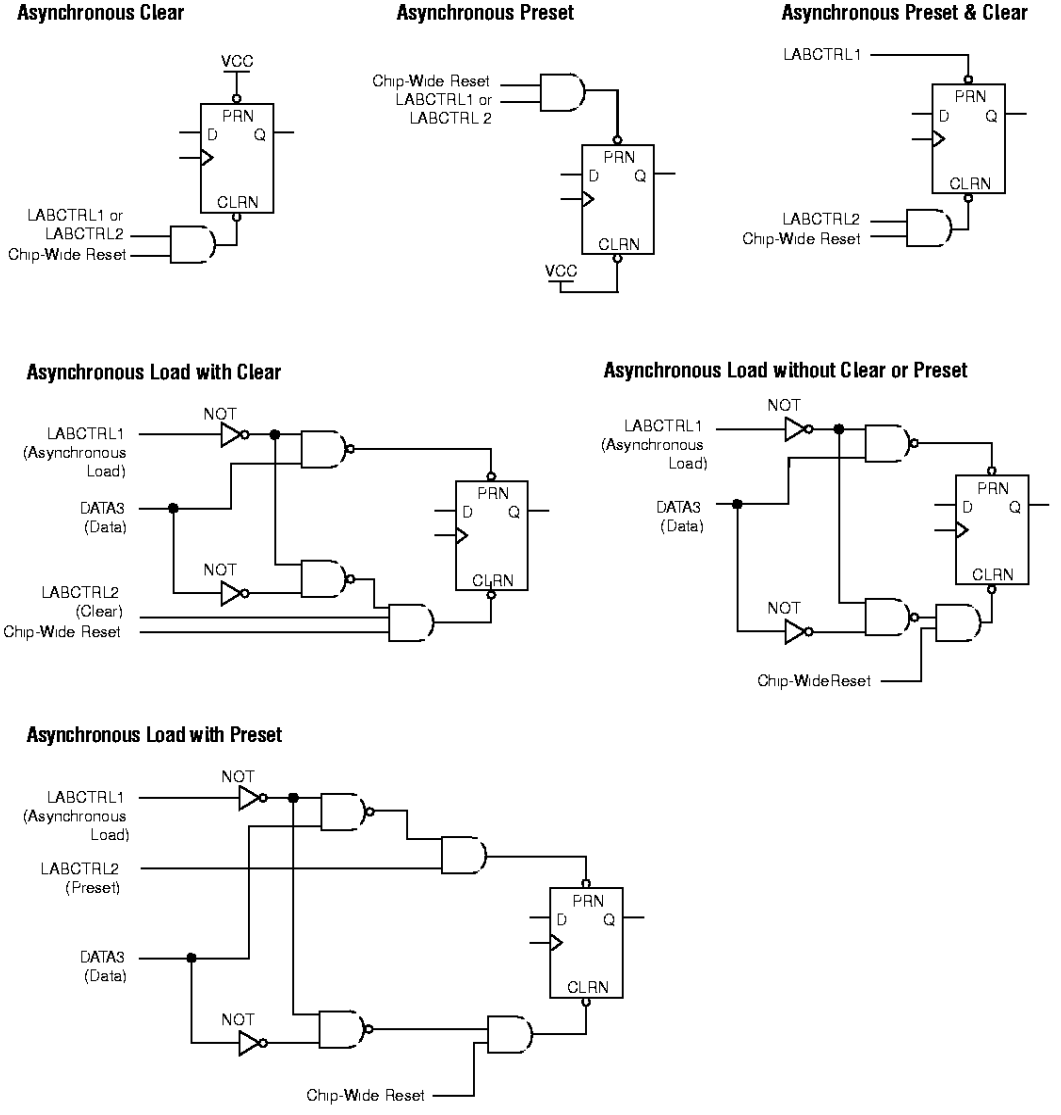
During compilation, the MAX+PLUS II Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

In addition to the six clear and preset modes, FLEX 10KE devices provide a chip-wide reset pin that can reset all registers in the device. Use of this feature is set during design entry. In any of the clear and preset modes, the chip-wide reset overrides all other signals. Registers with asynchronous presets may be preset when the chip-wide reset is asserted. Inversion can be used to implement the asynchronous preset. Figure 11 shows examples of how to enter a design for the desired functionality.

Figure 11. FLEX 10KE LE Clear & Preset Modes



Asynchronous Clear

The flipflop can be cleared by either LABCTRL1 or LABCTRL2. In this mode, the preset signal is tied to VCC to deactivate it.

Asynchronous Preset

An asynchronous preset is implemented as an asynchronous load, or with an asynchronous clear. If DATA3 is tied to VCC, asserting LABCTRL1 asynchronously loads a one into the register. Alternatively, the MAX+PLUS II software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

Asynchronous Preset & Clear

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. DATA3 is tied to VCC, so that asserting LABCTRL1 asynchronously loads a one into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

Asynchronous Load with Clear

When implementing an asynchronous load in conjunction with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear; LABCTRL2 does not have to feed the preset circuits.

Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with preset, the MAX+PLUS II software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 presets the register, while asserting LABCTRL1 loads the register. The MAX+PLUS II software inverts the signal that drives DATA3 to account for the inversion of the register's output.

Asynchronous Load without Preset or Clear

When implementing an asynchronous load without preset or clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

FastTrack Interconnect Routing Structure

In the FLEX 10KE architecture, connections between LEs, EABs, and device I/O pins are provided by the FastTrack Interconnect routing structure, which is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

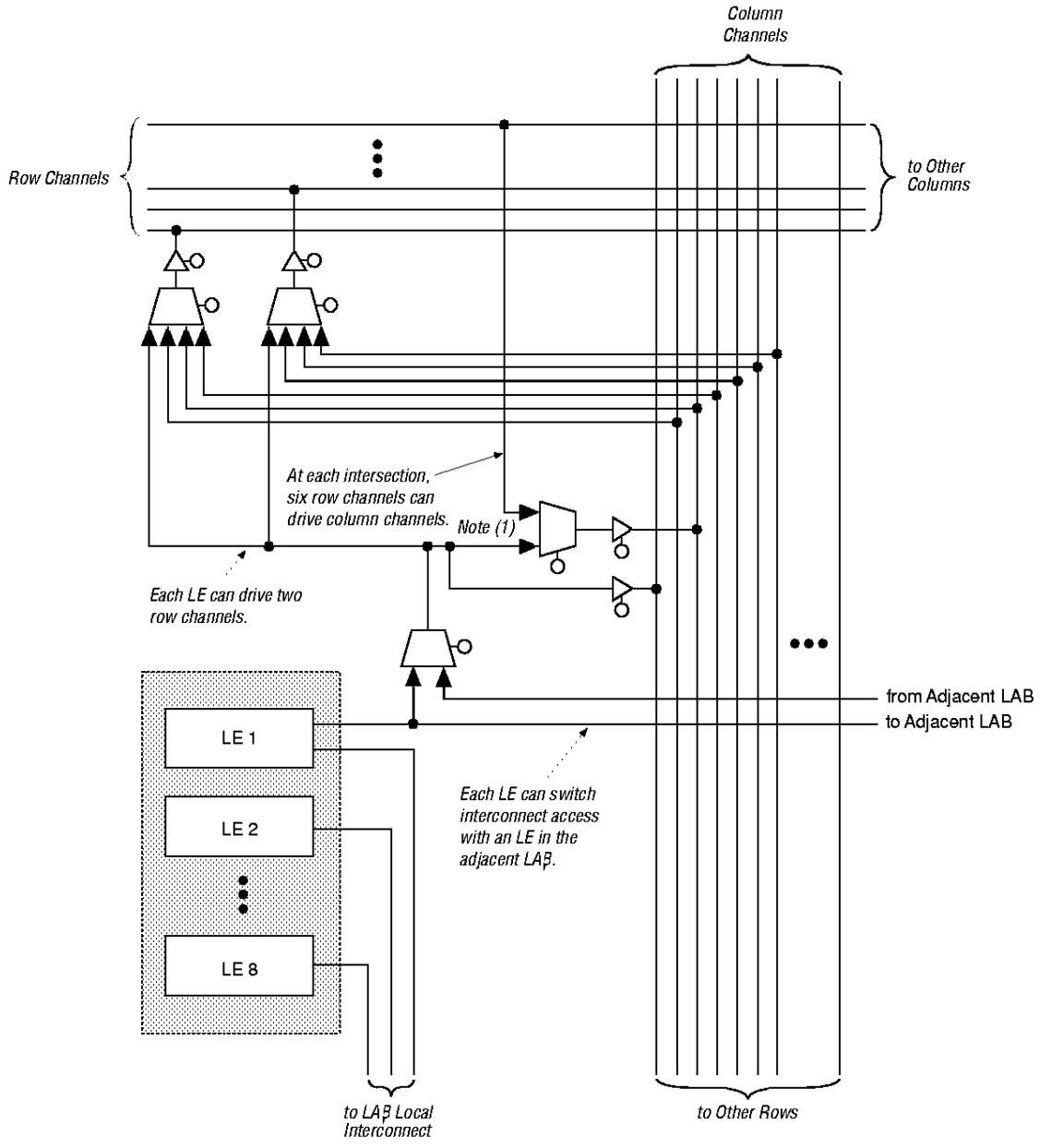
The FastTrack Interconnect routing structure consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the row. The column interconnect routes signals between rows and can drive I/O pins.

Row channels drive into the LAB or EAB local interconnect. The row signal is buffered at every LAB or EAB to reduce the effect of fan-out on delay. A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in a LAB drive the row interconnect.

Each column of LABs or EABs is served by a dedicated column interconnect. The column interconnect that serves the EABs has twice as many channels as other column interconnects. The column interconnect can then drive I/O pins or another row's interconnect to route the signals to other LABs or EABs in the device. A signal from the column interconnect, which can be either the output of a LE or an input from an I/O pin, must be routed to the row interconnect before it can enter a LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, a LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This routing flexibility enables routing resources to be used more efficiently (see Figure 12).

Figure 12. FLEX 10KE LAβ Connections to Row & Column Interconnect



Note:
(1) In EPF10K100B devices, four row channels can drive column channels at each intersection.

For improved routing, the row interconnect consists of a combination of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. The EAB can be driven by the half-length channels in the left half of the row and by the full-length channels. The EAB drives out to the full-length channels. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-row channel, thereby saving the other half of the channel for the other half of the row.

Table 7 summarizes the FastTrack Interconnect routing structure resources available in each FLEX 10KE device.

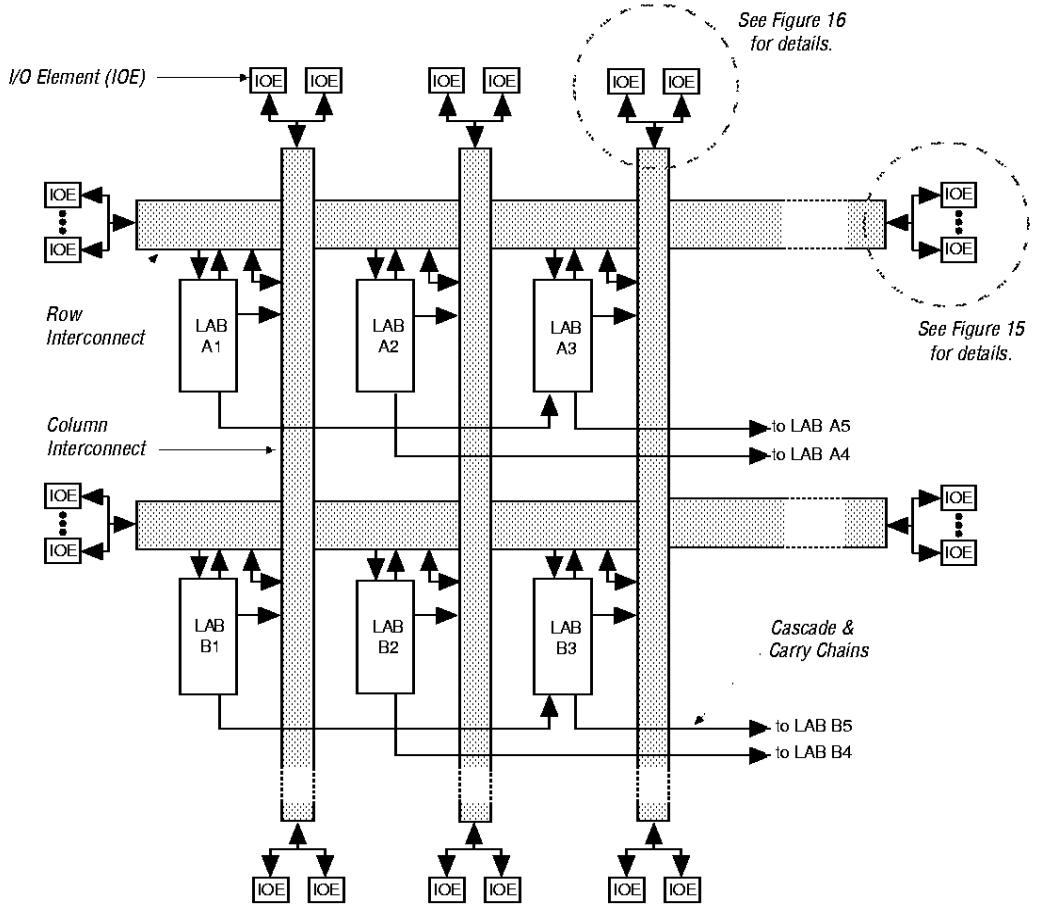
Table 7. FLEX 10KE FastTrack Interconnect Resources

Device	Rows	Channels per Row	Columns	Channels per Column
EPF10K30E	6	216	36	24
EPF10K50E	10	216	36	24
EPF10K100B EPF10K100E	12	312	52	24
EPF10K130E	16	312	52	32
EPF10K200E	24	312	52	48
EPF10K250E	20	456	76	40

In addition to general-purpose I/O pins, FLEX 10KE devices have six dedicated input pins that provide low-skew signal distribution across the device. These six inputs can be used for global clock, clear, preset, and peripheral output enable and clock enable control signals. These signals are available as control signals for all LABs and IOEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Figure 13 shows the interconnection of adjacent LABs and EABs, with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number represents the column. For example, LAB B3 is in row B, column 3.

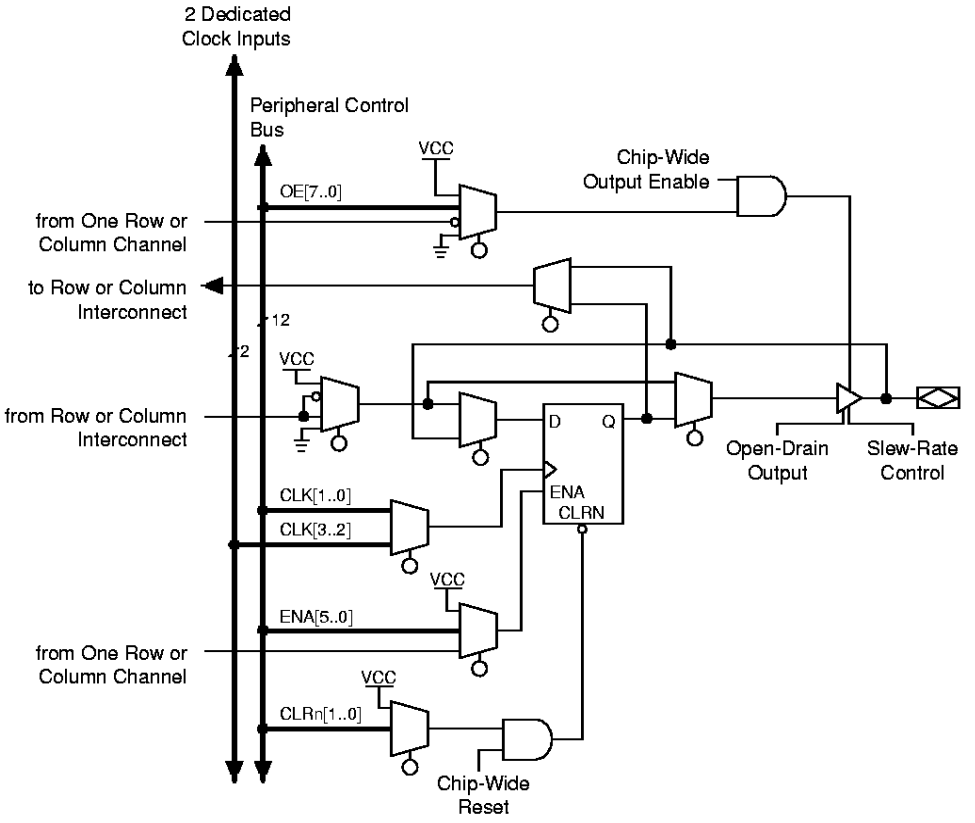
Figure 13. FLEX 10KE Interconnect Resources



I/O Element

An IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. In some cases, using an LE register for an input register will result in a faster setup time than using an IOE register. IOEs can be used as input, output, or bidirectional pins. The MAX+PLUS II Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Figure 14 shows the IOE block diagram.

Figure 14. FLEX 10KE I/O Element



Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across devices; it provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, a LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal resets all IOE registers, overriding any other control signals.

When a dedicated clock pin drives IOE registers, it can be inverted for all IOEs in the device. All IOEs must use the same sense of the clock. For example, if any IOE uses the inverted clock, all IOEs must use the inverted clock and no IOE can use the non-inverted clock. However, LEs can still use the true or complement of the clock on a LAB-by-LAB basis.

The incoming signal may be inverted at the dedicated clock pin and will drive all IOEs. To use the true and complement of a clock to drive IOEs, drive it into both global clock pins. One global clock pin will supply the true, and the other will supply the complement.

When the true and complement of a dedicated input drives IOE clocks, then two signals on the peripheral control bus are consumed, one for each sense of the clock.

When dedicated inputs drive non-inverted and inverted peripheral clears, clock enables, and output enables, two signals on the peripheral control bus will be used.

Tables 8 and 9 list the sources for each peripheral control signal, and show how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals. The tables also show the rows that can drive global signals.

Table 8. EPF10K30E & EPF10K50E Peripheral Bus Sources

Peripheral Control Signal	EPF10K30E	EPF10K50E
OE0	Row A	Row A
OE1	Row B	Row B
OE2	Row C	Row D
OE3	Row D	Row F
OE4	Row E	Row H
OE5	Row F	Row J
CLKENA0/CLK0/GLOBAL0	Row A	Row A
CLKENA1/OE6/GLOBAL1	Row B	Row C
CLKENA2/CLR0	Row C	Row E
CLKENA3/OE7/GLOBAL2	Row D	Row G
CLKENA4/CLR1	Row E	Row I
CLKENA5/CLK1/GLOBAL3	Row F	Row J

Table 9. EPF10K100β, EPF10K100E, EPF10K130E, EPF10K200E & EPF10K250E Peripheral βus Sources

Peripheral Control Signal	EPF10K100β EPF10K100E	EPF10K130E	EPF10K200E	EPF10K250E
OE0	Row A	Row C	Row G	Row E
OE1	Row C	Row E	Row I	Row G
OE2	Row E	Row G	Row K	Row I
OE3	Row L	Row N	Row R	Row P
OE4	Row I	Row K	Row O	Row M
OE5	Row K	Row M	Row Q	Row O
CLKENA0/CLK0/GLOBAL0	Row F	Row H	Row L	Row J
CLKENA1/OE6/GLOBAL1	Row D	Row F	Row J	Row H
CLKENA2/CLR0	Row B	Row D	Row H	Row F
CLKENA3/OE7/GLOBAL2	Row H	Row J	Row N	Row L
CLKENA4/CLR1	Row J	Row L	Row P	Row N
CLKENA5/CLK1/GLOBAL3	Row G	Row I	Row M	Row K

Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3 in Tables 8 and 9. An internally generated signal can drive a global signal, providing the same low-skew, low-delay characteristics as a signal driven by an input pin. An LE drives the global signal by driving a row line that drives the peripheral bus, which then drives the global signal. This feature is ideal for internally generated clear or clock signals with high fan-out. However, internally driven global signals offer no advantage over the general-purpose interconnect for routing data signals.

The chip-wide output enable pin is an active-low pin that can be used to tri-state all pins on the device. This option can be set in the MAX+PLUS II software. The registers in the IOE can also be reset by the chip-wide reset pin.

Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel (see Figure 15).

Figure 15. FLEX 10KE Row-to-IOE Connections

The values for m and n are provided in Table 10.

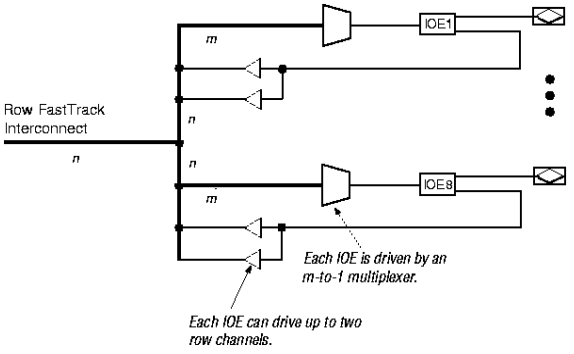


Table 10 lists the FLEX 10KE row-to-IOE interconnect resources.

Table 10. FLEX 10KE Row-to-IOE Interconnect Resources

Device	Channels per Row *(n)*	Row Channels per Pin *(m)*
EPF10K30E	216	27
EPF10K50E	216	27
EPF10K100B EPF10K100E	312	39
EPF10K130E	312	39
EPF10K200E	312	39
EPF10K250E	456	57

Column-to-IOE Connections

When an IOE is used as an input, it can drive up to two separate column channels. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the column channels. Two IOEs connect to each side of the column channels. Each IOE can be driven by column channels via a multiplexer. The set of column channels is different for each IOE (see Figure 16).

Figure 16. FLEX 10KE Column-to-IOE Connections

The values for m and n are provided in Table 11.

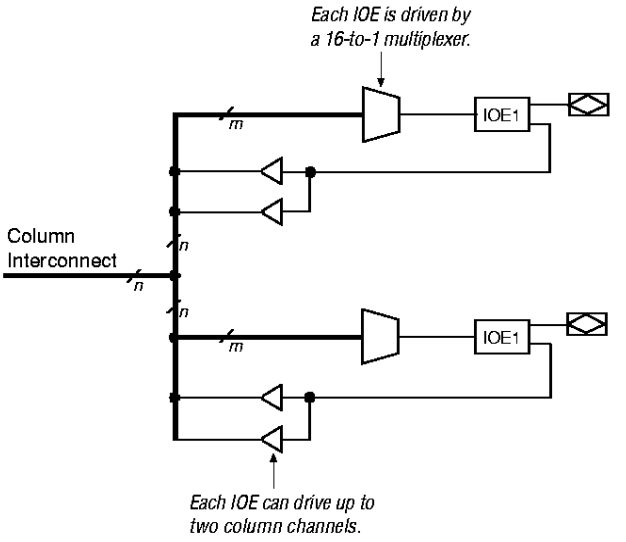


Table 11 lists the FLEX 10KE column-to-IOE interconnect resources.

Table 11. FLEX 10KE Column-to-IOE Interconnect Resources

Device	Channels per Column *(n)*	Column Channels per Pin *(m)*
EPF10K30E	24	16
EPF10K50E	24	16
EPF10K100B EPF10K100E	24	16
EPF10K130E	32	24
EPF10K200E	48	40
EPF10K250E	40	32

ClockLock & ClockBoost Features

To support high-speed designs, FLEX 10KE devices offer optional ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) that is used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by resource sharing within the device. ClockBoost allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

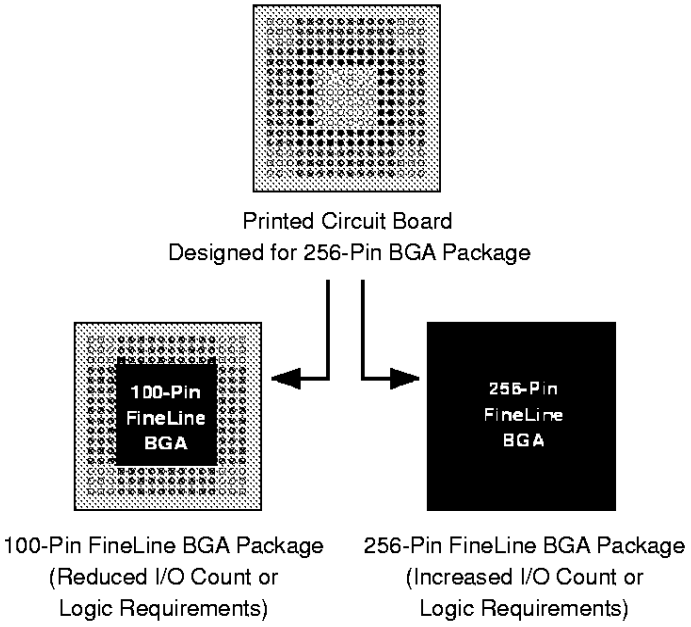
The ClockLock and ClockBoost features in FLEX 10KE devices are enabled through the MAX+PLUS II software. External devices are not required to use these features.

SameFrame Pin-Outs

FLEX 10KE devices support the SameFrame pin-out feature for FineLine BGA packages. SameFrame pin-out is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support anything from an EPF10K30E device in a 256-pin FineLine BGA package to an EPF10K250E device in a 672-pin FineLine BGA package.

The MAX+PLUS II software versions 9.1 and higher provide support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use, and MAX+PLUS II software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 17).

Figure 17. SameFrame Pin-Out Example



Output Configuration

This section discusses the peripheral component interconnect (PCI) pull-up clamping diode option, slew-rate control, open-drain output option, and MultiVolt I/O interface for FLEX 10KE devices. The PCI pull-up clamping diode, slew-rate control, and open-drain output options are controlled pin-by-pin via MAX+PLUS II logic options. The MultiVolt I/O interface is controlled by connecting VCCIO to a different voltage. Its effect can be simulated in the MAX+PLUS II software via a **Global Project Device Options** command (Assign menu).

PCI Pull-up Clamping Diode Option

FLEX 10KE devices have a pull-up clamping diode on every I/O, dedicated input, and dedicated clock pin. PCI clamping diodes clamp the signal to the V_{CCIO} value and are required for 3.3-V PCI compliance. Clamping diodes can also be used to limit overshoot in other systems.

Clamping diodes are controlled pin-by-pin. When V_{CCIO} is 3.3 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V or 3.3-V signal, but not a 5.0-V signal. When V_{CCIO} is 2.5 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V signal, but not a 3.3-V or 5.0-V signal. Additionally, a clamping diode can be activated for a subset of pins, which would allow a device to bridge between a 3.3-V PCI bus and a 5.0-V device.

Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of approximately 4.3 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate pin-by-pin or assign a default slew rate to all pins on a device-wide basis. The slow slew rate setting affects both the falling and rising edges of the output.

Open-Drain Output Option

FLEX 10KE devices provide an optional open-drain output (electrically equivalent to open-collector output) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

MultiVolt I/O Interface

The FLEX 10KE device architecture supports the MultiVolt I/O interface feature, which allows FLEX 10KE devices in all packages to interface with systems of differing supply voltages. These devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 2.5-V power supply. With a 2.5-V V_{CCINT} level, input voltages are compatible with 2.5-V, 3.3-V, and 5.0-V inputs. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels higher than 3.0-V achieve a faster timing delay of t_{OD2} instead of t_{OD1}.

Table 12 describes FLEX 10KE MultiVolt I/O support.

Table 12. FLEX 10KE MultiVolt I/O Support

V_{CCIO} (V)	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓ (1)	✓ (1)	✓		
3.3	✓	✓	✓ (1)	✓ (2)	✓	✓

Notes:

(1) The PCI clamping diode must be disabled to drive an input with signals higher than V_{CCIO}.

(2) When V_{CCIO} = 3.3 V, a FLEX 10KE device can drive a 2.5-V device that has 3.3-V tolerant inputs.

Output pins on FLEX 10KE devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. VCCIO should be connected to 3.3 V. When the I/O pin drives high, it will actively drive to VCCIO. The resistor will then pull the signal to 5.0 V. Because the FLEX 10KE device is 5.0-V tolerant, this operation will not affect the device. The PCI pull-up clamping diode must be disabled for any pin with a pull-up resistor to 5.0 V. The signal rise time is dependent on the value of the pull-up resistor and load impedance. When selecting a pull-up resistor, consider the I_{OL} current specification.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 10KE devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. FLEX 10KE devices can also be configured using the JTAG pins through the BitBlaster serial download cable, ByteBlaster parallel port download cable, or ByteBlasterMV parallel port download cable, or via hardware that uses the Jam™ programming and test language. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. FLEX 10KE devices support the JTAG instructions shown in Table 13.

Table 13. FLEX 10KE JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
UESCODE	Selects the user electronic signature (UESCODE) register and places it between the TDI and TDO pins, allowing the UESCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	These instructions are used when configuring a FLEX 10KE device via JTAG ports with a BitBlaster, ByteBlaster, or ByteBlasterMV download cable, or using a Jam File via an embedded processor.

For more information, go to the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlaster Parallel Port Download Cable Data Sheet*
- *Jam Programming and Test Language Specification*

Figure 18 shows the timing requirements for the JTAG signals.

Figure 18. FLEX 10KE JTAG Waveforms

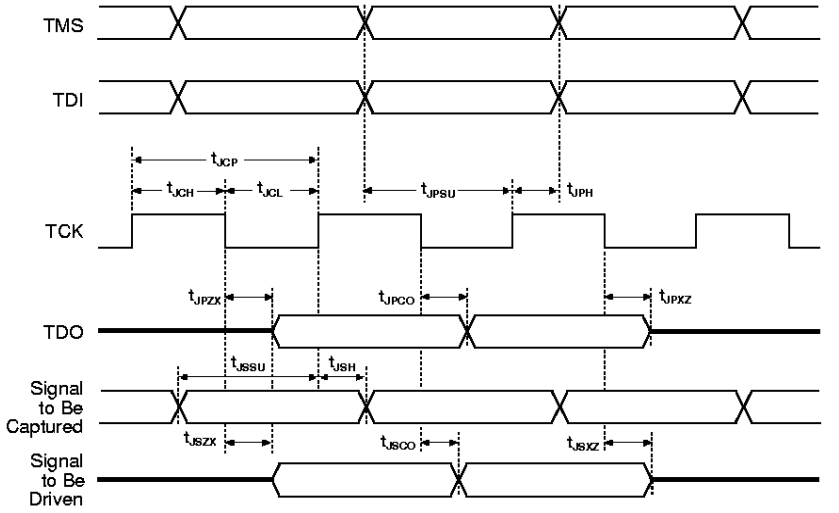


Table 14 shows the timing parameters and values for FLEX 10KE devices.

Table 14. FLEX 10KE JTAG Timing Parameters & Values

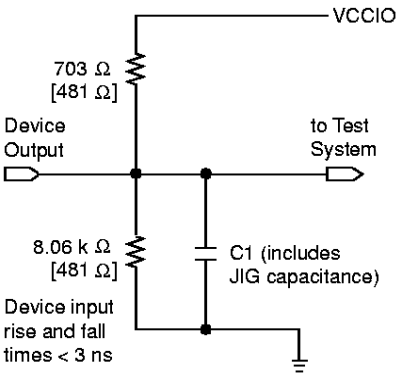
Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high-impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

Generic Testing

Each FLEX 10KE device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for FLEX 10KE devices are made under conditions equivalent to those shown in Figure 19. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 19. FLEX 10KE AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V outputs. Numbers without brackets are for 3.3-V outputs.



Operating Conditions

The following tables provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V FLEX 10KE devices.

FLEX 10KE 2.5-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground, *Note (2)*	–0.5	3.6	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–2.0	5.7	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

FLEX 10KE 2.5-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*Notes (3), (4)*	2.30 (2.30)	2.70 (2.70)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*Notes (3), (4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*Notes (3), (4)*	2.30 (2.30)	2.70 (2.70)	V
V_I	Input voltage	*Note (5)*	0	5.3	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

FLEX 10KE 2.5-V Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		1.7, 0.5 × V_{CCIO}, *Note (8)*		5.3	V
V_{IL}	Low-level input voltage		–0.3		0.8, 0.3 × V_{CCIO}, *Note (8)*	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V, *Note (9)*	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V, *Note (9)*	V_{CCIO} – 0.2			V
	3.3-V high-level PCI output voltage	I_{OH} = –0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V, *Note (9)*	0.9 × V_{CCIO}			V
	2.5-V high-level output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 2.30 V, *Note (9)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V, *Note (9)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V, *Note (9)*	1.7			V
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 4 mA DC, V_{CCIO} = 3.00 V, *Note (10)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V, *Note (10)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V, *Note (10)*			0.1 × V_{CCIO}	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V, *Note (10)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V, *Note (10)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V, *Note (10)*			0.7	V
I_I	Input pin leakage current	V_I = 5.3 to –0.3	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 5.3 to –0.3	–10		10	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load, no toggling inputs, -1 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, -2, -3 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V, *Note (11)*	20		50	kΩ
		V_{CCIO} = 2.3 V, *Note (11)*	30		80	kΩ

Capacitance of FLEX 10KE Devices *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* in the ***1998 Data Book***.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.7 V for periods shorter than 20 ns under no-load conditions.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25° C, V_{CCINT} = 2.5 V, and V_{CCIO} = 2.5 V or 3.3 V.
(7) These values are specified under "FLEX 10KE 2.5-V Device Recommended Operating Conditions" on page 42.
(8) The FLEX 10KE input buffers are compatible with 2.5-V, 3.3-V LVTTL and LVCMOS, 5.0-V TTL, and CMOS signals. Additionally, the input buffers are 3.3-V PCI compliant when V_{CCIO} and V_{CCINT} meet the relationship shown in Figure 20.
(9) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
(10) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(11) Pin pull-up resistance values will be lower if the pin is driven higher than V_{CCIO} by an external source.
(12) Capacitance is sample-tested only.

Figure 20 shows the relationship between V_{CCIO} and V_{CCINT} for 3.3-V compliance.

Figure 20. Relationship between V_{CCIO} & V_{CCINT} for 3.3-V PCI Compliance

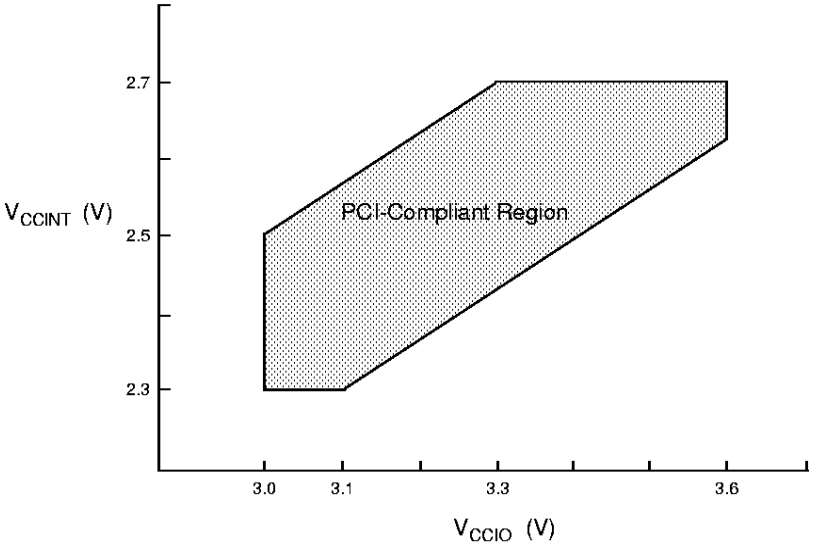
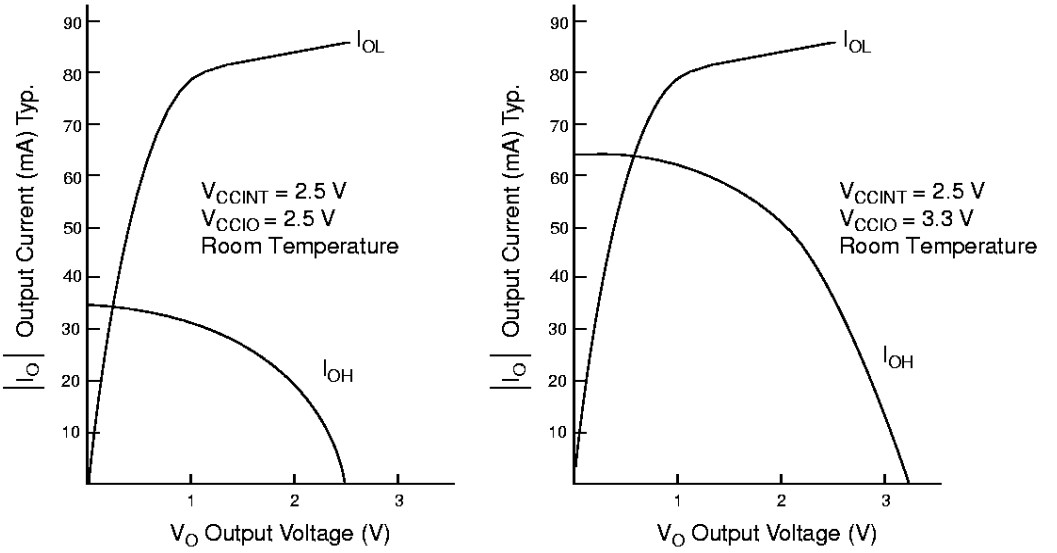


Figure 21 shows the typical output drive characteristics of FLEX 10KE devices with 3.3-V and 2.5-V V_{CCIO}. The output driver is compatible with the 3.3-V ***PCI Local Bus Specification, Revision 2.1*** (with 3.3-V V_{CCIO}).

Figure 21. Output Drive Characteristics of FLEX 10KE Devices



Timing Model

Table 15 shows the external timing parameters of FLEX 10KE devices. Detailed timing information for these devices will be released as it is available.

Table 15. FLEX 10KE External Timing Parameters

Symbol	Parameter	Device	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	
t_{DRR}	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects	EPF10K30E		8.5		10.0		13.5	ns
		EPF10K50E		8.5		10.0		13.5	ns
		EPF10K100B		11.0		12.0		14.5	ns
		EPF10K100E		10.0		12.0		16.0	ns
		EPF10K130E		10.0		12.0		16.0	ns
		EPF10K200E		10.0		12.0		16.0	ns
		EPF10K250E		11.0		13.5		17.0	ns

Power Consumption

The supply power (P) for FLEX 10KE devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value is calculated based on the amount of current that each LE typically consumes. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)* in the ***1998 Data Book***.

☞ Compared to the rest of the device, the embedded array consumes a negligible amount of power. Therefore, the embedded array can be ignored when calculating supply current.

The $I_{CCACTIVE}$ value can be calculated with the following equation:

$$I_{CCACTIVE} = K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}} \times \frac{\mu A}{MHz \times LE}$$

Where:

$\mathbf{f_{MAX}}$	=	Maximum operating frequency in MHz
N	=	Total number of LEs used in the device
$\mathbf{tog_{LC}}$	=	Average percent of LEs toggling at each clock (typically 12.5%)
K	=	Constant

Table 16 provides the constant (K) values for EPF10K50E, EPF10K100B, and EPF10K200E devices. K factors for other FLEX 10KE devices will be released as they become available.

Table 16. FLEX 10KE K Constant Values

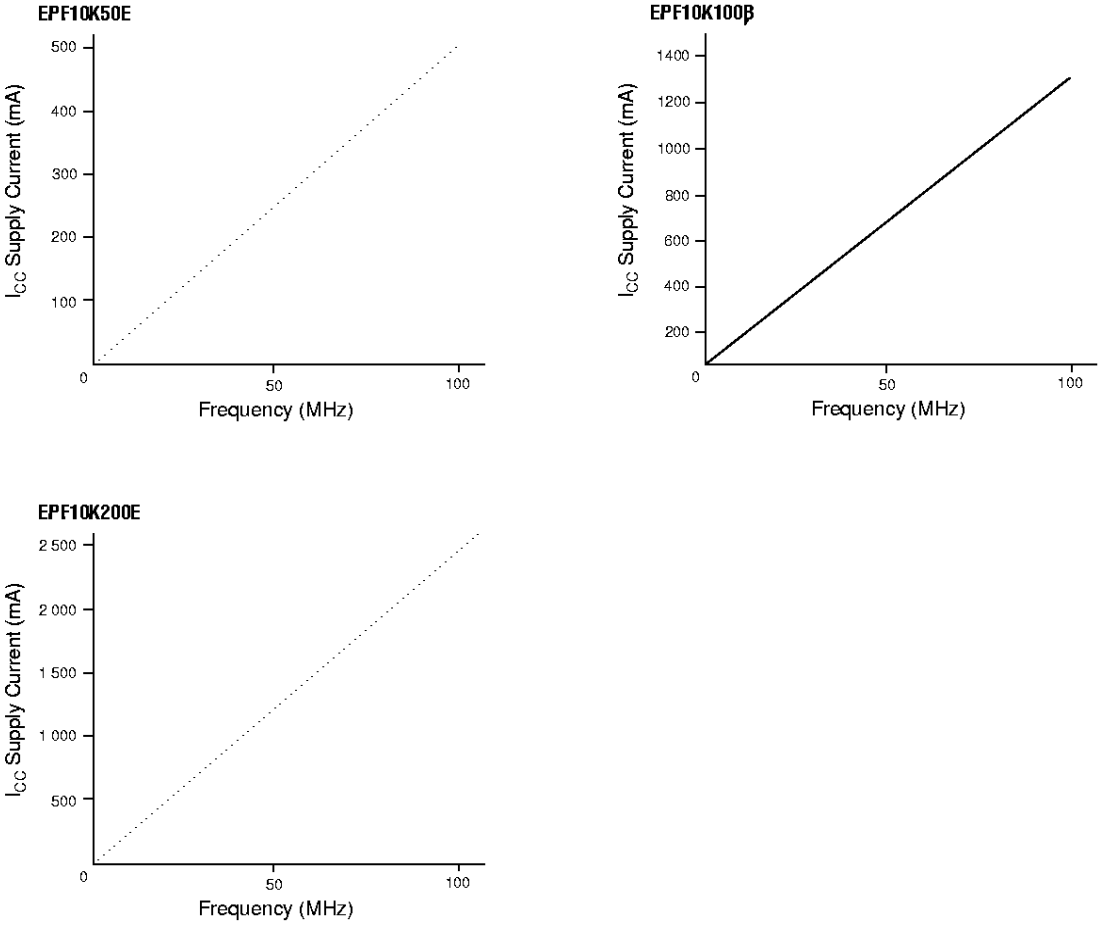
Device	K Value
EPF10K50E	14
EPF10K100B	19
EPF10K200E	19

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

To better reflect actual designs, the power model (and the constant K in the power calculation equations) for continuous interconnect FLEX devices assume that LEs drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assume that all LEs drive only one short interconnect segment. This assumption may lead to inaccurate results when compared to measured power consumption for actual designs in segmented FPGAs.

Figure 22 shows the relationship between the current and operating frequency of EPF10K50E, EPF10K100B, and EPF10K200E devices. For other FLEX 10KE devices, contact Altera Applications at (800) 800-EPLD.

Figure 22. FLEX 10KE $I_{CCACTIVE}$ vs. Operating Frequency



Configuration & Operation

The FLEX 10KE architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The FLEX 10KE architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. The process of physically loading the SRAM data into the device is called *configuration*. Before configuration, as V_{CC} rises, the device initiates a Power-On Reset (POR). This POR event clears the device and prepares it for configuration. The FLEX 10KE POR time does not exceed 50 µs; however, when configuring with a Configuration EPROM, the Configuration EPROM imposes a 100 µs delay that allows system power to stabilize before configuration.

During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow FLEX 10KE devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 330 ms and can be used to reconfigure an entire system dynamically. In-field upgrades can be performed by distributing new configuration files.

Before and during configuration, all I/O pins (except dedicated inputs, clock, or configuration pins) are pulled high by a weak pull-up resistor.

Programming Files

Despite being function- and pin-compatible, FLEX 10KE devices are not programming- or configuration-file-compatible with FLEX 10K or FLEX 10KA devices. A design therefore must be recompiled before it is transferred from a FLEX 10K or FLEX 10KA device to an equivalent FLEX 10KE device. This recompilation should be performed both to create a new programming or configuration file and to check design timing in the faster FLEX 10KE device.

FLEX 10KE devices are generally pin-compatible with the equivalent FLEX 10KA device. In some cases, FLEX 10KE devices have fewer I/O pins than FLEX 10KA devices. Table 17 shows which FLEX 10KE devices have fewer I/Os. However, power, ground, JTAG, and configuration pins are the same on FLEX 10KA and FLEX 10KE devices, enabling migration from a FLEX 10KA design to a FLEX 10KE design.

Table 17. I/O Count on FLEX 10KA & FLEX 10KE Devices

FLEX 10KA		FLEX 10KE	
Device	**I/O Count**	**Device**	**I/O Count**
EPF10K30AF256	191	EPF10K30EF256	176
EPF10K30AF484	244	EPF10K30EF484	218
EPF10K30AB356	246	EPF10K30EB356	220
EPF10K50VF484	300	EPF10K50EF484	254
EPF10K50VB356	274	EPF10K50EB356	256
EPF10K100AF484	366	EPF10K100EF484	337
EPF10K130VB600	470	EPF10K130EB600	426

Configuration Schemes

The configuration data for a FLEX 10KE device can be loaded with one of five configuration schemes (see Table 18), chosen on the basis of the target application. An EPC2, EPC1, or EPC1441 Configuration EPROM, intelligent controller, or the JTAG port can be used to control the configuration of a FLEX 10KE device, allowing automatic configuration on system power-up.

Multiple FLEX 10KE devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device. Additional FLEX 10K, FLEX 10KA, FLEX 10KE, and FLEX 6000 devices can be configured in the same serial chain.

Table 18. Data Sources for FLEX 10KE Configuration

Configuration Scheme	Data Source
Configuration EPROM	EPC1, EPC2, or EPC1441 Configuration EPROM
Passive serial (PS)	BitBlaster, ByteBlaster, or ByteBlasterMV download cables, or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	BitBlaster, ByteBlaster, or ByteBlasterMV download cables, or microprocessor with a Jam File

Device Pin-Outs

Table 19 shows the dedicated pin-outs for FLEX 10KE devices in 144-pin TQFP, 208-pin PQFP, 240-pin PQFP, 356-pin BGA, 599-pin PGA, and 600-pin BGA packages.

Table 19. FLEX 10KE Device Pin-Outs (Part 1 of 4) *Note (1)*

Pin Name	144-Pin TQFP EPF10K30E EPF10K50E	208-Pin PQFP EPF10K30E EPF10K50E EPF10K100E EPF10K100β	240-Pin PQFP EPF10K50E EPF10K100E EPF10K100β	240-Pin PQFP EPF10K130E	356-Pin βGA EPF10K100E	599-Pin PGA EPF10K200E EPF10K250E	600-Pin βGA EPF10K200E EPF10K250E
MSEL0 *(2)*	77	108	124	124	D4	F6	F5
MSEL1 *(2)*	76	107	123	123	D3	C3	C1
nSTATUS *(2)*	35	52	60	60	D24	E43	D32
nCONFIG *(2)*	74	105	121	121	D2	B4	D4
DCLK *(2)*	107	155	179	179	AC5	BE5	AP1
CONF_DONE *(2)*	2	2	2	2	AC24	BC43	AM32
INIT_DONE *(3)*	14	19	26	26	T24	AM40	AE32
nCE *(2)*	106	154	178	178	AC2	BB6	AN2
nCEO *(2)*	3	3	3	3	AC22	BF44	AP35
nWS *(4)*	142	206	238	238	AE24	BB40	AR29
nRS *(4)*	141	204	236	236	AE23	BA37	AM28

Table 19. FLEX 10KE Device Pin-Outs (Part 2 of 4) *Note (1)*

Pin Name	144-Pin TQFP EPF10K30E EPF10K50E	208-Pin PQFP EPF10K30E EPF10K50E EPF10K100E EPF10K100β	240-Pin PQFP EPF10K50E EPF10K100E EPF10K100β	240-Pin PQFP EPF10K130E	356-Pin βGA EPF10K100E	599-Pin PGA EPF10K200E EPF10K250E	600-Pin βGA EPF10K200E EPF10K250E
nCS *(4)*	144	208	240	240	AD24	AY38	AL29
CS *(4)*	143	207	239	239	AD23	BA39	AN29
RDYnBSY *(4)*	11	16	23	23	U22	AW47	AG35
CLKUSR *(4)*	7	10	11	11	AA24	AY42	AM34
DATA7 *(4)*	116	166	190	190	AF4	BD14	AM13
DATA6 *(4)*	114	164	188	188	AD8	BA17	AR12
DATA5 *(4)*	113	162	186	186	AE5	BB16	AN12
DATA4 *(4)*	112	161	185	185	AD6	BF12	AP11
DATA3 *(4)*	111	159	183	183	AF2	BG11	AM11
DATA2 *(4)*	110	158	182	182	AD5	BG9	AR10
DATA1 *(4)*	109	157	181	181	AD4	BF10	AN10
DATA0 *(2)*, *(5)*	108	156	180	180	AD3	BC5	AM4
TDI *(2)*	105	153	177	177	AC3	BF4	AN1
TDO *(2)*	4	4	4	4	AC23	BB42	AN34
TCK *(2)*	1	1	1	1	AD25	BE43	AL31
TMS *(2)*	34	50	58	58	D22	F42	C35
TRST *(2)*	*Note (6)*	51	59	59	D23	B46	C34
Dedicated Inputs	54, 56, 124, 126	78, 80, 182, 184	90, 92, 210, 212	90, 92, 210, 212	A13, B14, AF14, AE13	B24, C25, BG25, BG23	C18, D18, AM18, AN18
Dedicated Clock Pins	55, 125	79, 183	91, 211	91, 211	A14, AF13	BF24, A25	AL18, E18
DEV_CLRn *(3)*	122	180	209	209	AD13	–	–
DEV_OE *(3)*	128	186	213	213	AE14	–	–
VCCINT (2.5 V)	6, 25, 52, 53, 75, 93, 123	6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181	5, 27, 47, 89, 96, 122, 130, 150, 170	5, 20, 27, 47, 76, 89, 96, 122, 130, 150, 159, 170	A1, A26, C14, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26	BE23	AR17

Table 19. FLEX 10KE Device Pin-Outs (Part 3 of 4) *Note (1)*

Pin Name	144-Pin TQFP EPF10K30E EPF10K50E	208-Pin PQFP EPF10K30E EPF10K50E EPF10K100E EPF10K100β	240-Pin PQFP EPF10K50E EPF10K100E EPF10K100β	240-Pin PQFP EPF10K130E	356-Pin βGA EPF10K100E	599-Pin PGA EPF10K200E EPF10K250E	600-Pin βGA EPF10K200E EPF10K250E
VCCIO (2.5 or 3.3 V)	5, 24, 45, 61, 71, 94, 115, 134	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194	16, 37, 57, 77, 112, 140, 160, 189, 205, 224	16, 37, 57, 77, 112, 140, 160, 189, 205, 224	A7, A23, B4, C15, D25, F4, H24, K5, M23, P2, T25, V2, W22, AB1, AC25, AD18, AF3, AF7, AF16	BC25	AR19
GNDINT	16, 57, 58, 84, 103, 127	21, 33, 49, 81, 82, 123, 129, 151, 185	10, 22, 32, 42, 52, 69, 85, 93, 104, 125, 135, 145, 155, 165, 176, 197, 216, 232	10, 22, 32, 42, 52, 69, 85, 93, 104, 125, 135, 145, 155, 165, 176, 197, 216, 232	A2, A10, A20, B1, B13, B22, B25, B26, C2, C9, C13, C25, H23, J26, K1, M1, N26, R1, R26, T1, U26, W1, AD2, AD14, AD20, AE1, AE2, AE7, AE25, AE26, AF11, AF19, AF25	E5, A3, A45, C1, C11, C19, C29, C37, C47, G25, L3, L45, W3, W45, AJ3, AJ45, AU3, AU45, BE1, BE11, BE19, BE29, BE37, BE47, BG3, BG45	AL3, AG5, AE4, AB5, Y2, U3, P5, M2, H1, B1, A11, B18, D24, F31, F35, K32, N34, T35, V32, AA33, AD35, AF32, AK35, AK31, AP24, AR18, AR11, E2, A19

Table 19. FLEX 10KE Device Pin-Outs (Part 4 of 4) *Note (1)*

Pin Name	144-Pin TQFP EPF10K30E EPF10K50E	208-Pin PQFP EPF10K30E EPF10K50E EPF10K100E EPF10K100β	240-Pin PQFP EPF10K50E EPF10K100E EPF10K100β	240-Pin PQFP EPF10K130E	356-Pin βGA EPF10K100E	599-Pin PGA EPF10K200E EPF10K250E	600-Pin βGA EPF10K200E EPF10K250E
GNDIO	15, 40, 50, 66, 85, 104, 129, 139	20, 32, 48, 59, 72, 91, 124, 130, 152, 171, 188, 201	–	–	–	D24, E9, E15, E21, E27, E33, E39, G7, G41, J5, J43, R5, R43, AA5, AA43, AD4, AD44, AG5, AG43, AN5, AN43, AW5, AW43, BA7, BA41, BC9, BC15, BC21, BC27, BC33, BC39, BD24	C8, E12, C15, A20, C23, A27, AM26, AR23, AM19, AN15, AL12, AN8, C2, C3, C4, D5, E5, C33, C32, D31, E31, AL5, AM5, AN4, AN3, AM31, AN32, AN33, AP34
Total User I/O Pins *(7)*	102	147	189	186	274	470	470

Notes:
(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) The optional JTAG pin TRST is not used in the 144-pin TQFP package.
(7) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.

Table 20 shows the dedicated pin-outs for FLEX 10KE devices in 256-pin FineLine BGA and 672-pin FineLine BGA packages.

Table 20. FLEX 10KE FineLine BGA Device Pin-Outs (Part 1 of 4) *Note (1)*

Pin Name	256-Pin FineLine BGA EPF10K30E	256-Pin FineLine BGA EPF10K50E EPF10K100E EPF10K100B	672-Pin FineLine BGA EPF10K130E	672-Pin FineLine BGA EPF10K200E EPF10K250E
MSEL0 *(2)*	P1	P1	W6	W6
MSEL1 *(2)*	R1	R1	Y6	Y6
nSTATUS *(2)*	T16	T16	AA21	AA21
nCONFIG *(2)*	N4	N4	V9	V9
DCLK *(2)*	B2	B2	G7	G7
CONF_DONE *(2)*	C15	C15	H20	H20
INIT_DONE *(3)*	G16	G16	M21	M21
nCE *(2)*	B1	B1	G6	G6
nCEO *(2)*	B16	B16	G21	G21
nWS *(4)*	B14	B14	G19	G19
nRS *(4)*	C14	C14	H19	H19
nCS *(4)*	A16	A16	F21	F21
CS *(4)*	A15	A15	F20	F20
RDYnBSY *(4)*	G14	G14	M19	M19
CLKUSR *(4)*	D15	D15	J20	J20
DATA7 *(4)*	B5	B5	G10	G10
DATA6 *(4)*	D4	D4	J9	J9
DATA5 *(4)*	A4	A4	F9	F9
DATA4 *(4)*	B4	B4	G9	G9
DATA3 *(4)*	C3	C3	H8	H8
DATA2 *(4)*	A2	A2	F7	F7
DATA1 *(4)*	B3	B3	G8	G8
DATA0 *(2)*, *(5)*	A1	A1	F6	F6
TDI *(2)*	C2	C2	H7	H7
TDO *(2)*	C16	C16	H21	H21
TCK *(2)*	B15	B15	G20	G20
TMS *(2)*	P15	P15	W20	W20
TRST *(2)*	R16	R16	Y21	Y21
Dedicated Inputs	B9, E8, M9, R8	B9, E8, M9, R8	Y13, U14, G14, K13	Y13, U14, G14, K13
Dedicated Clock Pins	A9, L8	A9, L8	T13, F14	T13, F14

Table 20. FLEX 10KE FineLine βGA Device Pin-Outs (Part 2 of 4) *Note (1)*

Pin Name	256-Pin FineLine βGA EPF10K30E	256-Pin FineLine βGA EPF10K50E EPF10K100E EPF10K100β	672-Pin FineLine βGA EPF10K130E	672-Pin FineLine βGA EPF10K200E EPF10K250E
DEV_CLRn *(3)*	D8	D8	J13	J13
DEV_OE *(3)*	C9	C9	H14	H14
VCCINT (2.5 V)	E11, F5, F7, F9, F12, H6, H7, H10, J7, J10, J11, K9, L5, L7, L9, L12, M11, R2	E11, F5, F7, F9, F12, H6, H7, H10, J7, J10, J11, K9, L5, L7, L9, L12, M11, R2	E13, E17, H2, H25, K16, L10, L12, L14, L17, M2, M25, N11, N12, N15, P12, P15, P16, R14, T2, T10,T12, T14, T17, T25, U16, Y7, AA23, AB10, AC14	E13, E17, H2, H25, K16, L10, L12, L14, L17, M2, M25, N11, N12, N15, P12, P15, P16, R14, T2, T10,T12, T14, T17, T25, U16, Y7, AA23, AB10, AC14
VCCIO (2.5 or 3.3 V)	D12, E6, F8, F10, G6, G8, G11, H11, J6, K6, K8, K11, L10, M6, N12	D12, E6, F8, F10, G6, G8, G11, H11, J6, K6, K8, K11, L10, M6, N12	C8, C15, D7, G3, J3, J17, K11, K22, L13, L15, M11, M13, M16, M22, N16, P11, R5, R11, R13, R16, R22, T15, U3, U11, V5, V17, V24, Y2, Y24, AA26, AD15	C8, C15, D7, G3, J3, J17, K11, K22, L13, L15, M11, M13, M16, M22, N16, P11, R5, R11, R13, R16, R22, T15, U3, U11, V5, V17, V24, Y2, Y24, AA26, AD15
GND	E5, E12, F6, F11, G7, G9, G10, H8, H9, J8, J9, K7, K10, L6, L11, M5, M12, T8	E5, E12, F6, F11, G7, G9, G10, H8, H9, J8, J9, K7, K10, L6, L11, M5, M12, T8	A2, A25, B2, B25, C3, C10, C24, D3, D4, D19, D23, D24, E4, E23, G23, J5, J23, K4, K10, K17, L11, L16, L22, M5, M12, M14, M15, N13, N14, P13, P14, P22, R12, R15, T11, T16, U10, U17, U24, V3, Y5, AA13, AA22, AB3, AB4, AB5, AB23, AB24, AC3, AC8, AC24, AD13, AD18, AE2, AE25, AF2, AF25	A2, A25, B2, B25, C3, C10, C24, D3, D4, D19, D23, D24, E4, E23, G23, J5, J23, K4, K10, K17, L11, L16, L22, M5, M12, M14, M15, N13, N14, P13, P14, P22, R12, R15, T11, T16, U10, U17, U24, V3, Y5, AA13, AA22, AB3, AB4, AB5, AB23, AB24, AC3, AC8, AC24, AD13, AD18, AE2, AE25, AF2, AF25

Table 20. FLEX 10KE FineLine βGA Device Pin-Outs (Part 3 of 4) *Note (1)*

Pin Name	256-Pin FineLine βGA EPF10K30E	256-Pin FineLine βGA EPF10K50E EPF10K100E EPF10K100β	672-Pin FineLine βGA EPF10K130E	672-Pin FineLine βGA EPF10K200E EPF10K250E
No Connect (N.C.)	D1, E3, E16, G3, H1, H16, J1, K3, K14, K16, L2, L4, M14, M16, N15	–	A4, A5, A6, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B16, B19, B20, B21, B22, B23, B24, C1, AE4, AE5, AE6, AE7, AE8, AE9, AE10, AE11, AE12, AE14, AE15, AE16, AE17, AF18, AE19, AE20, AE21, AE22, AE23, AF4, AF5, AF6, AF7, AF8, AF9, AF10, AF12, AF13, AF14, AF15, AF16, AF20, AF21, AF24, AF23	A3, A4, A5, A6, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B16, B19, B20, B21, B22, B23, B24, B26, C1, C25, C26, D1, D2, D25, D26, E1, E25, E26, F1, F25, G25, G26, H1, J1, J25, J26, K26, L2, L25, N2, P1, P2, R1, R26, T1, U1, U25, V1, V26, W1, Y26, AA1, AA2, AA25, AB2, AB25, AB26, AC1, AC2, AC25, AC26, AD2, AD26, AE1, AE3, AE4, AE5, AE6, AE7, AE8, AE9, AE10, AE11, AE12, AE14, AE15, AE16, AE17, AE19, AE20, AE21, AE22, AE23, AE24, AE26, AF3, AF4, AF5, AF6, AF7, AF8, AF9, AF10, AF11, AF12, AF13, AF14, AF15, AF16, AF17, AF18, AF20, AF21, AF23, AF24

Table 20. FLEX 10KE FineLine βGA Device Pin-Outs (Part 4 of 4) *Note (1)*

Pin Name	256-Pin FineLine βGA EPF10K30E	256-Pin FineLine βGA EPF10K50E EPF10K100E EPF10K100β	672-Pin FineLine βGA EPF10K130E	672-Pin FineLine βGA EPF10K200E EPF10K250E
Total User I/O Pins *(7)*	176	191	413	470

Notes:
(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) The optional JTAG pin TRST is not used in the 144-pin TQFP package.
(7) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.

Table 21 shows the dedicated pin-outs for FLEX 10KE devices in 484-pin FineLine BGA packages.

Table 21. FLEX 10KE FineLine βGA Device Pin-Outs (Part 1 of 5) *Note (1)*

Pin Name	484-Pin FineLine βGA EPF10K30E	484-Pin FineLine βGA EPF10K50E	484-Pin FineLine βGA EPF10K100E	484-Pin FineLine βGA EPF10K130E
MSEL0 *(2)*	U4	U4	U4	U4
MSEL1 *(2)*	V4	V4	V4	V4
nSTATUS *(2)*	W19	W19	W19	W19
nCONFIG *(2)*	T7	T7	T7	T7
DCLK *(2)*	E5	E5	E5	E5
CONF_DONE *(2)*	F18	F18	F18	F18
INIT_DONE *(3)*	K19	K19	K19	K19
nCE *(2)*	E4	E4	E4	E4
nCEO *(6)*	E19	E19	E19	E19
nWS *(4)*	E17	E17	E17	E17
nRS *(4)*	F17	F17	F17	F17
nCS *(4)*	D19	D19	D19	D19
CS *(4)*	D18	D18	D18	D18
RDYnBSY *(4)*	K17	K17	K17	K17
CLKUSR *(4)*	G18	G18	G18	G18
DATA7 *(4)*	E8	E8	E8	E8
DATA6 *(4)*	G7	G7	G7	G7

Table 21. FLEX 10KE FineLine βGA Device Pin-Outs (Part 2 of 5) Note (1)				
Pin Name	**484-Pin FineLine βGA EPF10K30E**	**484-Pin FineLine βGA EPF10K50E**	**484-Pin FineLine βGA EPF10K100E**	**484-Pin FineLine βGA EPF10K130E**
DATA5 *(4)*	D7	D7	D7	D7
DATA4 *(4)*	E7	E7	E7	E7
DATA3 *(4)*	F6	F6	F6	F6
DATA2 *(4)*	D5	D5	D5	D5
DATA1 *(4)*	E6	E6	E6	E6
DATA0 *(2)*, *(5)*	D4	D4	D4	D4
TDI *(2)*	F5	F5	F5	F5
TDO *(2)*	F19	F19	F19	F19
TCK *(2)*	E18	E18	E18	E18
TMS *(2)*	U18	U18	U18	U18
TRST *(2)*	V19	V19	V19	V19
Dedicated Inputs	E12, H11, R12, V11	E12, H11, R12, V11	E12, H11, R12, V11	E12, H11, R12, V11
Dedicated Clock Pins	D12, P11	D12, P11	D12, P11	D12, P11
DEV_CLRn *(3)*	G11	G11	G11	G11
DEV_OE *(3)*	F12	F12	F12	F12
VCCINT (2.5 V)	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P12, P15, R14, V5, W21, Y8, AA12	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P12, P15, R14, V5, W21, Y8, AA12	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P12, P15, R14, V5, W21, Y8, AA12	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P12, P15, R14, V5, W21, Y8, AA12
VCCIO (2.5 or 3.3 V)	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13

Table 21. FLEX 10KE FineLine βGA Device Pin-Outs (Part 3 of 5) Note (1)

Pin Name	484-Pin FineLine βGA EPF10K30E	484-Pin FineLine βGA EPF10K50E	484-Pin FineLine βGA EPF10K100E	484-Pin FineLine βGA EPF10K130E
GND	A1, A8, A22, B1, B2, B17, B21, B22, C2, C21, E21, G3, G21, H2, H8, H15, J9, J14, J20, K3, K10, K12, K13, L11, L12, M11, M12, M20, N10, N13, P9, P14, R8, R15, R22, T1, V3, W11, W20, Y1, Y2, Y3, Y21, Y22, AA1, AA6, AA22, AB11, AB16	A1, A8, A22, B1, B2, B17, B21, B22, C2, C21, E21, G3, G21, H2, H8, H15, J9, J14, J20, K3, K10, K12, K13, L11, L12, M11, M12, M20, N10, N13, P9, P14, R8, R15, R22, T1, V3, W11, W20, Y1, Y2, Y3, Y21, Y22, AA1, AA6, AA22, AB11, AB16	A1, A8, A22, B1, B2, B17, B21, B22, C2, C21, E21, G3, G21, H2, H8, H15, J9, J14, J20, K3, K10, K12, K13, L11, L12, M11, M12, M20, N10, N13, P9, P14, R8, R15, R22, T1, V3, W11, W20, Y1, Y2, Y3, Y21, Y22, AA1, AA6, AA22, AB11, AB16	A1, A8, A22, B1, B2, B17, B21, B22, C2, C21, E21, G3, G21, H2, H8, H15, J9, J14, J20, K3, K10, K12, K13, L11, L12, M11, M12, M20, N10, N13, P9, P14, R8, R15, R22, T1, V3, W11, W20, Y1, Y2, Y3, Y21, Y22, AA1, AA6, AA22, AB11, AB16

Table 21. FLEX 10KE FineLine βGA Device Pin-Outs (Part 4 of 5) *Note (1)*

Pin Name	484-Pin FineLine βGA EPF10K30E	484-Pin FineLine βGA EPF10K50E	484-Pin FineLine βGA EPF10K100E	484-Pin FineLine βGA EPF10K130E
No Connect (N.C.)	A2, A3, A4, A5, A7, A9, A11, A12, A14, A15, A20, A21, B3, B4, B9, B10, B12, B16, B19, B20, C1, C6, C9, C10, C12, C13, C14, C16, C17, C22, D1, D2, D3, D20, D21, D22, E2, E3, E20, E22, F1, F2, F3, F20, F21, F22, G2, G4, G20, G22, H1, H3, H6, H19, H21, H22, J1, J2, J3, J21, J22, K1, K2, K6, K21, K22, L1, L2, L3, L4, L19, L20, L21, L22, M1, M2, M3, M4, M21, M22, N1, N2, N21, N22, N6, N17, N19, P1, P2, P3, P5, P7, P20, P21, P22, R2, R3, R17, R19, R20, R21, T2, T18, T20, T21, U1, U2, U3, U20, U21, U22, V1, V2, V20, V21, W1, W2, W22, Y4, Y9, Y12, Y13, Y16, Y19, Y20, AA2, AA3, AA4, AA9, AA11, AA13, AA15, AA21, AB1, AB2, AB3, AB4, AB5, AB7, AB8, AB9, AB12, AB15, AB17, AB18, AB19, AB20, AB21, AB22	A2, A3, A4, A5, A7, A9, A11, A12, A14, A15, A20, A21, B3, B4, B9, B10, B12, B16, B19, B20, C1, C6, C9, C10, C12, C13, C14, C16, C17, C22, D1, D2, D3, D20, D21, E2, E3, E20, E22, F1, F2, F20, F21, G2, G20, G22, J1, J2, J3, J21, K2, K22, L1, L2, L20, L22, M2, M3, M22, N1, N2, N21, N22, P3, P20, P21, P22, R2, R3, R21, T2, T20, T21, U1, U2, U3, U20, U21, U22, V2, V20, W1, W2, W22, Y4, Y9, Y12, Y13, Y16, Y19, Y20, AA2, AA3, AA4, AA9, AA11, AA13, AA15, AA21, AB1, AB2, AB3, AB4, AB5, AB7, AB8, AB9, AB12, AB15, AB17, AB18, AB19, AB20, AB21, AB22	A2, A3, A4, A5, B3, B4, B10, C17, F2, J2, K2, L2, N1, P20, P22, R3, T20, T21, U1, W22, Y16, AA15, AB3, AB4, AB5, AB7, AB15, AB17, AB18, AB19, AB20	–
GNDINT	–	–	–	–

Table 21. FLEX 10KE FineLine βGA Device Pin-Outs (Part 5 of 5) *Note (1)*

Pin Name	484-Pin FineLine βGA EPF10K30E	484-Pin FineLine βGA EPF10K50E	484-Pin FineLine βGA EPF10K100E	484-Pin FineLine βGA EPF10K130E
GNDIO	–	–	–	–
Total User I/O Pins *(7)*	220	254	338	369

Notes to Tables:
(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) The optional JTAG pin TRST is not used in the 144-pin TQFP package.
(7) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.

Table 22 shows pin compatibility between FLEX 10KE devices.

Table 22. FLEX 10KE Device Pin Compatibility

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	256-Pin FineLine βGA	484-Pin FineLine βGA	599-Pin PGA	600-Pin βGA	672-Pin FineLine βGA
EPF10K30E	*Note (1)*	*Note (1)*		*Note (2)*	*Note (2)*			
EPF10K50E	*Note (1)*	*Note (1)*	*Note (2)*	*Note (2)*	*Note (2)*			
EPF10K100B		*Note (1)*	*Note (2)*	*Note (2)*				
EPF10K100E		*Note (1)*	*Note (2)*	*Note (2)*	*Note (2)*			
EPF10K130E			*Note (2)*		*Note (2)*			*Note (2)*
EPF10K200E						*Note (1)*	*Note (1)*	*Note (2)*
EPF10K250E						*Note (1)*	*Note (1)*	*Note (2)*

Notes:
(1) Devices in the same package are pin-compatible and have the same number of I/O pins.
(2) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices. MAX+PLUS II software versions 9.1 and higher provide features to help use only the common pins.

Table 23 shows the FLEX 10KE device/package combinations that support SameFrame pin-outs. All FineLine BGA packages support SameFrame pin-outs providing the flexibility to migrate not only from device to device within the same package, but also from one package to another. The I/O count will vary, and MAX+PLUS II software versions 9.1 and higher provide features to help use only the common pins.

Table 23. FLEX 10KE SameFrame Pin-Out Support

Device	256-Pin FineLine BGA	484-Pin FineLine BGA	672-Pin FineLine BGA
EPF10K30E	✓	✓	
EPF10K50E	✓	✓	
EPF10K100B	✓		
EPF10K100E	✓	✓	
EPF10K130E		✓	✓
EPF10K200E			✓
EPF10K250E			✓

Revision History

The information contained in the *FLEX 10KE Embedded Programmable Logic Family Data Sheet* version 1.01 supersedes information published in previous versions.

The *FLEX 10KE Embedded Programmable Logic Family Data Sheet* version 1.01 contains the following change:

- Updated Table 15 (FLEX 10KE external timing parameters).

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