ZCU106 Evaluation Board

User Guide

UG1244 (v1.0) March 28, 2018

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/28/2018	1.0	Initial Xilinx release.

Table of Contents

Appendix D: Additional Resources and Legal Notices

Introduction

Overview

The ZCU106 is a general purpose evaluation board for rapid-prototyping based on the ZU7EV silicon part and package in the 16 nm FinFET Zynq® UltraScale+™ MPSoC. The ZU7EV device integrates a quad core ARM® Cortex™-A53 processing system (PS) and a dual core ARM Cortex-R5 real-time processor, which provides application developers an unprecedented level of heterogeneous multiprocessing. The ZCU106 evaluation board provides a flexible prototyping platform with high-speed DDR4 memory interfaces, FMC expansion ports, multi-gigabit per second serial transceivers, video codec unit (VCU), several peripheral interfaces, and FPGA fabric for customized designs.

Additional Resources

See Appendix D, Additional Resources and Legal Notices for references to documents, files, and resources relevant to the ZCU106 evaluation board.

Block Diagram

The ZCU106 board block diagram is shown in Figure 1-1.

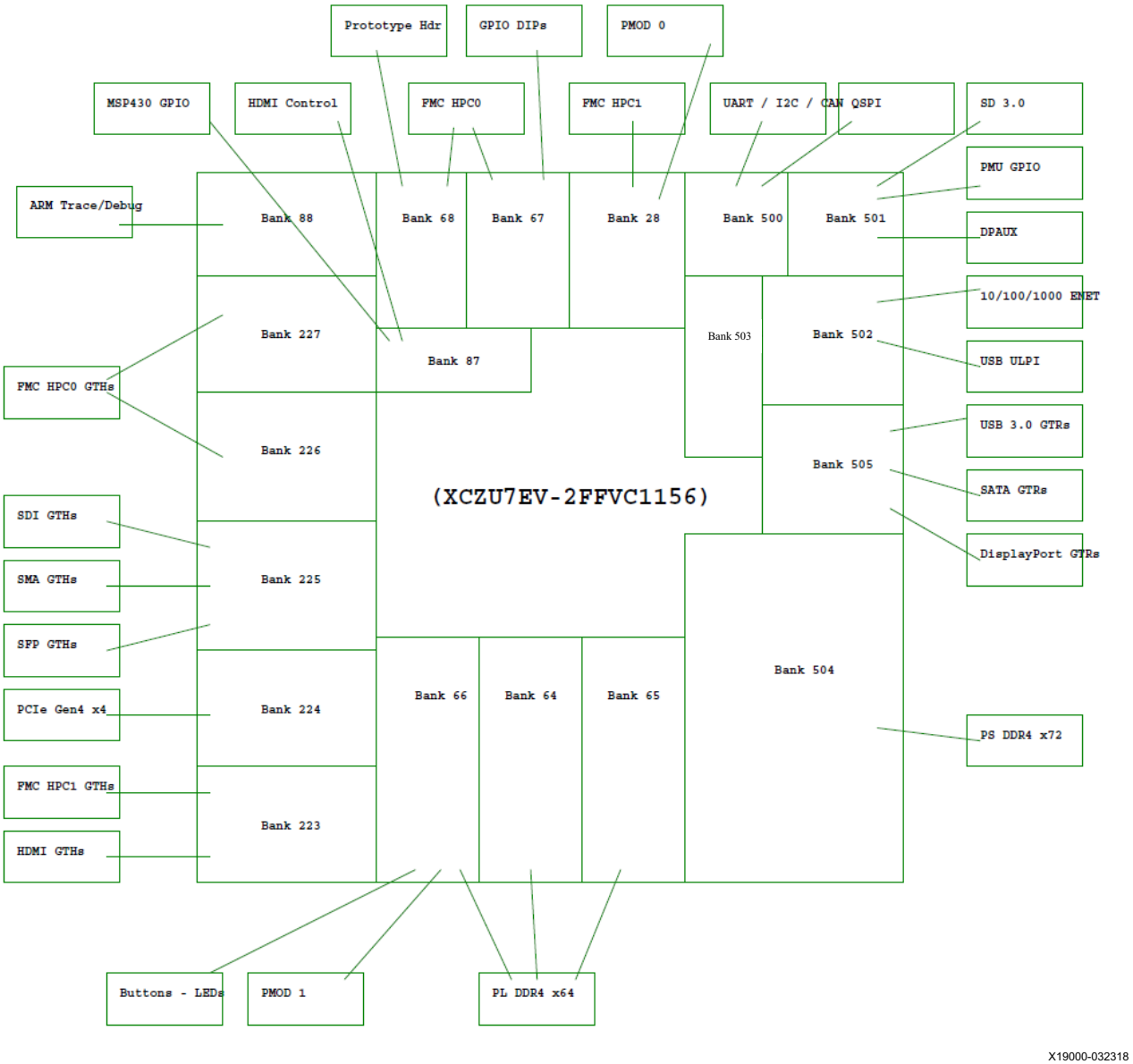


Figure 1-1: **ZCU106 Evaluation Board Block Diagram**

Board Features

The ZCU106 evaluation board features are listed here. Detailed information for each feature is provided in Component Descriptions in Chapter 3.

- XCZU7EV-2, FFVC1156 package
- PL V_{CCINT} for range in data sheet
- Form factor for PCIe® Gen[1-3]x4 endpoint (PL GTH transceiver), Micro-ATX chassis footprint
- Configuration from Quad SPI
- Configuration from SD card
- Configuration over JTAG with platform cable USB header
- Configuration over JTAG with ARM 20-pin header
- Configuration over USB-to-JTAG bridge
- Clocks
  - USER_MGT_SI570
  - PL_74.25M, PL_125M, PL_300M
  - USER_SMA_MGT
  - GTR_DP, GTR_USB3, GTR_SATA
  - PS_REF_CLK
- PS DDR4 72-bit SODIMM (includes ECC)
- PL DDR4 64-bit component (4x16-bit)
- PS-GTR assignment
  - DisplayPort (two GTRs)
  - USB3 (one GTR)
  - SATA (one GTR)
- PL GTH transceiver assignment (20 total)
  - High-definition multimedia interface (HDMI®) (three GTH transceivers)
  - FMC HPC1 DP (one GTH transceiver)
  - PCIe (four GTH transceivers)
  - SDI (one GTH transceiver)
  - SMA (one GTH transceiver)

  - SFP+ (two GTH transceivers)
  - FMC HPC0 DP (eight GTH transceivers)
- PL FMC HPC0 connectivity - full LA bus
- PL FMC HPC1 connectivity - partial LA bus
- PS MIO: dual Quad SPI
- PS MIO: two channels of quad-UART bridge
- PS MIO: CAN
- PS MIO: I2C shared across PS and PL
- PS MIO: SD
- PS MIO: DisplayPort
- PS MIO: system controller I/F
- PS MIO: Ethernet
- PS MIO: USB3
- PS-side user LED (one)
- PS-side user pushbutton (one)
- PL-side user LEDs (eight)
- PL-side user DIP switch (8-position)
- PL-side user pushbuttons (five)
- PL-side CPU reset pushbutton
- PL-side PMOD headers
- PL-side bank 0 PROG_B pushbutton
- Security - PSBATT button battery backup
- SYSMON (previously XADC), prototype header
- Operational switches (power on/off, PROG_B, boot mode DIP switch)
- Operational status LEDs (power status, INIT, DONE, PG, JTAG status, DDR power good)
- Power management

The ZCU106 provides designers a rapid prototyping platform using the XCZU7EV-2FFVC1156 device. The ZU7EV contains many PS hard block peripherals exposed through the multi-use I/O (MIO) interface and several FPGA programmable logic (PL), high-density (HD), and high-performance (HP) banks. Table 1-1 lists a summary of the resources available within the ZU7EV. A feature set overview, description, and ordering information is provided in the *Zynq UltraScale+ MPSoC Data Sheet: Overview* (DS891) [Ref 1].

Table 1-1: **Zynq UltraScale+ MPSoC ZU7EV Features and Resources**

Feature	Resource Count
HD banks	Two banks, total of 48 pins
HP banks	Six banks, total of 312 pins
MIO banks	Three banks, total of 78 pins
PS-GTR transceivers (6 Gb/s)	Four PS-GTR transceivers
GTH transceivers (16.3 Gb/s)	20 GTH transceivers
VCU	One
PCIe hard block Gen1/2/3/4 x4	Two
Logic cells	504 K
CLB flip-flops	460.8 K
Distributed RAM	6.2 Mb
Total block RAM	11 Mb
UltraRAM	27 Mb
DSP slices	1728

Board Specifications

Dimensions

Height: 7.323 inch (18.60 cm)

Length: 9.5 inch (24.13 cm)

Thickness: 0.062 inch ±0.005 inch (0.157 cm ±0.0127 cm)

Note: A 3D model of this board is not available.

IMPORTANT: *The ZCU106 board height exceeds the standard 4.376 inch (11.15 cm) height of a PCI Express® card.*

See ZCU106 board documentation for XDC listing, schematics, layout files, board outline drawings, etc.

Environmental

Temperature

Operating: 0°C to +45°C

Storage: -25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

+12 V_{DC}

Board Setup and Configuration

Board Component Location

Figure 2-1 shows the ZCU106 board component locations. Each numbered component shown in the figure is keyed to Table 2-1. Table 2-1 identifies the components, references the respective schematic (0381770) page numbers, and links to a detailed functional description of the components and board features in Chapter 3.

IMPORTANT: *Figure 2-1 is for visual reference only and might not reflect the current revision of the board.*

IMPORTANT: *There could be multiple revisions of this board. The specific details concerning the differences between revisions are not captured in this document. This document is not intended to be a reference design guide and the information herein should not be used as such. Always refer to the schematic, layout, and XDC files of the specific ZCU106 version of interest for such details.*

CAUTION! *The ZCU106 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.*

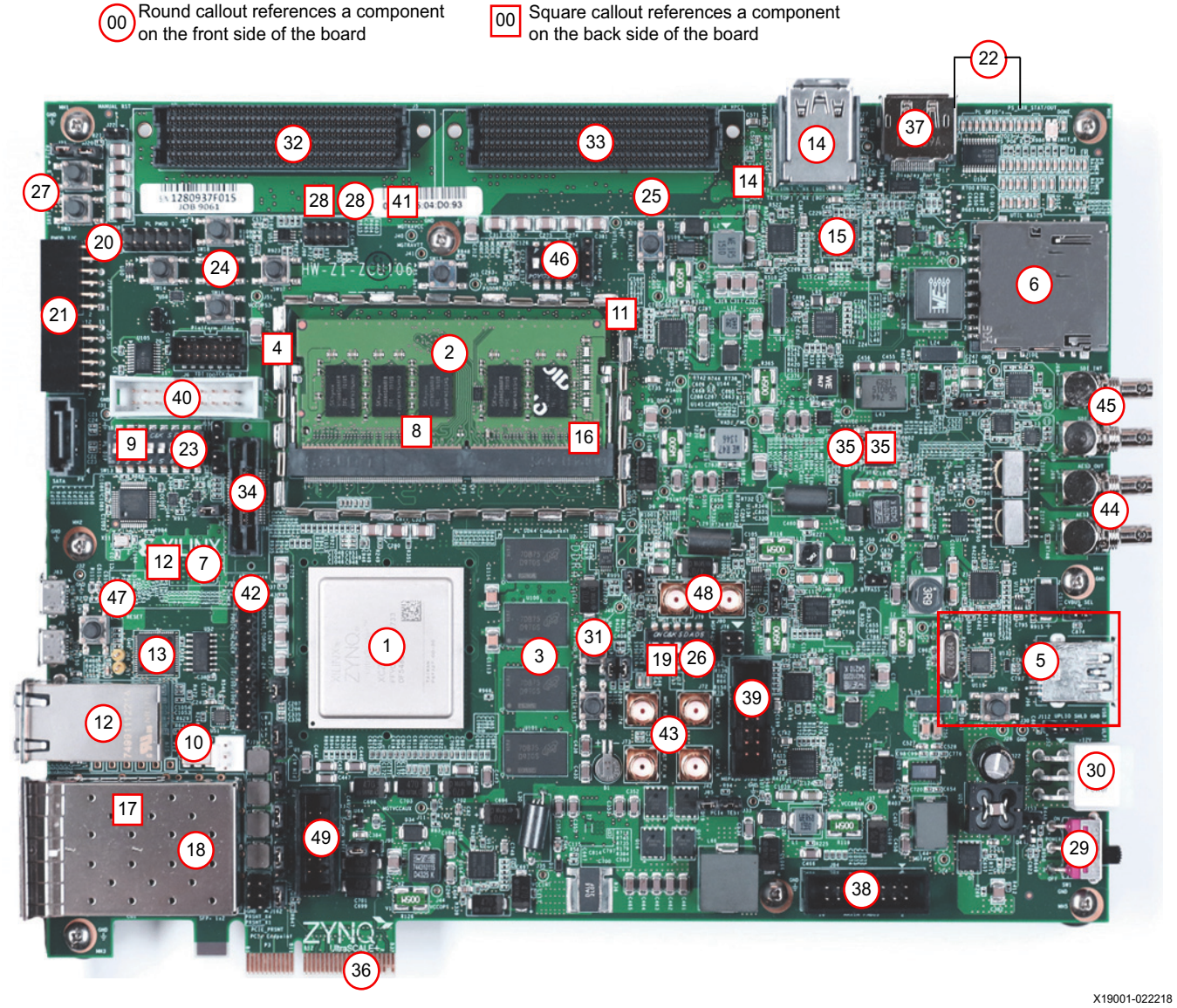


Figure 2-1: **ZCU106 Evaluation Board Components**

Table 2-1: **ZCU106 Board Component Locations**

Callout Number	Ref. Des.	Feature ([B] = bottom of board)	Notes	Schematic Page
1	U1	Zynq UltraScale+ XCZU7EV MPSoC, GTH Transceivers, PS GTR Transceivers	XCZU7EV-2FFVC1156	
2	J1	PS-Side: DDR4 SODIMM Socket	LOTESADDR0067-P001A/KINGSTON KVR21SE15S8/4	24
3	U2, U99-U101	DDR4 Component Memory, (4 Gb)	Micron MT40A256M16GE-075E	26-29
4	U119, U120	Quad SPI Flash Memory (MIO 0–12) [B]	Micron MT25QU512ABB8ESF-0SIT	53
5	U116, J96	USB 3.0 Transceiver and USB 2.0 ULPI PHY (USB 3.0 A connector)	SMSC USB3320-EZK, KYCON KMMX-AB10-SMT1SB30TR	58
6	J100	SD Card Interface	Hirose DMIAA-SF-PET(21)	54
7	U152, J2	Programmable Logic JTAG Programming Options	FTDI FT232HL-REEL, Hirose ZX62D-AB-5P8	22
8	U69	SI5341B 10 Independent Output Any-Frequency Clock Generator [B]	Silicon Labs SI5341B-B05071-GM	44
9	U42	Programmable User Clock [B]	Silicon Labs SI570BAB001614DG	45
10	U56	Programmable User MGT Clock, Cooling Fan Connector	Silicon Labs SI570BAB000544DG	45
11	U20	SFP/SFP+ Clock Recovery [B]	Silicon Labs SI5328B-C-GMR	46
12	U98, P12	GEM3 Ethernet (MIO 64-77), 10/100/1000 MHz Tri-Speed Ethernet PHY	TI DP83867IRPAP, Halo HFJ11-1G01E-L12RL	59
13	U40, J83	CP2108 USB UART Interface	Silicon Labs CP2108-B02-GM, Hirose ZX62D-AB-5P8	47
14	U94, P7	HDMI Video Output [B]	TI SN65DP159RGZ, TE Connectivity 1888811-1	40
15	U19, P7	HDMI Video Output	TI TMDS181IRGZT, TE Connectivity 1888811-1	41
16	U60, U61, U97	I2C0 (MIO 14-15), I2C0 bus switch and two expanders [B]	TI PCA9544ARGYR, Two each TI TCA6416APWR	64
17	U34, U135	I2C1 (MIO 16-17), I2C1 bus switches [B]	Two each TI TCA9548APWR	65
18	P1, P2	SFP/SFP+ Connectors	Molex 74441-0010	38-39
19	U41	TI MSP430 System Controller [B]	TI MSP430F5342	43
20	J87	User PMOD GPIO Headers	SULLINS PBC36DAAN	62
21	J160, J55	User PMOD GPIO Headers	SULLINS PPPC062LJBN-RC	56
22	DS37-DS44	User I/O, Power and Status LEDs	GPIO LEDs, GREEN 0603	60
23	SW13	User I/O DIP switch	C&K SDA08H1SBD	60

Table 2-1: **ZCU106 Board Component Locations *(Cont'd)***

Callout Number	Ref. Des.	Feature ([B] = bottom of board)	Notes	Schematic Page
24	SW14-SW18	User I/O pushbuttons	E-switch TL3301EP100QG placed in N,S,W,E,C pattern	60
25	SW20	User I/O reset pushbutton switch	E-switch TL3301EP100QG	60
26	SW8	Switches system controller DIP	5-pole C&K SDA05H1SBD	43
27	SW3, SW4	System Reset Pushbuttons	E-switch TL3301EP100QG	12
28	U122, J98	CAN1 (MIO 24-25) [B], 2X4 male header	TI SN65HVD232, SULLINS PBC36DAAN	57
29	SW1	Power On/Off Slide Switch	C&K 1201M2S3AQE2	66
30	J52	Power On/Off Slide Switch	MOLEX 39-30-1060	66
31	SW5	Program_B Pushbutton	E-switch TL3301EP100QG	12
32	J5	FPGA Mezzanine Card Interface, FMC HPC0 Connector J5	Samtec ASP_134486_01	30-33
33	J4	FPGA Mezzanine Card Interface, FMC HPC1 Connector J4	Samtec ASP_134486_01	34-37
34	P6	EMIO ARM Trace Port	MICTOR 2-5767004-2	61
35	–	Board Power System	Maxim regulators	67-92
36	P3	PCI Express Endpoint Connectivity	FCI 10061913-101CLF	48
37	P11	DisplayPort DPAUX (MIO 27-30)	MOLEX 0472720001	51-52
38	J84	Monitoring Voltage and Current	ASSMANN AWHW16G-0202-T-R	64
39	J92	Programmable Logic JTAG Programming Options	TYCO 5103308-2	43
40	J6	Programmable Logic JTAG Programming Options	ASSMANN AWHW20G-0202-T-R	23
41	U108	HDMI Clock Recovery [B]	Silicon Labs SI5324C-C-GMR	42
42	J3	Prototype Header	SULLINS PBC36DAAN	63
43	J74/J73, J72/J42	SMA, MGTH interface RX, TX SMA connectors	ROSENBERGER 32K10K-400L5	45
44	J69, J70	AES3 Audio	Samtec HDBNC–J–P–GN–RA–BH2	50
45	J10, J68	SDI Video	Samtec HDBNC–J–P–GN–RA–BH2	49
46	SW6	Switches MPSoC PS mode DIP	4-pole C&K SDA04H1SBD	12
47	SW9	Ethernet PHY Reset	E-switch TL3301EP100QG	59
48	J79/J80	User SMA MGT Clock	ROSENBERGER 32K10K-400L5	45
49	J93	SYSMON 2X6 vertical male pin header	SULLINS PBC36DAAN	3

Default Jumper and Switch Settings

Figure 2-2 shows the ZCU106 board jumper header and DIP switch locations. Each numbered component shown in the figure is keyed to Table 2-2 or Table 2-3 (for default switch settings). Both tables reference the respective schematic (0381770) page numbers.

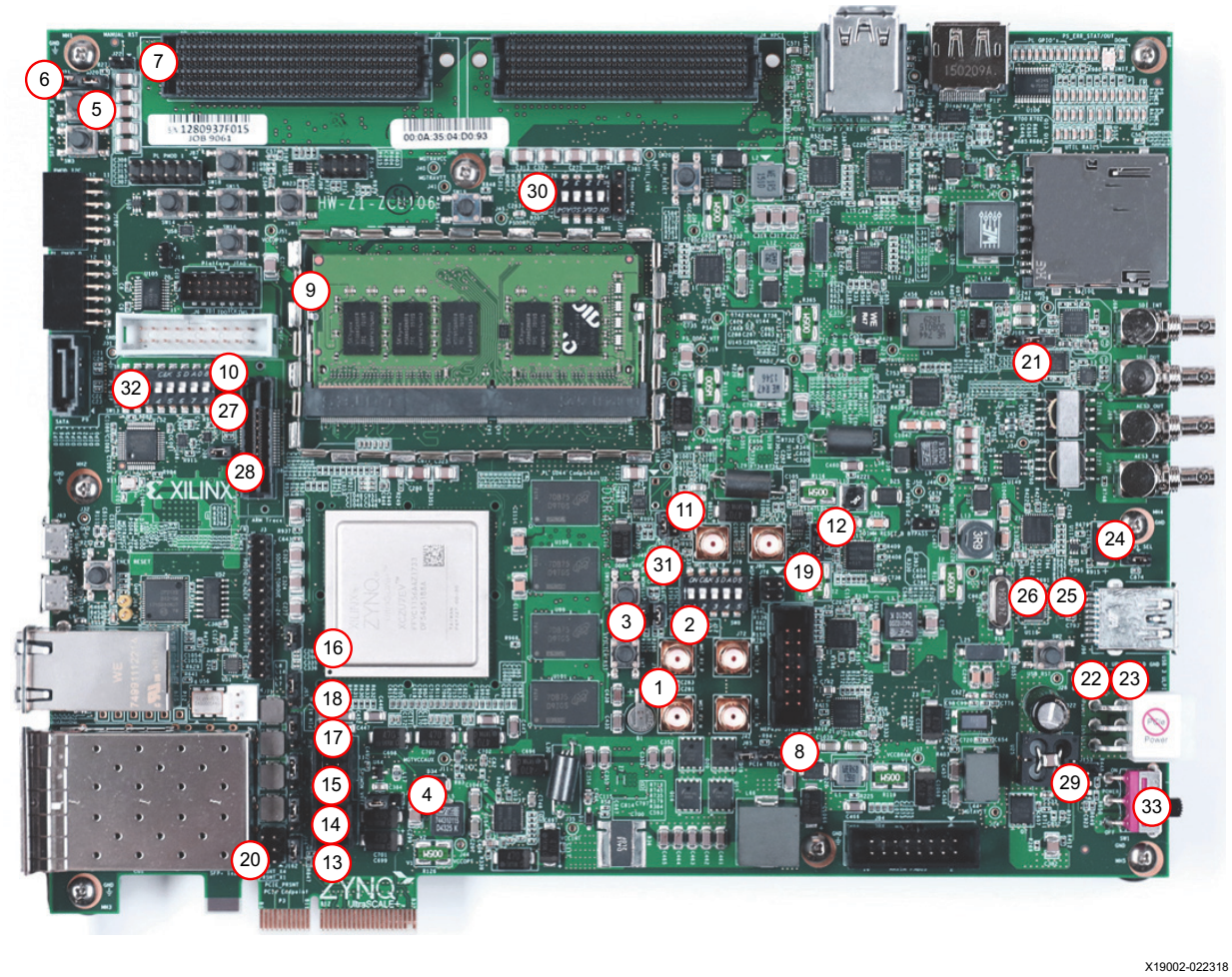


Figure 2-2: **Board Jumper Header and DIP Switch Locations**

Jumpers

Table 2-2: **Default Jumper Settings**

Number	Ref. Des.	Function	Default	Schematic Page
1	J85	POR_OVERRIDE • 1-2: Enable • 2-3: Disable	2-3	3
2	J12	SYSMON I2C address • Open: SYSMON_VP_R floating • 1-2: SYSMON_VP_P pulled down	1-2	3
3	J13	SYSMON I2C address • Open: SYSMON_VN_R floating • 1-2: SYSMON_VP_N pulled down	1-2	3
4	J90	SYSMON VREFP • 1-2:1.25V VREFP connected to FPGA • 2-3: VREFP connected to GND	1-2	3
5	J20	Reset sequencer PS_POR_B • Open: Sequencer does not control PS_POR_B • 1-2: Sequencer can control PS_POR_B	1-2	12
6	J21	Reset sequencer PS_SRST_B • Open: Sequencer does not control PS_SRST_B • 1-2: Sequencer can control PS_SRST_B	1-2	12
7	J22	Reset sequencer inhibit • Open: Sequencer normal operation • 1-2: Sequencer inhibit (resets stay asserted)	Open	12
8	J75	VCCINT_VCU power • Open: VCCINT_VCU not powered • 1-2, 3-4, 5-6: VCCINT_VCU powered	1-2 3-4 5-6	16
9	J14	ARM® debug VTREF • Open: VTREF floating • 1-2: VTREF = VCCOPS3 (1.8V)	1-2	22
10	J15	ARM debug VSUPPLY • Open: VSUPPLY floating • 1-2: VSUPPLY = VCCOPS3 (1.8V)	Open	22
11	J56	VCCO_PSDDR_504 select • 1-2: Switched DDR4 VDDQ • 3-4: Direct DDR4 VDDQ	1-2	24
12	J159	DDR4 reset suspend enable • 1-2: Suspend disabled (gate bypass) • 2-3: Suspend enabled	1-2	24

Table 2-2: **Default Jumper Settings *(Cont'd)***

Number	Ref. Des.	Function	Default	Schematic Page
13	J16	SFP0 enable	1-2	37
14	J62	SFP0 TX bandwidth • 1-2: Full bandwidth • 2-3: Low bandwidth	2-3	37
15	J63	SFP0 TX bandwidth • 1-2: Full bandwidth • 2-3: Low bandwidth	2-3	37
16	J17	SFP1 enable	1-2	38
17	J64	SFP1 TX bandwidth • 1-2: Full bandwidth • 2-3: Low bandwidth	2-3	38
18	J65	SFP1 TX bandwidth • 1-2: Full bandwidth • 2-3: Low bandwidth	2-3	38
19	J76	MSP430 programming • 1-2: Reset to GPIO • 3-4: Test to GPIO	Open	42
20	J162	PCIe PRSNT select • 1-2: x1 • 3-4: x4 • 5-6: GND • Open: card defined	Open	47
21	J108	SD level shifter internal reference • 1-2: 3.3V reference • 2-3: GND	1-2	53
22	J110	CVBUS select • 1-2: Device or OTG mode • 2-3: Host mode	1-2	57
23	J109	ID select • 1-2: Connector ID • 2-3: VDD33 ID	2-3	57
24	J112	Shield GND select • 1-2: Capacitor • 2-3: GND	1-2	57
25	J7	Device or host select • 1-2: Host/OTG • Open: Device	Open	57

Table 2-2: **Default Jumper Settings *(Cont'd)***

Number	Ref. Des.	Function	Default	Schematic Page
26	J113	Device/host or OTG select • 1-2: Device or host • 2-3: OTG	1-2	57
27	J88	ARM trace VTREF • 1-2: 3.3V • Open: 0V	Open	60
28	J38	ARM trace power • 1-2: 3.3V • Open: 0V	1-2	60
29	J153	Power inhibit • Open: Rails power on normally • 1-2: All rails (except UTIL) OFF	1-2	65

Switches

Table 2-3: **Default Switch Settings**

Number	Ref. Des.	Function	Default	Schematic Page
30	SW6 ***Note:*** For this DIP switch, in relation to the arrow, moving the switch toward the label ON is a 0. DIP switch labels 1 through 4 are equivalent to mode pins 0 through 3.	Switch PS_MODE select		12
		(ON = pull down, OFF = pull up)		
		1: PS_MODE0	On	
		2: PS_MODE1	On	
		3: PS_MODE2	On	
		4: PS_MODE3	On	
31	SW8 ***Note:*** For this DIP switch, in relation to the arrow, moving the switch toward the label ON is a 0. 1 through 5 are tied to MSP430 U41 GPIO[1:5].	MSP430 GPIO		42
		1: SW0	Off	
		2: SW1	Off	
		3: SW2	Off	
		4: SW3	Off	
		5: SW4	Off	
32	SW13	GPIO	All Off	59
33	SW1	Main power switch	Off	65

Installing the ZCU106 Board in a PC Chassis

Installation of the ZCU106 board inside a computer chassis is required when developing or testing PCI Express® functionality. When the ZCU106 board is installed in the PCIe® slot, power is provided from the ATX power supply 4-pin peripheral connector through the ATX adapter cable (Figure 2-3), which is plugged into J52 on the ZCU106 board. The Xilinx® part number for this cable is 2600304. See [Ref 25] for ordering information.

Figure 2-3: **ATX Power Supply Adapter Cable**

To install the ZCU106 board in a PC chassis:

1. On the ZCU106 board, remove the seven screws retaining the six rubber feet with their standoffs, and the PCIe bracket. Reinstall the PCIe bracket using two of the previously removed screws.
2. Power down the host computer and remove the power cord from the PC.
3. Open the PC chassis following the instructions provided with the PC.
4. Select a vacant PCIe expansion slot and remove the expansion cover (at the back of the chassis) by removing the screws on the top and bottom of the cover.

IMPORTANT: *The ZCU106 board height exceeds the standard PCIe board dimension, so the PC chassis top cover should remain off while using the ZCU106.*

5. Plug the ZCU106 board into an open PCIe expansion slot.
6. Install the top mounting bracket screw into the PC expansion cover retainer bracket to secure the ZCU106 board in its slot.
7. Connect the ATX power supply to the ZCU106 board using the ATX power supply adapter cable shown in Figure 2-3.
   a. Plug the 6-pin 2 x 3 Molex connector on the adapter cable into J52 on the ZCU106 board.
   b. Plug the 4-pin 1 x 4 peripheral power connector from the ATX power supply into the 4-pin adapter cable connector.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into the ZCU106 board power connector J52. The ATX 6-pin connector has a different pin out than J52. Connecting an ATX 6-pin connector into J52 damages the ZCU106 evaluation board and voids the board warranty.*

8. Slide the ZCU106 board power switch SW1 to the ON position. The PC can now be powered on.

MPSoC Device Configuration

Zynq UltraScale+ XCZU7EV MPSoC devices use a multi-stage boot process as described in the "Boot and Configuration" chapter of the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2]. Switch SW6 configuration option settings are listed in Table 2-4.

Table 2-4: **Switch SW6 Configuration Option Settings**

Boot Mode	Mode Pins [3:0]	Mode SW6 [4:1]
JTAG	0000	ON,ON,ON,ON
QSPI32	0010(1)	ON,ON,OFF,ON
SD	1110	OFF,OFF,OFF,ON

Notes:

1. Default switch setting.
2. For DIP SW6, in relation to the arrow, moving the switch toward the label ON is a 0. DIP switch labels 1 through 4 are equivalent to mode pins 0 through 3.

JTAG

Vivado®, SDK, or third-party tools can establish a JTAG connection to the Zynq UltraScale+ MPSoC device through one of these provided JTAG interfaces:

- Xilinx platform USB or cable PC4 connector (J8)
- ARM 20-pin JTAG connector (J6)
- FTDI FT232HL USB-to-JTAG bridge U152 with micro-USB connector (J2)

Quad SPI

To boot from the dual Quad SPI nonvolatile configuration memory:

1. Store a valid Zynq UltraScale+ MPSoC boot image in the Quad SPI flash devices connected to the MIO Quad SPI interface.
2. Set the boot mode pins SW6 [3:0] PS_MODE[3:0] as indicated in Table 2-4 for Quad SPI32.
3. Either power-cycle or press the power-on reset (POR) pushbutton. SW6 is callout 46 in Figure 2-1.

SD

To boot from an SD card:

1. Store a valid Zynq UltraScale+ MPSoC boot image file on to an SD card (plugged into SD socket J100) connected to the MIO SD interface.
2. Set the boot mode pins SW6 [3:0] PS_MODE[3:0] as indicated in Table 2-4 for SD.
3. Either power-cycle or press the power-on reset (POR) pushbutton. SW6 is callout 46 in Figure 2-1.

See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] for more information about Zynq UltraScale+ MPSoC configuration options.

Board Component Descriptions

Overview

This chapter provides a detailed functional description of the board's components and features. Table 2-1, page 14 identifies the components, references the respective schematic page numbers, and links to the corresponding detailed functional description in this chapter. Component locations are shown in Table 2-1, page 14.

Component Descriptions

Zynq UltraScale+ XCZU7EV MPSoC

[Figure 2-1, callout 1]

The ZCU106 board is populated with the Zynq UltraScale+ XCZU7EV-2FFVC1156 MPSoC, which combines a powerful processing system (PS) and programmable logic (PL) in the same device. The PS in a Zynq UltraScale+ MPSoC features the ARM® flagship Cortex®-A53 64-bit quad-core processor and Cortex-R5 dual-core real-time processor.

Production ZCU106 evaluation boards will ship with -2 speed grade devices. Support of multiple speed grades requires voltage adjustments.

The V_{CCINT} supplies are user adjustable via the PMBus with the voltage ranges listed in Table 3-1 to support multiple Zynq UltraScale+ MPSoC speed grades.

Table 3-1: **Recommended Operating Conditions**

Symbol	Description	Min	Typ	Max	Units
Processing System					
$V_{CC\_PSINTFP}$	PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS full-power domain supply voltage.	0.873	0.900	0.927	V
$V_{CC\_PSINTLP}$	PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS low-power domain supply voltage.	0.873	0.900	0.927	V
Programmable Logic					
V_{CCINT}	PL internal supply voltage.	0.825	0.850	0.876	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PL internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: PL internal supply voltage.	0.873	0.900	0.927	V

The top-level block diagram is shown in Figure 3-1.

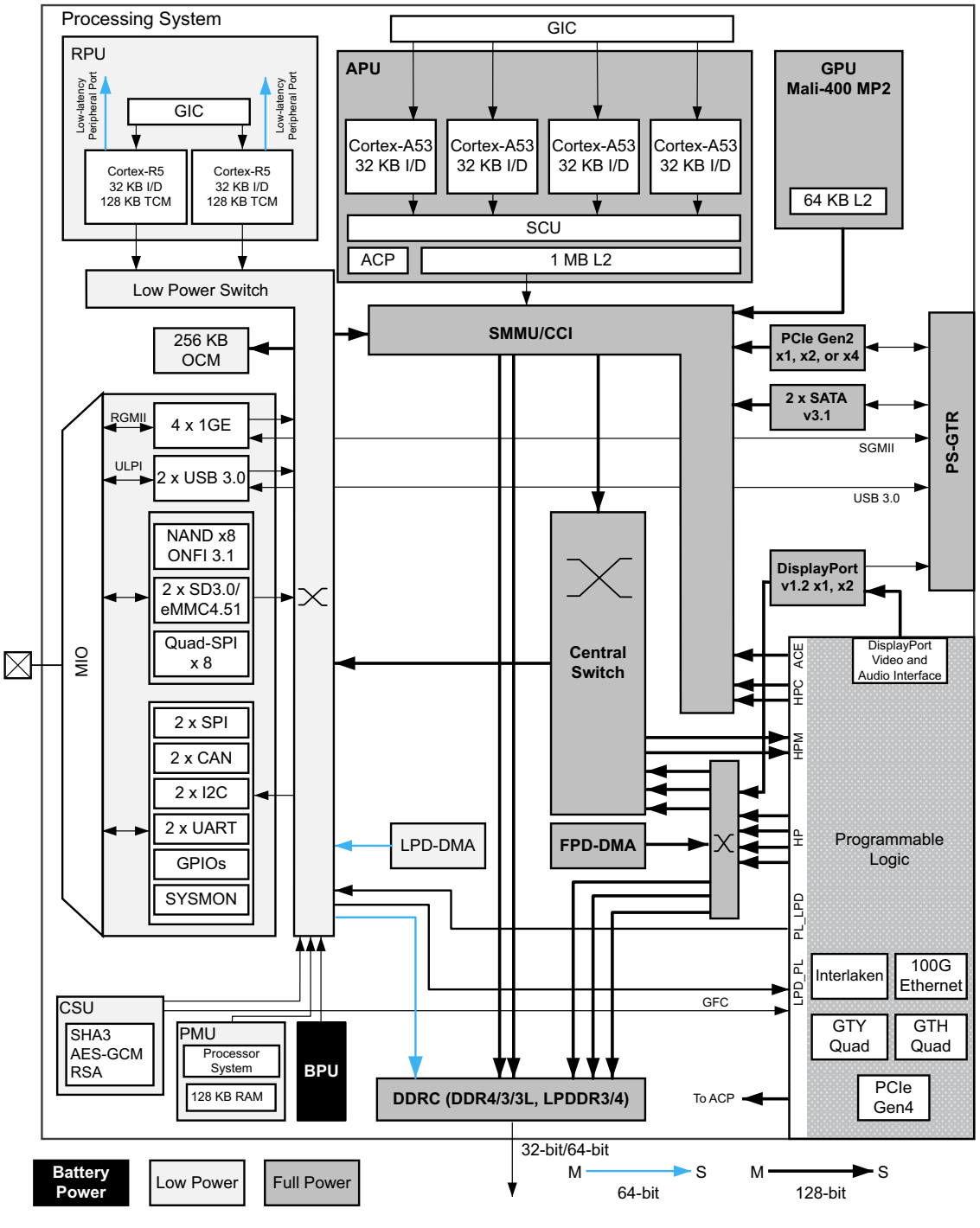


Figure 3-1: **Top-Level Block Diagram**

The Zynq UltraScale+ MPSoC PS block has three major processing units:

- Cortex-A53 application processing unit (APU)-ARM v8 architecture-based 64-bit quad-core multiprocessing CPU.
- Cortex-R5 real-time processing unit (RPU)-ARM v7 architecture-based 32-bit dual real-time processing unit with dedicated tightly coupled memory (TCM).
- Mali-400 graphics processing unit (GPU)-graphics processing unit with pixel and geometry processor and 64 KB L2 cache.

The Zynq UltraScale+ MPSoC PS has four high-speed serial I/O (HSSIO) interfaces supporting these protocols:

- Integrated block for PCI Express® interface-PCIe™ base specification version 2.1 compliant.
- SATA 3.1 specification compliant interface.
- DisplayPort interface-implements a DisplayPort source-only interface with video resolution up to 4K x 2K-30 (300 MHz pixel rate).
- USB 3.0 interface-compliant to USB 3.0 specification implementing a 5 Gb/s line rate.
- Serial GMII interface-supports a 1 Gb/s SGMII interface.

The PS and PL can be coupled with multiple interfaces and other signals to effectively integrate user-created hardware accelerators and other functions in the PL logic that are accessible to the processors. They can also access memory resources in the PS. The PS I/O peripherals, including the static/flash memory interfaces share a multiplexed I/O (MIO) of up to 78 MIO pins. Zynq UltraScale+ MPSoCs can also use the I/O in the PL domain for many of the PS I/O peripherals. This is done through an extended multiplexed I/O interface (EMIO).and boots at power-up or reset.

For additional information on Zynq UltraScale+ MPSoC devices, see the *Zynq UltraScale+ MPSoC Data Sheet: Overview* (DS891) [Ref 1]. See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] for more information about Zynq UltraScale+ MPSoC configuration options.

Encryption Key Battery Backup Circuit

The XCZU7EV MPSoC U1 implements bit stream encryption key technology. The ZCU106 board provides the encryption key backup battery circuit shown in Figure 3-2.

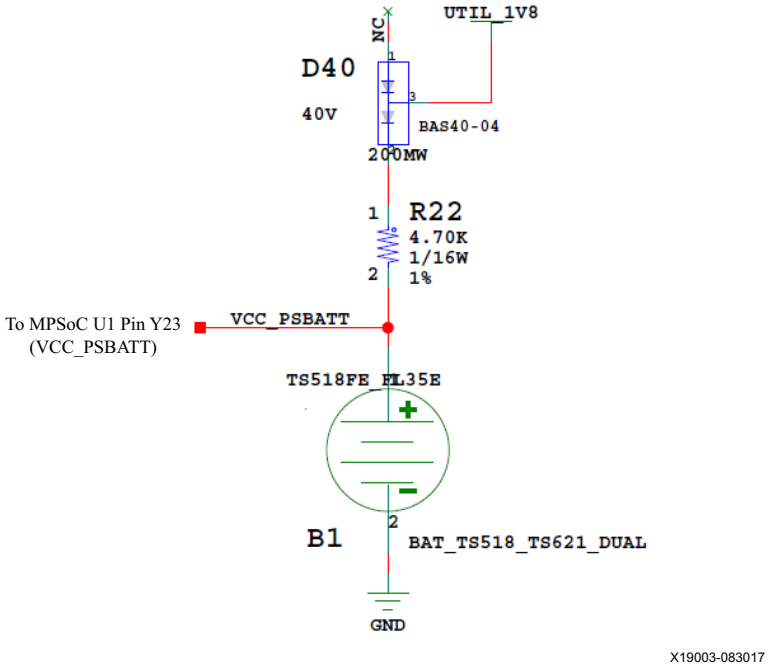


Figure 3-2: **Encryption Key Backup Circuit**

The Seiko TS518FE rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XCZU7EV MPSoC U1 V_{CC_PSBATT} pin Y23. The battery supply current I_{BATT} specification is 150 nA maximum when board power is off. B1 is charged from the UTIL_1V8 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and 4.7 ΩK current limit resistor. The nominal charging voltage is 1.42V.

On MPSoC devices, the encryption key battery is also used for the battery-backed RAM and the real-time clock (RTC) supply voltage. See *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925) [Ref 11].

I/O Voltage Rails

The XCZU7EV MPSoC PL I/O bank voltages on the ZCU106 board are listed in Figure 3-2.

Table 3-2: **I/O Voltage Rails**

XCZU7EV	Power Net Name	Voltage	Connected To
PL Bank 28	V_{ADJ_FMC}(1)	1.8V	FMC_HPC1 LA BUS, PMOD0
PL Bank 64	V_{CC1V2}	1.2V	DDR4 DQ[0:31]
PL Bank 65	V_{CC1V2}	1.2V	DDR4 DQ[32:63]
PL Bank 66	V_{CC1V2}	1.2V	DDR4 ADDR/CTRL, GPIO LED, GPIO SW, PMOD1
PL Bank 67	V_{ADJ_FMC}(1)	1.8V	FMC_HPC0 LA BUS, GPIO DIP SW
PL Bank 68	V_{ADJ_FMC}(1)	1.8V	FMC_HPC0 LA BUS, SFP REC CLOCK
PL Bank 87	V_{CC3V3}	3.3V	HDMI, MSP430 GPIO
PL Bank 88	V_{CC3V3}	3.3V	TRACE DEBUG CONNECTOR
PS Bank 500	V_{CCOPS}	1.8V	CAN, UART0/1, I2C0/1, QSPI LWR/UPR
PS Bank 501	V_{CCOPS}	1.8V	SDIO, PMU_GPO[0:5], DP
PS Bank 502	V_{CCOPS}	1.8V	ENET, USB_DATA[0:7], USB_CTRL
PS Bank 503	V_{CCOPS3}	1.8V	PS CONFIG I/F
PS Bank 504	$V_{CCO\_PSDDR\_504}$	1.2V	DDR4 72-BIT SODIMM I/F

Notes:

1. The ZCU106 board is shipped with V_{ADJ_FMC} set to 1.8V by the MSP430 system controller.

PS-Side: DDR4 SODIMM Socket

[Figure 2-1, callout 2]

The PS-side memory is wired to the Zynq UltraScale+ DDRC bank 504 hard memory controller. A 64-bit single rank DDR4 SODIMM with ECC (72-bit) is inserted into socket J1. The ZCU106 is shipped with a DDR4 SODIMM installed:

- Manufacturer: Kingston
- Part Number: KVR21SE15S8/4
- Description:
  - 4 GByte DDR4 SODIMM
  - Single rank x8
  - 512 Mbit x 72-Bit
  - PC4-2133 260-Pin

The ZCU106 supports full power-off suspend mode where only the system controller and the PS-side DDR4 SODIMM memory are powered. The DDR4 memory is kept in a self-refresh state and has its reset input controlled by the system controller such that the memory is not reset when waking-up from suspend mode. DDR4 SODIMM socket J1 connections are listed in Table 3-3.

Table 3-3: **DDR4 SODIMM Socket J1 Connections to FPGA PS DDR Bank 504**

XCZU7EV (U1) Pin	Net Name	DDR4 SODIMM Memory J1	
		Pin Number	Pin Name
AN34	DDR4_SODIMM_A0	144	A0
AM34	DDR4_SODIMM_A1	133	A1
AM33	DDR4_SODIMM_A2	132	A2
AL34	DDR4_SODIMM_A3	131	A3
AL33	DDR4_SODIMM_A4	128	A4
AK33	DDR4_SODIMM_A5	126	A5
AK30	DDR4_SODIMM_A6	127	A6
AJ30	DDR4_SODIMM_A7	122	A7
AJ31	DDR4_SODIMM_A8	125	A8
AH31	DDR4_SODIMM_A9	121	A9
AG31	DDR4_SODIMM_A10	146	A10/AP
AF31	DDR4_SODIMM_A11	120	A11
AG30	DDR4_SODIMM_A12	119	A12
AF30	DDR4_SODIMM_A13	158	A13
AE27	DDR4_SODIMM_BA0	150	BA0
AE28	DDR4_SODIMM_BA1	145	BA1
AD27	DDR4_SODIMM_BG0	115	BG0
AF27	DDR4_SODIMM_BG1	113	BG1
AP27	DDR4_SODIMM_DQ0	8	DQ0
AP25	DDR4_SODIMM_DQ1	7	DQ1
AP26	DDR4_SODIMM_DQ2	20	DQ2
AM26	DDR4_SODIMM_DQ3	21	DQ3
AP24	DDR4_SODIMM_DQ4	4	DQ4
AL25	DDR4_SODIMM_DQ5	3	DQ5
AM25	DDR4_SODIMM_DQ6	16	DQ6
AM24	DDR4_SODIMM_DQ7	17	DQ7
AM28	DDR4_SODIMM_DQ8	28	DQ8
AN28	DDR4_SODIMM_DQ9	29	DQ9
AP29	DDR4_SODIMM_DQ10	41	DQ10

Table 3-3: **DDR4 SODIMM Socket J1 Connections to FPGA PS DDR Bank 504 *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	DDR4 SODIMM Memory J1	
		Pin Number	Pin Name
AP28	DDR4_SODIMM_DQ11	42	DQ11
AM31	DDR4_SODIMM_DQ12	24	DQ12
AP31	DDR4_SODIMM_DQ13	25	DQ13
AN31	DDR4_SODIMM_DQ14	38	DQ14
AM30	DDR4_SODIMM_DQ15	37	DQ15
AF25	DDR4_SODIMM_DQ16	50	DQ16
AG25	DDR4_SODIMM_DQ17	49	DQ17
AG26	DDR4_SODIMM_DQ18	62	DQ18
AJ25	DDR4_SODIMM_DQ19	63	DQ19
AG24	DDR4_SODIMM_DQ20	46	DQ20
AK25	DDR4_SODIMM_DQ21	45	DQ21
AJ24	DDR4_SODIMM_DQ22	58	DQ22
AK24	DDR4_SODIMM_DQ23	59	DQ23
AH28	DDR4_SODIMM_DQ24	70	DQ24
AH27	DDR4_SODIMM_DQ25	71	DQ25
AJ27	DDR4_SODIMM_DQ26	83	DQ26
AK27	DDR4_SODIMM_DQ27	84	DQ27
AL26	DDR4_SODIMM_DQ28	66	DQ28
AL27	DDR4_SODIMM_DQ29	67	DQ29
AH29	DDR4_SODIMM_DQ30	79	DQ30
AL28	DDR4_SODIMM_DQ31	80	DQ31
AB29	DDR4_SODIMM_DQ32	174	DQ32
AB30	DDR4_SODIMM_DQ33	173	DQ33
AC29	DDR4_SODIMM_DQ34	187	DQ34
AD32	DDR4_SODIMM_DQ35	186	DQ35
AC31	DDR4_SODIMM_DQ36	170	DQ36
AE30	DDR4_SODIMM_DQ37	169	DQ37
AC28	DDR4_SODIMM_DQ38	183	DQ38
AE29	DDR4_SODIMM_DQ39	182	DQ39
AC27	DDR4_SODIMM_DQ40	195	DQ40
AA27	DDR4_SODIMM_DQ41	194	DQ41
AA28	DDR4_SODIMM_DQ42	207	DQ42
AB28	DDR4_SODIMM_DQ43	208	DQ43
W27	DDR4_SODIMM_DQ44	191	DQ44

Table 3-3: **DDR4 SODIMM Socket J1 Connections to FPGA PS DDR Bank 504 *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	DDR4 SODIMM Memory J1	
		Pin Number	Pin Name
W29	DDR4_SODIMM_DQ45	190	DQ45
W28	DDR4_SODIMM_DQ46	203	DQ46
V27	DDR4_SODIMM_DQ47	204	DQ47
AA32	DDR4_SODIMM_DQ48	216	DQ48
AA33	DDR4_SODIMM_DQ49	215	DQ49
AA34	DDR4_SODIMM_DQ50	228	DQ50
AE34	DDR4_SODIMM_DQ51	229	DQ51
AD34	DDR4_SODIMM_DQ52	211	DQ52
AB31	DDR4_SODIMM_DQ53	212	DQ53
AC34	DDR4_SODIMM_DQ54	224	DQ54
AC33	DDR4_SODIMM_DQ55	225	DQ55
AA30	DDR4_SODIMM_DQ56	237	DQ56
Y30	DDR4_SODIMM_DQ57	236	DQ57
AA31	DDR4_SODIMM_DQ58	249	DQ58
W30	DDR4_SODIMM_DQ59	250	DQ59
Y33	DDR4_SODIMM_DQ60	232	DQ60
W33	DDR4_SODIMM_DQ61	233	DQ61
W34	DDR4_SODIMM_DQ62	245	DQ62
Y34	DDR4_SODIMM_DQ63	246	DQ63
AF32	DDR4_SODIMM_CB0	92	CB0/NC
AE32	DDR4_SODIMM_CB1	91	CB1/NC
AH33	DDR4_SODIMM_CB2	101	CB2/NC
AE33	DDR4_SODIMM_CB3	105	CB3/NC
AF33	DDR4_SODIMM_CB4	88	CB4/NC
AH34	DDR4_SODIMM_CB5	87	CB5/NC
AJ34	DDR4_SODIMM_CB6	100	CB6/NC
AK34	DDR4_SODIMM_CB7	104	CB7/NC
AN24	DDR4_SODIMM_DM0_B	12	DM0_N/DBI0_N
AM29	DDR4_SODIMM_DM1_B	33	DM1_N/DBI1_N
AH24	DDR4_SODIMM_DM2_B	54	DM2_N/DBI2_N
AJ29	DDR4_SODIMM_DM3_B	75	DM3_N/DBI3_N
AD29	DDR4_SODIMM_DM4_B	178	DM4_N/DBI4_N
Y29	DDR4_SODIMM_DM5_B	199	DM5_N/DBI5_N
AC32	DDR4_SODIMM_DM6_B	220	DM6_N/DBI6_N

Table 3-3: **DDR4 SODIMM Socket J1 Connections to FPGA PS DDR Bank 504 *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	DDR4 SODIMM Memory J1	
		Pin Number	Pin Name
Y32	DDR4_SODIMM_DM7_B	241	DM7_N/DBI7_N
AF34	DDR4_SODIMM_DM8_B	96	DM8_N/DBI8_N/NC
AN26	DDR4_SODIMM_DQS0_T	13	DQS0_T
AN27	DDR4_SODIMM_DQS0_C	11	DQS0_C
AN29	DDR4_SODIMM_DQS1_T	34	DQS1_T
AP30	DDR4_SODIMM_DQS1_C	32	DQS1_C
AH26	DDR4_SODIMM_DQS2_T	55	DQS2_T
AJ26	DDR4_SODIMM_DQS2_C	53	DQS2_C
AK28	DDR4_SODIMM_DQS3_T	76	DQS3_T
AK29	DDR4_SODIMM_DQS3_C	74	DQS3_C
AD30	DDR4_SODIMM_DQS4_T	179	DQS4_T
AD31	DDR4_SODIMM_DQS4_C	177	DQS4_C
Y27	DDR4_SODIMM_DQS5_T	200	DQS5_T
Y28	DDR4_SODIMM_DQS5_C	198	DQS5_C
AB33	DDR4_SODIMM_DQS6_T	221	DQS6_T
AB34	DDR4_SODIMM_DQS6_C	219	DQS6_C
W31	DDR4_SODIMM_DQS7_T	242	DQS7_T
W32	DDR4_SODIMM_DQS7_C	240	DQS7_C
AG33	DDR4_SODIMM_DQS8_T	97	DQS8_T
AG34	DDR4_SODIMM_DQS8_C	95	DQS8_C
AL31	DDR4_SODIMM_CK0_C	139	CK0_C
AN32	DDR4_SODIMM_CK0_T	137	CK0_T
AL30	DDR4_SODIMM_CK1_C	140	CK1_C/NF
AL32	DDR4_SODIMM_CK1_T	138	CK1_T/NF
AN33	DDR4_SODIMM_CKE0	109	CKE0
AH32	DDR4_SODIMM_CKE1	110	CKE1
AP32	DDR4_SODIMM_ODT0	155	ODT0
AJ32	DDR4_SODIMM_ODT1	161	ODT1
AF28	DDR4_SODIMM_RAS_B	152	RAS_N/A16
AG28	DDR4_SODIMM_CAS_B	156	CAS_N/A15
AG29	DDR4_SODIMM_WE_B	151	WE_N/A14
AE25	DDR4_SODIMM_ACT_B	114	ACT_N
AB26	DDR4_SODIMM_ALERT_B	116	ALERT_N
AA26	DDR4_SODIMM_PARITY	143	PARITY

Table 3-3: **DDR4 SODIMM Socket J1 Connections to FPGA PS DDR Bank 504 *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	DDR4 SODIMM Memory J1	
		Pin Number	Pin Name
AP33	DDR4_SODIMM_CS0_B	149	CS0_N
AK32	DDR4_SODIMM_CS1_B	157	CS1_N

The ZCU106 DDR4 SODIMM interface adheres to the constraints guidelines documented in the "PCB Guidelines for DDR4" section of the *UltraScale Architecture PCB Design Guide* (UG583) [Ref 3]. The DDR4 SODIMM interface is a 40Ω impedance implementation. Other memory interface details are also available in the *UltraScale Architecture FPGAs Memory Interface Solutions Guide* (PG150) [Ref 4].

DDR4 Component Memory

[Figure 2-1, callout 2]

The 2 GB 64-bit wide DDR4 memory system is comprised of four 256 Mb x 16 SDRAMs (Micron MT40A256M16GE-075E) U2 and 99–101. This memory system is connected to PL-side XCZU7EV banks 64, 65, and 66. The DDR4 0.6V VTT termination voltage is supplied from sink-source regulator U35. The connections between the DDR4 memory and the XCZU7EV device are listed in Table 3-4.

Table 3-4: **DDR4 Component Memory Connection to the XCZU7EV MPSoC**

XCZU7EV (U1) Pin	Net Name	I/O Standard	DDR4 Component Memory		
			Pin #	Pin Name	Ref. Des.
AF16	DDR4_DQ0	POD12_DCI	G2	DQL0	U101
AF18	DDR4_DQ1	POD12_DCI	F7	DQL1	U101
AG15	DDR4_DQ2	POD12_DCI	H3	DQL2	U101
AF17	DDR4_DQ3	POD12_DCI	H7	DQL3	U101
AF15	DDR4_DQ4	POD12_DCI	H2	DQL4	U101
AG18	DDR4_DQ5	POD12_DCI	H8	DQL5	U101
AG14	DDR4_DQ6	POD12_DCI	J3	DQL6	U101
AE17	DDR4_DQ7	POD12_DCI	J7	DQL7	U101
AA14	DDR4_DQ8	POD12_DCI	A3	DQU0	U101
AC16	DDR4_DQ9	POD12_DCI	B8	DQU1	U101
AB15	DDR4_DQ10	POD12_DCI	C3	DQU2	U101
AD16	DDR4_DQ11	POD12_DCI	C7	DQU3	U101
AB16	DDR4_DQ12	POD12_DCI	C2	DQU4	U101
AC17	DDR4_DQ13	POD12_DCI	C8	DQU5	U101
AB14	DDR4_DQ14	POD12_DCI	D3	DQU6	U101

Table 3-4: **DDR4 Component Memory Connection to the XCZU7EV MPSoC *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	I/O Standard	DDR4 Component Memory		
			Pin #	Pin Name	Ref. Des.
AD17	DDR4_DQ15	POD12_DCI	D7	DQU7	U101
AH14	DDR4_DQS0_T	DIFF_POD12_DCI	G3	DQSL_T	U101
AJ14	DDR4_DQS0_C	DIFF_POD12_DCI	F3	DQSL_C	U101
AA16	DDR4_DQS1_T	DIFF_POD12_DCI	B7	DQSU_T	U101
AA15	DDR4_DQS1_C	DIFF_POD12_DCI	A7	DQSU_C	U101
AH18	DDR4_DM0	POD12_DCI	E7	DML_B/DBIL_B	U101
AD15	DDR4_DM1	POD12_DCI	E2	DMU_B/DBIU_B	U101
AJ16	DDR4_DQ16	POD12_DCI	G2	DQL0	U99
AJ17	DDR4_DQ17	POD12_DCI	F7	DQL1	U99
AL15	DDR4_DQ18	POD12_DCI	H3	DQL2	U99
AK17	DDR4_DQ19	POD12_DCI	H7	DQL3	U99
AJ15	DDR4_DQ20	POD12_DCI	H2	DQL4	U99
AK18	DDR4_DQ21	POD12_DCI	H8	DQL5	U99
AL16	DDR4_DQ22	POD12_DCI	J3	DQL6	U99
AL18	DDR4_DQ23	POD12_DCI	J7	DQL7	U99
AP13	DDR4_DQ24	POD12_DCI	A3	DQU0	U99
AP16	DDR4_DQ25	POD12_DCI	B8	DQU1	U99
AP15	DDR4_DQ26	POD12_DCI	C3	DQU2	U99
AN16	DDR4_DQ27	POD12_DCI	C7	DQU3	U99
AN13	DDR4_DQ28	POD12_DCI	C2	DQU4	U99
AM18	DDR4_DQ29	POD12_DCI	C8	DQU5	U99
AN17	DDR4_DQ30	POD12_DCI	D3	DQU6	U99
AN18	DDR4_DQ31	POD12_DCI	D7	DQU7	U99
AK15	DDR4_DQS2_T	DIFF_POD12_DCI	G3	DQSL_T	U99
AK14	DDR4_DQS2_C	DIFF_POD12_DCI	F3	DQSL_C	U99
AM14	DDR4_DQS3_T	DIFF_POD12_DCI	B7	DQSU_T	U99
AN14	DDR4_DQS3_C	DIFF_POD12_DCI	A7	DQSU_C	U99
AM16	DDR4_DM2	POD12_DCI	E7	DML_B/DBIL_B	U99
AP18	DDR4_DM3	POD12_DCI	E2	DMU_B/DBIU_B	U99
AB19	DDR4_DQ32	POD12_DCI	G2	DQL0	U100
AD19	DDR4_DQ33	POD12_DCI	F7	DQL1	U100
AC18	DDR4_DQ34	POD12_DCI	H3	DQL2	U100
AC19	DDR4_DQ35	POD12_DCI	H7	DQL3	U100
AA20	DDR4_DQ36	POD12_DCI	H2	DQL4	U100

Table 3-4: **DDR4 Component Memory Connection to the XCZU7EV MPSoC *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	I/O Standard	DDR4 Component Memory		
			Pin #	Pin Name	Ref. Des.
AE20	DDR4_DQ37	POD12_DCI	H8	DQL5	U100
AA19	DDR4_DQ38	POD12_DCI	J3	DQL6	U100
AD20	DDR4_DQ39	POD12_DCI	J7	DQL7	U100
AF22	DDR4_DQ40	POD12_DCI	A3	DQU0	U100
AH21	DDR4_DQ41	POD12_DCI	B8	DQU1	U100
AG19	DDR4_DQ42	POD12_DCI	C3	DQU2	U100
AG21	DDR4_DQ43	POD12_DCI	C7	DQU3	U100
AE24	DDR4_DQ44	POD12_DCI	C2	DQU4	U100
AG20	DDR4_DQ45	POD12_DCI	C8	DQU5	U100
AE23	DDR4_DQ46	POD12_DCI	D3	DQU6	U100
AF21	DDR4_DQ47	POD12_DCI	D7	DQU7	U100
AA18	DDR4_DQS4_T	DIFF_POD12_DCI	G3	DQSL_T	U100
AB18	DDR4_DQS4_C	DIFF_POD12_DCI	F3	DQSL_C	U100
AF23	DDR4_DQS5_T	DIFF_POD12_DCI	B7	DQSU_T	U100
AG23	DDR4_DQS5_C	DIFF_POD12_DCI	A7	DQSU_C	U100
AE18	DDR4_DM4	POD12_DCI	E7	DML_B/DBIL_B	U100
AH22	DDR4_DM5	POD12_DCI	E2	DMU_B/DBIU_B	U100
AL22	DDR4_DQ48	POD12_DCI	G2	DQL0	U100
AJ22	DDR4_DQ49	POD12_DCI	F7	DQL1	U2
AL23	DDR4_DQ50	POD12_DCI	H3	DQL2	U2
AJ21	DDR4_DQ51	POD12_DCI	H7	DQL3	U2
AK20	DDR4_DQ52	POD12_DCI	H2	DQL4	U2
AJ19	DDR4_DQ53	POD12_DCI	H8	DQL5	U2
AK19	DDR4_DQ54	POD12_DCI	J3	DQL6	U2
AJ20	DDR4_DQ55	POD12_DCI	J7	DQL7	U2
AP22	DDR4_DQ56	POD12_DCI	A3	DQU0	U2
AN22	DDR4_DQ57	POD12_DCI	B8	DQU1	U2
AP21	DDR4_DQ58	POD12_DCI	C3	DQU2	U2
AP23	DDR4_DQ59	POD12_DCI	C7	DQU3	U2
AM19	DDR4_DQ60	POD12_DCI	C2	DQU4	U2
AM23	DDR4_DQ61	POD12_DCI	C8	DQU5	U2
AN19	DDR4_DQ62	POD12_DCI	D3	DQU6	U2
AN23	DDR4_DQ63	POD12_DCI	D7	DQU7	U2
AK22	DDR4_DQS6_T	DIFF_POD12_DCI	G3	DQSL_T	U2

Table 3-4: **DDR4 Component Memory Connection to the XCZU7EV MPSoC *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	I/O Standard	DDR4 Component Memory		
			Pin #	Pin Name	Ref. Des.
AK23	DDR4_DQS6_C	DIFF_POD12_DCI	F3	DQSL_C	U2
AM21	DDR4_DQS7_T	DIFF_POD12_DCI	B7	DQSU_T	U2
AN21	DDR4_DQS7_C	DIFF_POD12_DCI	A7	DQSU_C	U2
AL20	DDR4_DM6	POD12_DCI	E7	DML_B/DBIL_B	U2
AP19	DDR4_DM7	POD12_DCI	E2	DMU_B/DBIU_B	U2
AK9	DDR4_A0	SSTL12_DCI	P3	A0	U2,U99-U101
AG11	DDR4_A1	SSTL12_DCI	P7	A1	U2,U99-U101
AJ10	DDR4_A2	SSTL12_DCI	R3	A2	U2,U99-U101
AL8	DDR4_A3	SSTL12_DCI	N7	A3	U2,U99-U101
AK10	DDR4_A4	SSTL12_DCI	N3	A4	U2,U99-U101
AH8	DDR4_A5	SSTL12_DCI	P8	A5	U2,U99-U101
AJ9	DDR4_A6	SSTL12_DCI	P2	A6	U2,U99-U101
AG8	DDR4_A7	SSTL12_DCI	R8	A7	U2,U99-U101
AH9	DDR4_A8	SSTL12_DCI	R2	A8	U2,U99-U101
AG10	DDR4_A9	SSTL12_DCI	R7	A9	U2,U99-U101
AH13	DDR4_A10	SSTL12_DCI	M3	A10/AP	U2,U99-U101
AG9	DDR4_A11	SSTL12_DCI	T2	A11	U2,U99-U101
AM13	DDR4_A12	SSTL12_DCI	M7	A12/BC_B	U2,U99-U101
AF8	DDR4_A13	SSTL12_DCI	T8	A13	U2,U99-U101
AK8	DDR4_BA0	SSTL12_DCI	N2	BA0	U2,U99-U101
AL12	DDR4_BA1	SSTL12_DCI	N8	BA1	U2,U99-U101
AE14	DDR4_BG0	SSTL12_DCI	M2	BG0	U2,U99-U101
AC12	DDR4_A14_WE_B	SSTL12_DCI	L2	WE_B/A14	U2,U99-U101
AF11	DDR4_A16_RAS_B	SSTL12_DCI	L8	RAS_B/A16	U2,U99-U101
AE12	DDR4_A15_CAS_B	SSTL12_DCI	M8	CAS_B_A15	U2,U99-U101
AH11	DDR4_CK_T	DIFF_SSTL12_DCI	K7	CK_T	U2,U99-U101
AJ11	DDR4_CK_C	DIFF_SSTL12_DCI	K8	CK_C	U2,U99-U101
AB13	DDR4_CKE	SSTL12_DCI	K2	CKE	U2,U99-U101
AD14	DDR4_ACT_B	SSTL12_DCI	L3	ACT_B	U2,U99-U101
R156 P/D	DDR4_TEN	SSTL12_DCI	N9	TEN	U2,U99-U101
R499 P/U	DDR4_ALERT_B	SSTL12_DCI	P9	ALERT_B	U2,U99-U101
AC13	DDR4_PAR	SSTL12_DCI	T3	PAR	U2,U99-U101
AF12	DDR4_RESET_B	LVCMOS12	P1	RESET_B	U2,U99-U101

Table 3-4: **DDR4 Component Memory Connection to the XCZU7EV MPSoC *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	I/O Standard	DDR4 Component Memory		
			Pin #	Pin Name	Ref. Des.
AF10	DDR4_ODT	SSTL12_DCI	K3	ODT	U2,U99-U101
AD12	DDR4_CS_B	SSTL12_DCI	L7	CS_B	U2,U99-U101

The ZCU106 board DDR4 64-bit component memory interface adheres to the constraints guidelines documented in the "PCB Guidelines for DDR4" section of *UltraScale Architecture PCB Design User Guide* (UG583)[Ref 3]. The ZCU106 DDR4 component interface is a 40Ω impedance implementations. Other memory interface details are also available in the *UltraScale Architecture FPGAs Memory Interface Solutions Product Guide* (PG150) [Ref 4]. For more details, see the Micron MT40A256M16GE-075E data sheet at the Micron website [Ref 15].

PSMIO

Table 3-5 provides PS MIO peripheral mapping implemented on the ZCU106 board. See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] for more information on PS MIO peripheral mapping.

Table 3-5: **MIO Peripheral Mapping**

MIO[0:25] Bank 500		MIO[26:51] Bank 501		MIO[52:77] Bank 502	
0	QSPI	26	PMU IN	52	USB0
1	QSPI	27	DPAUX	53	USB0
2	QSPI	28	DPAUX	54	USB0
3	QSPI	29	DPAUX	55	USB0
4	QSPI	30	DPAUX	56	USB0
5	QSPI	31	Not assigned/no connect	57	USB0
6	Not assigned/no connect	32	PMU OUT	58	USB0
7	QSPI	33	PMU OUT	59	USB0
8	QSPI	34	PMU OUT	60	USB0
9	QSPI	35	PMU OUT	61	USB0
10	QSPI	36	PMU OUT	62	USB0
11	QSPI	37	PMU OUT	63	USB0
12	QSPI	38	GPIO	64	GEM3
13	GPIO	39	SD1	65	GEM3
14	I2C0	40	SD1	66	GEM3
15	I2C0	41	SD1	67	GEM3
16	I2C1	42	SD1	68	GEM3
17	I2C1	43		69	GEM3

Table 3-5: **MIO Peripheral Mapping *(Cont'd)***

MIO[0:25] Bank 500		MIO[26:51] Bank 501		MIO[52:77] Bank 502	
18	UART0	44	SD1	70	GEM3
19	UART0	45	SD1	71	GEM3
20	UART1	46	SD1	72	GEM3
21	UART1	47	SD1	73	GEM3
22	GPIO	48	SD1	74	GEM3
23	GPIO	49	SD1	75	GEM3
24	CAN1	50	SD1	76	GEM3
25	CAN1	51	SD1	77	GEM3

Quad SPI Flash Memory (MIO 0–12)

[Figure 2-1, callout 3]

The Micron dual MT25QU512ABB8ESF serial NOR flash Quad SPI flash memories can hold the boot image for the MPSoC system. To achieve higher performance, two Quad SPI flash memory devices are connected in parallel and provide an 8-bit data bus for boot and configuration. This interface is used to support QSPI32 boot mode as defined in the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2].

The dual Quad SPI flash memory located at U119/U120 provides 1 Gb of non-volatile storage that can be used for configuration and data storage.

- Part number: MT25QU512ABB8ESF-0SIT (Micron)
- Supply voltage: 1.8V
- Datapath width: 8 bits
- Data rate: various depending on single, dual, or quad mode

The connections between the SPI flash memory and the XCZU7EV MPSoC are listed in Table 3-6.

Table 3-6: **Quad SPI Flash Memory Component Connections to MPSoC U1**

XCZU7EV (U1) Pin	Net Name	Quad-SPI U119 (LWR), U120 (UPR)	
		Pin #	Pin Name
A25	MIO4_QSPI_LWR_DQ0	15	DQ0
C24	MIO1_QSPI_LWR_DQ1	8	DQ1
B24	MIO2_QSPI_LWR_DQ2	9	DQ2_WP_B
E25	MIO3_QSPI_LWR_DQ3	1	DQ3_RST_HOLD_B
A24	MIO0_QSPI_LWR_CLK	16	C
D25	MIO5_QSPI_LWR_CS_B	7	S_B
D26	MIO8_QSPI_UPR_DQ0	15	DQ0
C26	MIO9_QSPI_UPR_DQ1	8	DQ1
F26	MIO10_QSPI_UPR_DQ2	9	DQ2_WP_B
B26	MIO11_QSPI_UPR_DQ3	1	DQ3_RST_HOLD_B
C27	MIO12_QSPI_UPR_CLK	16	C
B25	MIO7_QSPI_UPR_CS_B	7	S_B

The configuration and Quad SPI flash memory section of the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] provides details on using the memory. For more Quad SPI details, see the Micron MT25QU512ABB8ESF-0SIT data sheet at the Micron website [Ref 15].

USB0 (MIO 52-63)

The USB interface on the PS-side serves multiple roles as a host or device controller. The USB 3.0 interface is supported by the MPSoC GTR interface while the USB 2.0 capabilities of the SMSC USB3320C controller are shared on a common USB 3.0 USB type A connector (J96).

USB 3.0 Transceiver and USB 2.0 ULPI PHY

[Figure 2-1, callout 5]

The ZCU106 board uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI transceiver at U116 to support a USB connection to the host computer (see Figure 3-3). A USB cable 3.0 A to A is supplied in the ZCU106 evaluation kit (host computer USB 3.0 A port to ZCU106 board connector J96). The USB3320 is a high-speed USB 2.0 PHY supporting the UTMI+ low pin interface (ULPI) interface standard. The ULPI standard defines the interface between the USB controller IP and the PHY device, which drives the physical USB bus. Use of the ULPI standard reduces the interface pin count between the USB controller IP and the PHY device.

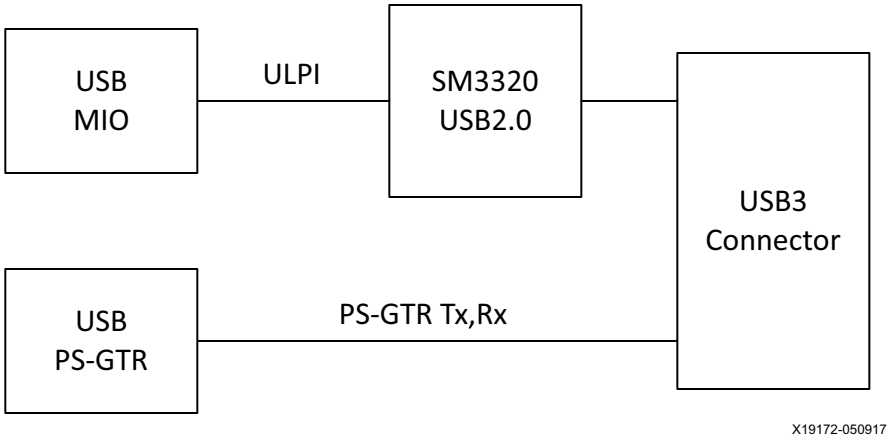


Figure 3-3: **USB Interface**

The USB3320 is clocked by a 24 MHz crystal. See the Standard Microsystems Corporation (SMSC) USB3320 data sheet for clocking mode details [Ref 16]. The interface to the USB3320 PHY is implemented through the IP in the XCZU7EV MPSoC PS.

Table 3-7 describes the jumper settings for the USB 2.0 circuit. Bold text identifies the default shunt positions for USB 2.0 high speed on-the-go (OTG) mode.

Table 3-7: **USB Jumper Settings**

Header	Function	Shunt Position	Notes
J110	CVBUS select	ON = Device mode (1 µF) **OFF = Host mode (120 µF) and source of bus power**	VBUS load capacitance
J96	USB 3.0 A	Position 1-2 = Shield floating (DNP C887 pads) **Position 2-3 = Shield connected to GND**	

The connections between the USB 2.0 PHY at U116 and the XCZU7EV MPSoC are listed in Table 3-8.

Table 3-8: **USB 2.0 ULPI Transceiver Connections to the XCZU7EV MPSoC**

XCZU7EV (U1) Pin	Net Name	USB3320 U116	
		Pin #	Pin Name
U117.4	ULPI0_RST_B(1)	27	RESET_B
H31	MIO58_USB_STP(2)	29	STP
G30	MIO53_USB_DIR	31	DIR
G29	MIO52_USB_CLK	1	CLKOUT
G33	MIO55_USB_NXT	2	NXT
G34	MIO56_USB_DATA0(2)	3	DATA0
H29	MIO57_USB_DATA1(2)	4	DATA1
G31	MIO54_USB_DATA2(2)	5	DATA2
H32	MIO59_USB_DATA3(2)	6	DATA3
H33	MIO60_USB_DATA4(2)	7	DATA4
H34	MIO61_USB_DATA5(2)	9	DATA5
J29	MIO62_USB_DATA6(2)	10	DATA6
J30	MIO63_USB_DATA7(2)	13	DATA7

Notes:

1. PS_POR_B (U1.M24) or PS_MODE1 (DIP SW6.2) or PB SW2 drive U116 RST_B via OR gate U117.
2. These nets are 30Ω series resistor coupled.

Note: The shield for the USB 3.0 A connector (J96) can be tied to GND by a jumper on header J112 pins 2-3 (default). The USB shield can optionally be connected through a capacitor to GND by installing a capacitor (body size 0402) at location C887 and jumping pins 1-2 on header J112.

The USB3320 ULPI U116 transceiver circuit (see Figure 3-4) has a Micrel MIC2544 high-side programmable current limit switch (U121). This switch has an open-drain output fault flag on pin 2, which turns on LED DS51 if over current or thermal shutdown conditions are detected. DS51 is located in the U116 circuit area near pushbutton SW2 (Figure 2-1, callout 5).

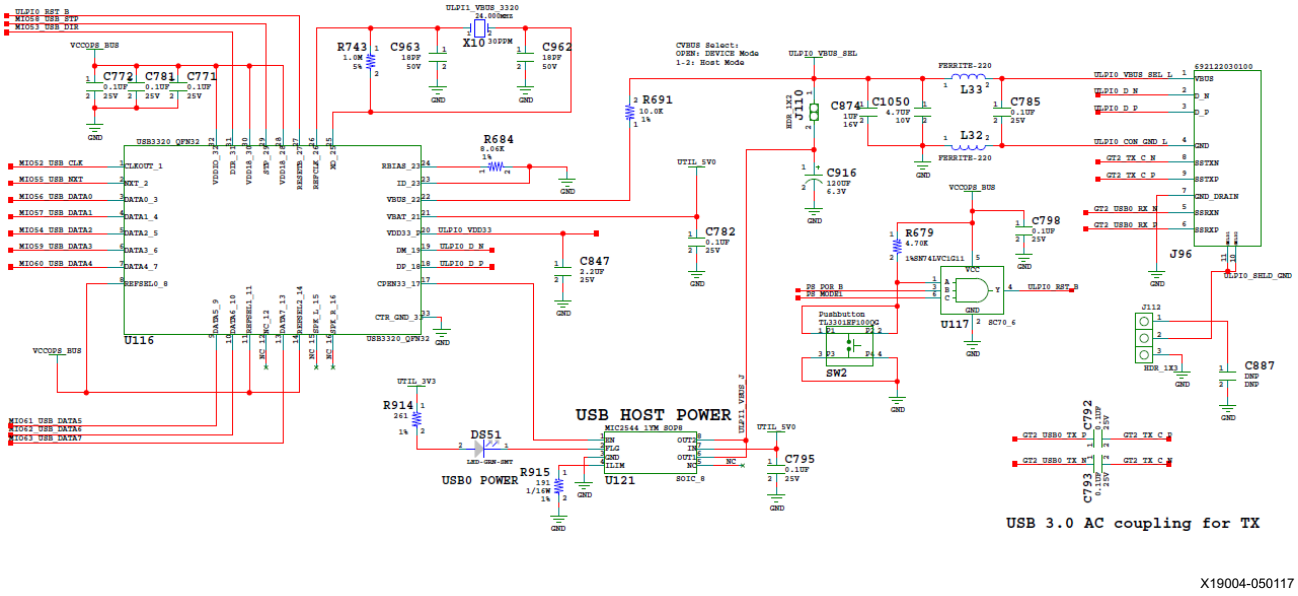


Figure 3-4: **ULPI U116 Transceiver Circuit**

SD1 (MIO 39-51)

A PS-side interface to an SD card connector is provided for booting and file system storage. This interface is used for the SD boot mode and supports SD3.0 access post boot.

SD Card Interface

[Figure 2-1, callout 6]

The ZCU106 board includes a secure digital input/output (SDIO) interface to provide access to general purpose non-volatile SDIO memory cards and peripherals. See the SanDisk Corporation [Ref 17] or SD Association [Ref 18] websites for more information on the SD I/O card specification. The ZCU106 SD card interface supports the SD1_LS configuration boot mode documented in the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2].

The SDIO signals are connected to XCZU7EV MPSoC PS bank 501, which has its V_{CCMIO} set to 1.8V. Each of the six MIO[46-51]_SDIO_* nets has a series 30Ω resistor at the source. An NXP IP4856CX25 SD 3.0-compliant voltage level-translator U133 is present between the XCZU7EV MPSoC and the SD card connector (J100). The NXP IP4856CX25 U133 device provides SD3.0 capability with SDR104 performance.

Figure 3-5 shows the connections of the SD card interface on the ZCU106 board.

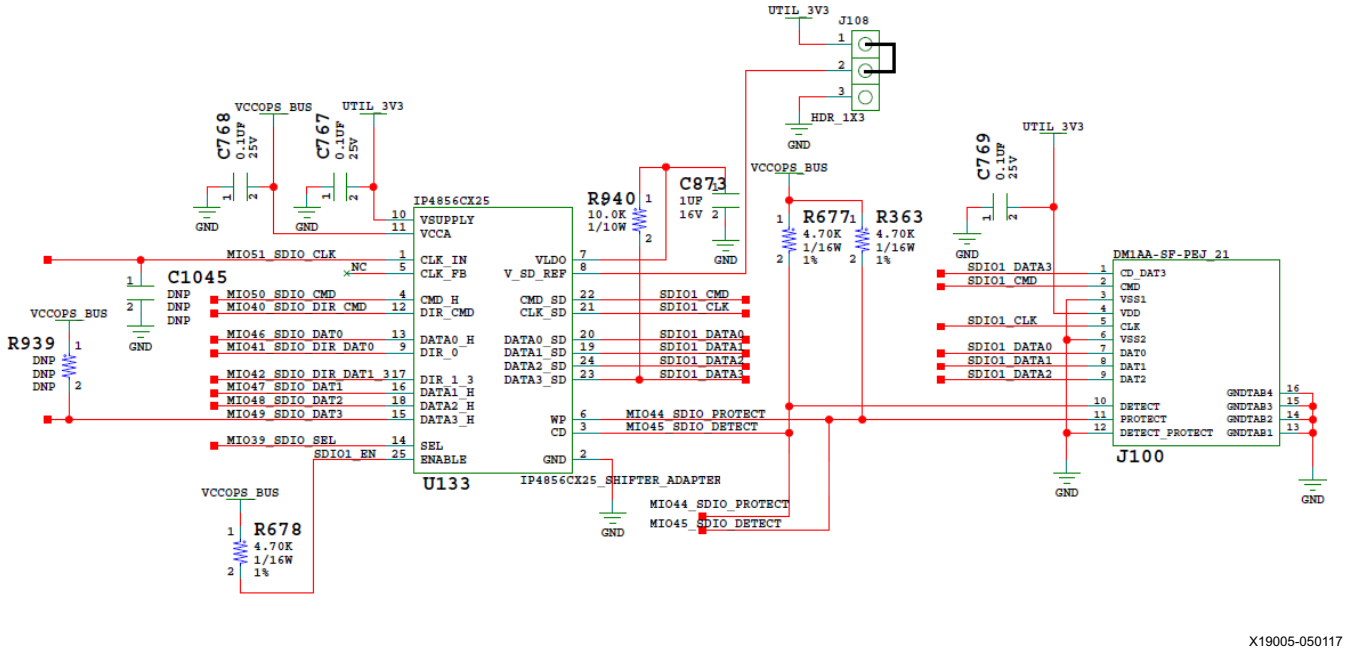


Figure 3-5: **SD Card Interface**

The NXP SD3.0 level shifter is mounted on an Aries adapter board that has the pin mapping listed in Table 3-9.

Table 3-9: **U133 IP4856CX25 Adapter Pin-Out**

Aries Adapter Pin Number	IP4856CX25 U133 Pin Number	IP4856CX25 U133 Pin Name
1	C1	CLK_IN
2	C3	GND
3	D3	CD
4	D2	CMD_H
5	E2	CLK_FB
6	E4	WP
7	B4	VLDO
8	C4	V_{SD_REF}
9	A3	DIR_0
10	A4	V_{SUPPLY}
11	B3	V_{CCA}
12	A2	DIR_CMD
13	D1	DATA0_H
14	B2	SEL

Table 3-9: **U133 IP4856CX25 Adapter Pin-Out *(Cont'd)***

Aries Adapter Pin Number	IP4856CX25 U133 Pin Number	IP4856CX25 U133 Pin Name
15	B1	DATA3_H
16	E1	DATA1_H
17	E3	DIR_1_3
18	A1	DATA2_H
19	E5	DATA1_SD
20	D5	DATA0_SD
21	C5	CLK_SD
22	D4	CMD_SD
23	B5	DATA3_SD
24	A5	DATA2_SD
25	C2	ENABLE

Table 3-10 lists the SD card interface connections to the XCZU7EV MPSoC.

Table 3-10: **SD Interface Connections to the XCZU7EV MPSoC**

XCZU7EV (U1) Pin	Net Name	U133 IP4856CX25 Adapter	
		Pin #	Pin Name
D30	MIO39_SDIO_SEL	14	SEL
D31	MIO40_SDIO_DIR_CMD	12	DIR_CMD
D32	MIO41_SDIO_DIR_DAT0	9	DIR_0
D34	MIO42_SDIO_DIR_DAT1_3	17	DIR_1_3
E34	MIO46_SDIO_DAT0	13	DATA0_H
F30	MIO47_SDIO_DAT1	16	DATA1_H
F31	MIO48_SDIO_DAT2	18	DATA2_H
F32	MIO49_SDIO_DAT3	15	DATA3_H
F33	MIO50_SDIO_CMD	4	CMD_H
F34	MIO51_SDIO_CLK	1	CLK_IN
E32	MIO44_SDIO_PROTECT	6	WP
E33	MIO45_SDIO_DETECT	3	CD

Programmable Logic JTAG Programming Options

[Figure 2-1, callouts 7 and 39]

ZCU106 JTAG chain:

- J2 USB micro AB connector connected to U152 FTDI USB JTAG bridge
- J8 2x7 2 mm shrouded, keyed JTAG pod flat cable connector
- J6 2x10 ARM JTAG male pin header

The ZCU106 board JTAG chain is shown in Figure 3-6.

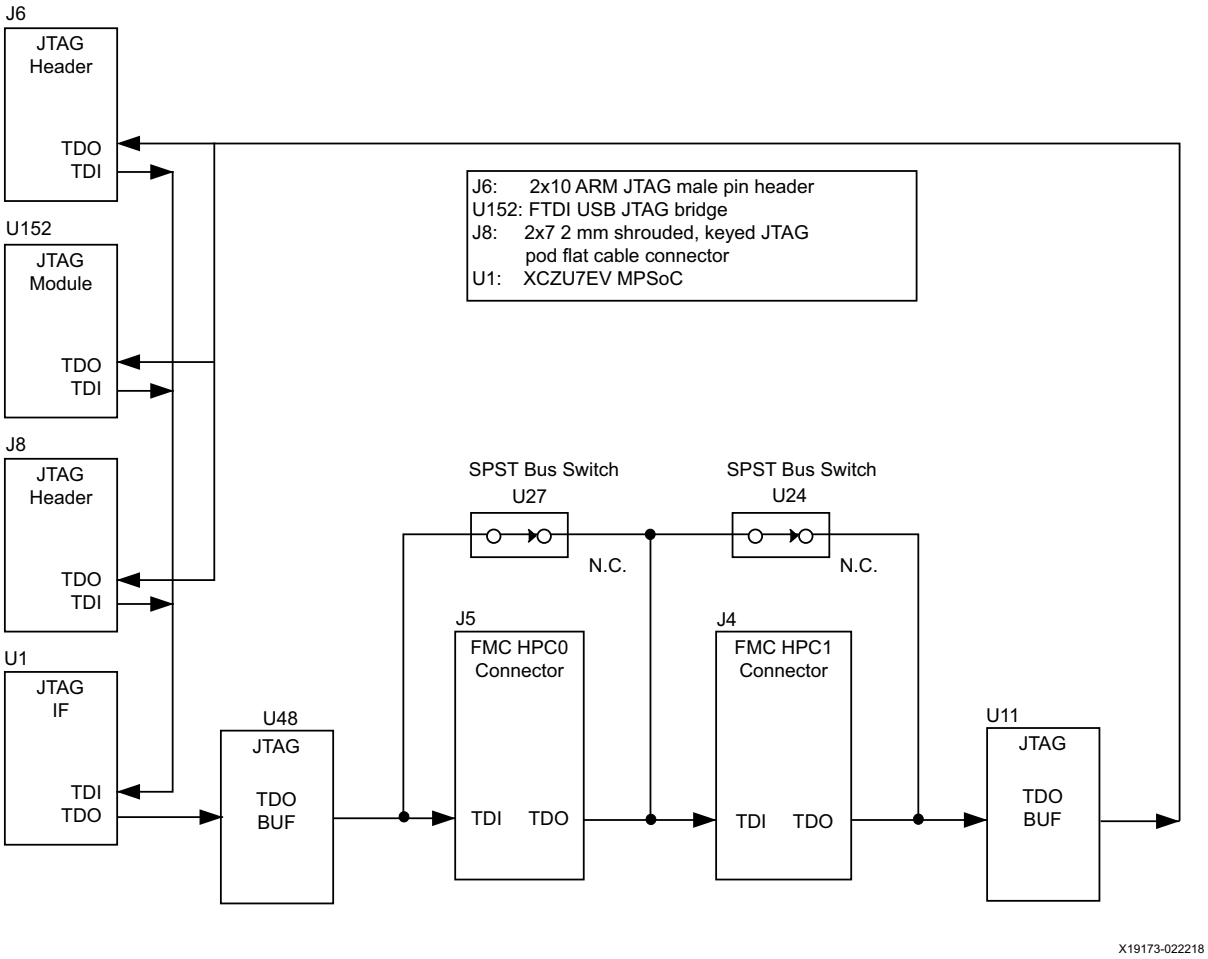


Figure 3-6: **JTAG Chain Block Diagram**

For more details on the FTDI FT232HL USB UART, see [Ref 26].

FMC Connector JTAG Bypass

When an FPGA mezzanine card (FMC) is attached to J5 or J4, it is automatically added to the JTAG chain through electronically controlled single-pole single-throw (SPST) switches U27 and U24. The SPST switches are normally closed and transition to an open state when an FMC is attached. Switch U27 adds an attached FMC to the JTAG chain as determined by the FMC_HPC0_PRSNT_M2C_B signal. Switch U24 adds an attached FMC to the JTAG chain as determined by the FMC_HPC1_PRSNT_M2C_B signal. The attached FMC card must implement a TDI-to-TDO connection using a device or bypass jumper to ensure that the JTAG chain connects to the U1 XCZU7EV MPSoC.

EMIO ARM Trace Port

[Figure 2-1, callout 34]

The ZCU106 evaluation board provides a trace/debug 38-pin Mictor connector, P6. Figure 3-7 shows connector P6 with its MPSoC bank 87/88 connections.

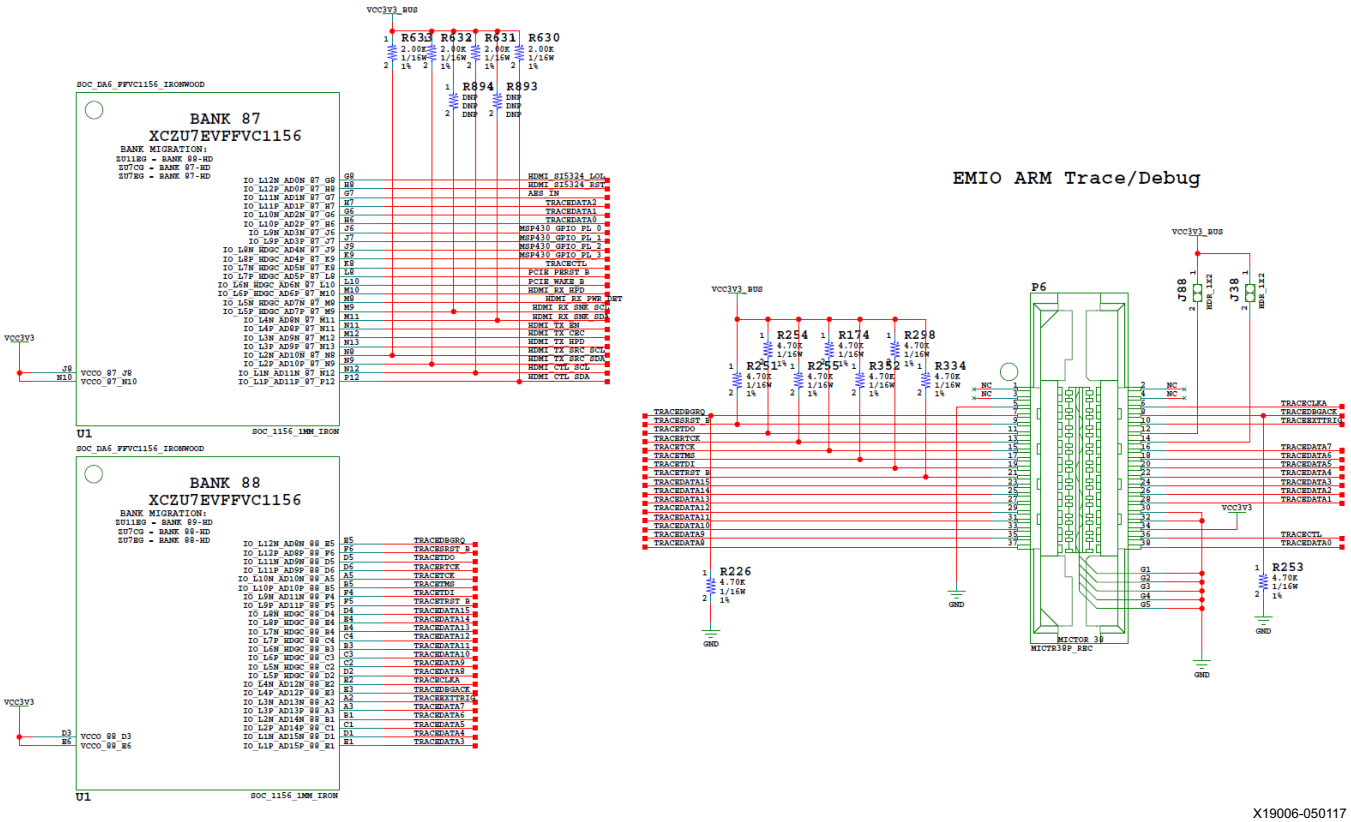


Figure 3-7: **EMIO ARM Trace Port Interface**

The P6 connector to MPSoC connections are listed in Table 3-11.

Table 3-11: **Trace/Debug Conn. P6 Connections to the XCZU7EV MPSoC**

XCZU7EV (U1) Pin	Net Name	I/O Standard	Trace/Debug P6 Pin
H6	TRACEDATA0	LVCMOS33	38
G6	TRACEDATA1	LVCMOS33	28
H7	TRACEDATA2	LVCMOS33	26
E1	TRACEDATA3	LVCMOS33	24
D1	TRACEDATA4	LVCMOS33	22
C1	TRACEDATA5	LVCMOS33	20
B1	TRACEDATA6	LVCMOS33	18
A3	TRACEDATA7	LVCMOS33	16
D2	TRACEDATA8	LVCMOS33	37
C2	TRACEDATA9	LVCMOS33	35
C3	TRACEDATA1	LVCMOS33	33
B3	TRACEDATA11	LVCMOS33	31
C4	TRACEDATA12	LVCMOS33	29
B4	TRACEDATA13	LVCMOS33	27
E4	TRACEDATA14	LVCMOS33	25
D4	TRACEDATA15	LVCMOS33	23
E2	TRACECLKA	LVCMOS33	6
D6	TRACERTCK	LVCMOS33	13
E5	TRACEDBGRQ	LVCMOS33	7
E3	TRACEDBGACK	LVCMOS33	8
K8	TRACECTL	LVCMOS33	36
A2	TRACEEXTTRIG	LVCMOS33	10
A5	TRACETCK	LVCMOS33	15
F4	TRACETDI	LVCMOS33	19
D5	TRACETDO	LVCMOS33	11
B5	TRACETMS	LVCMOS33	17
F5	TRACETRST_B	LVCMOS33	21
F6	TRACESRST_B	LVCMOS33	9

For more information about managing the Zynq MPSoC extended MIO (EMIO) trace port connections, see the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2].

Clock Generation

The ZCU106 board provides fixed and variable clock sources for the XCZU7EV MPSoC. Table 3-12 lists the source devices for each clock.

Table 3-12: **Clock Sources**

Clock (Net) Name	Frequency	Clock Source
Fixed Frequency Clocks		
PS_REF_CLK	33.33 MHz	U69 SI5341B clock generator
CLK_74_25	74.25 MHz	
CLK_125	125 MHz	
GTR_REF_CLK_SATA	125 MHz	
GTR_REF_CLK_USB3	26 MHz	
GTR_REF_CLK_DP	27 MHz	
Programmable Frequency Clocks		
USER_SI570	300 MHz (default)	U42 SI570 I2C PROG. OSC.
USER_MGT_SI570	156.25 MHz (default)	U56 SI570 I2C PROG. OSC.
USER_MGT_SMA	User-Provided source	J79 (P)/J80 (N) SMA CONN.
HDMI_SI5324_OUT	Variable	U108 SI5319C clock recovery
SFP_SI5328_OUT	Variable	U20 SI5328B clock recovery

Table 3-13 lists the source devices for each clock.

Table 3-13: **Clock Connections, Source to XCZU7EV MPSoC**

Clock Source Ref. Des. and Pin	Net Name	I/O Standard	XCZU7EV (U1) Pin
U69.59	PS_REF_CLK	(1)	R24
U69.45	CLK_125_P	LVDS_25	H9
U69.44	CLK_125_N	LVDS_25	G9
U69.51	CLK_74_25_P	LVDS_25	D15
U69.50	CLK_74_25_N	LVDS_25	D14
U69.35	GTR_REF_CLK_SATA_P	(2)	P27
U69.34	GTR_REF_CLK_SATA_N	(2)	P28
U69.31	GTR_REF_CLK_USB3_P	(2)	M27
U69.30	GTR_REF_CLK_USB3_N	(2)	M28
U69.24	GTR_REF_CLK_DP_P	(2)	M31
U69.23	GTR_REF_CLK_DP_N	(2)	M32
U42.4	USER_SI570_P	DIFF_SSTL12	AH12
U42.5	USER_SI570_N	DIFF_SSTL12	AJ12

Table 3-13: **Clock Connections, Source to XCZU7EV MPSoC *(Cont'd)***

Clock Source Ref. Des. and Pin	Net Name	I/O Standard	XCZU7EV (U1) Pin
U56.4	USER_MGT_SI570_P	(2)	(1-to-2 CLOCK BUFFER) U51.6
U56.5	USER_MGT_SI570_N	(2)	(1-to-2 CLOCK BUFFER) U51.7
U51.11	USER_MGT_SI570_CLOCK1_P	(2)	U10
U51.12	USER_MGT_SI570_CLOCK1_N	(2)	U9
U51.13	USER_MGT_SI570_CLOCK2_P	(2)	R10
U51.14	USER_MGT_SI570_CLOCK2_N	(2)	R9
J79.1	USER_SMA_MGT_CLOCK_P	(2)	AA10
J80.1	USER_SMA_MGT_CLOCK_N	(2)	AA9
U108.28	HDMI_SI5324_OUT_P	(2)	AD8
U108.29	HDMI_SI5324_OUT_N	(2)	AD7
U20.28	SFP_SI5328_OUT_P	(2)	W10
U20.29	SFP_SI5328_OUT_N	(2)	W9

Notes:

1. U1 XCU7EV Bank 503 supports LVCMOS level inputs.
2. U1 MGT (I/O standards do not apply).

SI5341B 10 Independent Output Any-Frequency Clock Generator

[Figure 2-1, callout 8]

- Clock generator: Silicon Labs SI5341B-B05071-GM
- Jitter: <100 fs RMS typical
- Differential and single-ended outputs

The SI5341B (U69) is a one-time programmable clock source. For more details, see the SI5341B data sheet [Ref 19]. The clock circuit is shown in Figure 3-8.

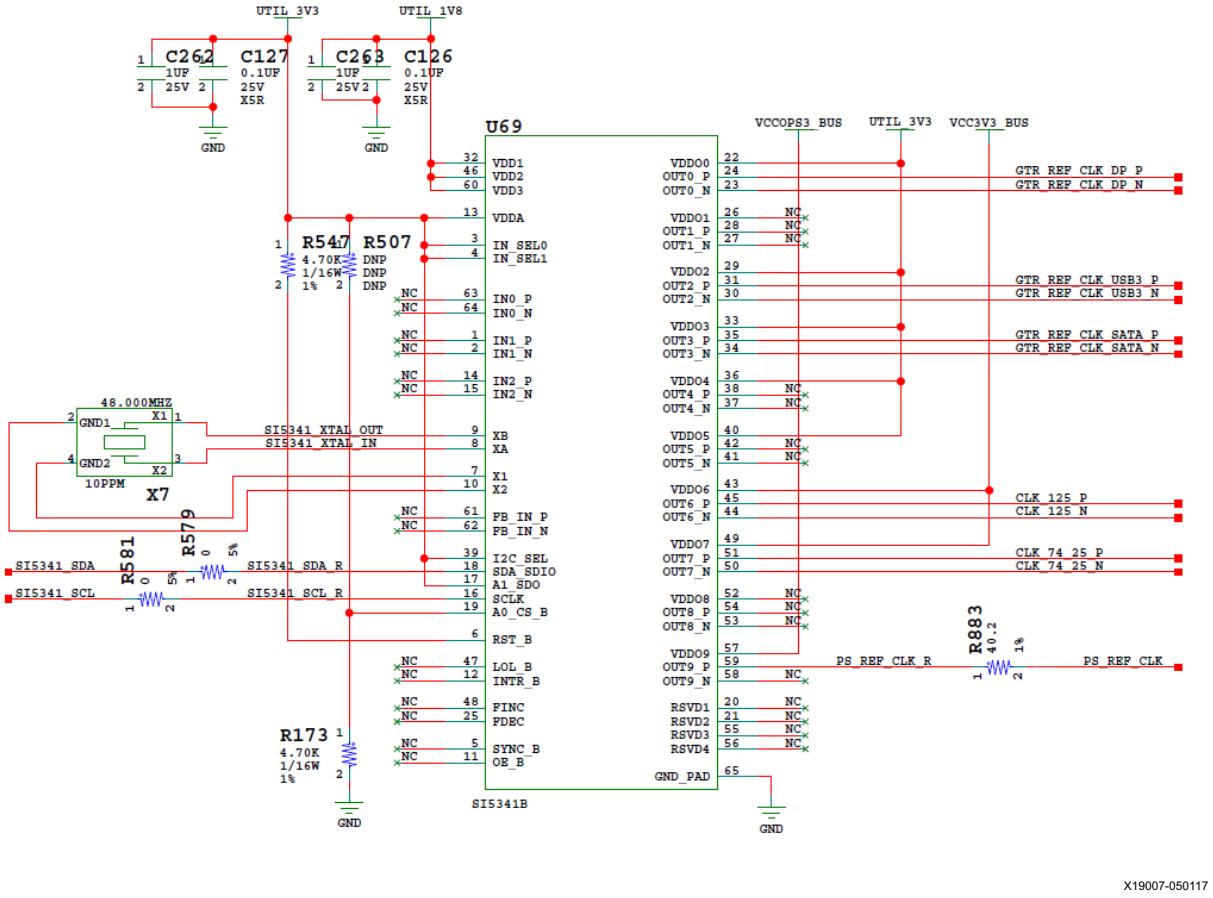


Figure 3-8: **SI5341B Clock Generator**

Programmable User Clock

[Figure 2-1, callout 9]

The ZCU106 board has an I2C programmable SI570 low-jitter 3.3V LVDS differential oscillator (U42) connected to the GC inputs of PL bank 66. This USER_SI570_P and USER_SI570_N clock signals are connected to XCZU7EV MPSoC U1 pins AH12 and AJ12, respectively. On power up, the user clock defaults to an output frequency of 300.000 MHz. User applications can change the output frequency within the range of 10 MHz to 810 MHz through an I2C interface. Power cycling the ZCU106 board reverts this user clock to the default frequency of 300.000 MHz.

This oscillator can be reprogrammed from MSP430 system controller U41 (see TI MSP430 System Controller, page 116 for more information).

- Programmable oscillator: Silicon Labs Si570BAB001614DG (10 MHz-810 MHz, 300 MHz default)
- LVDS differential output
- Total stability: 61.5 ppm

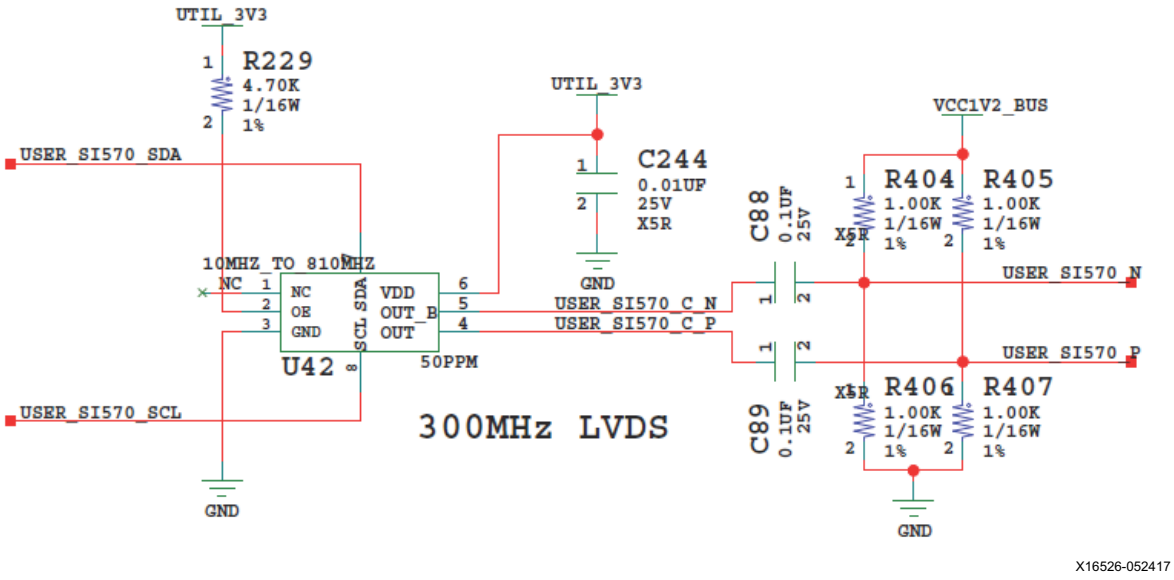


Figure 3-9: **Programmable User Clock**

Programmable User MGT Clock

[Figure 2-1, callout 10]

The ZCU106 board has a programmable low-jitter 3.3V LVDS SI570 differential oscillator (U56) connected to a 1-to-2 SI53340 clock driver (U51). On power up, the user clock defaults to an output frequency of 156.250 MHz. User applications can change the output frequency within the range of 10 MHz to 810 MHz through an I2C interface. Power cycling the ZCU106 board reverts this user clock to the default frequency of 156.250 MHz.

This oscillator can be reprogrammed from MSP430 system controller U41 (see TI MSP430 System Controller, page 116 for more information).

- Programmable oscillator: Silicon Labs Si570BAB000544DG (10 MHz-810 MHz, 156.250 MHz default)
- LVDS differential output
- Total stability: 61.5 ppm

The user clock MGT circuit is shown in Figure 3-10. The Silicon Labs Si570 and Si53340 data sheets are available on the Silicon Labs website [Ref 19].

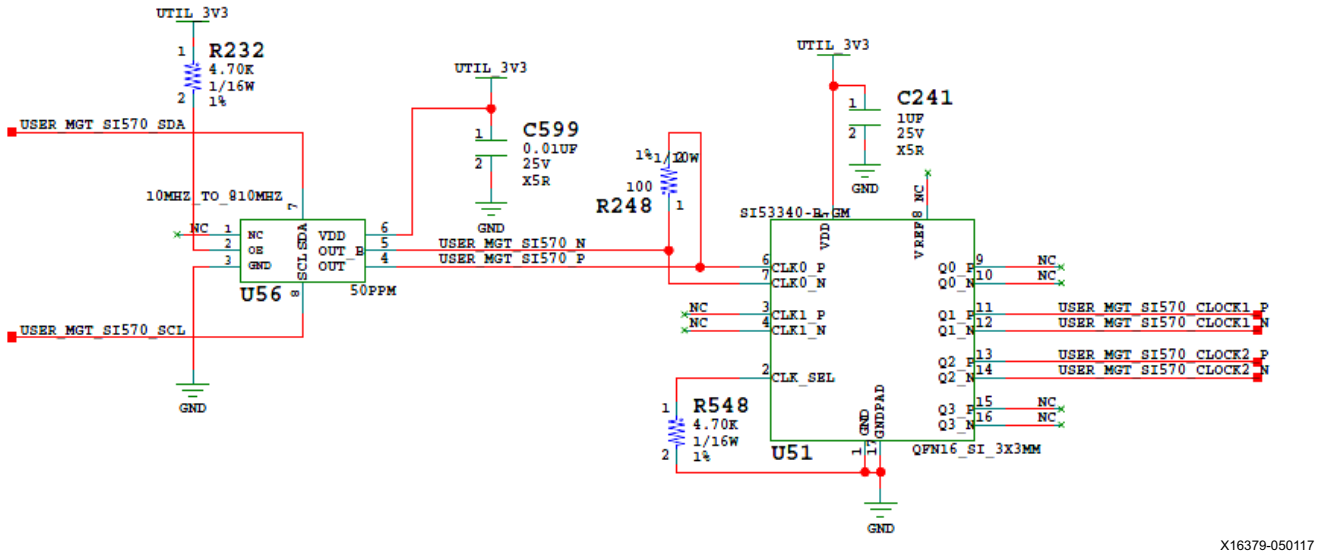


Figure 3-10: **Programmable User MGT Clock**

User SMA MGT Clock

[Figure 2-1, callout 48]

The ZCU106 board provides a pair of SMAs for differential AC coupled user MGT clock input into FPGA U1 MGTH bank 224. This differential signal pair is series-capacitor coupled. The P-side SMA J79 signal USER_SMA_MGT_CLOCK_P is connected to U1 MGTREFCLK1P pin AA10. The N-side SMA J80 signal USER_SMA_MGT_CLOCK_N connected to U1 MGTREFCLK1N pin AA9. The user SMA MGT clock circuit is shown in Figure 3-11.

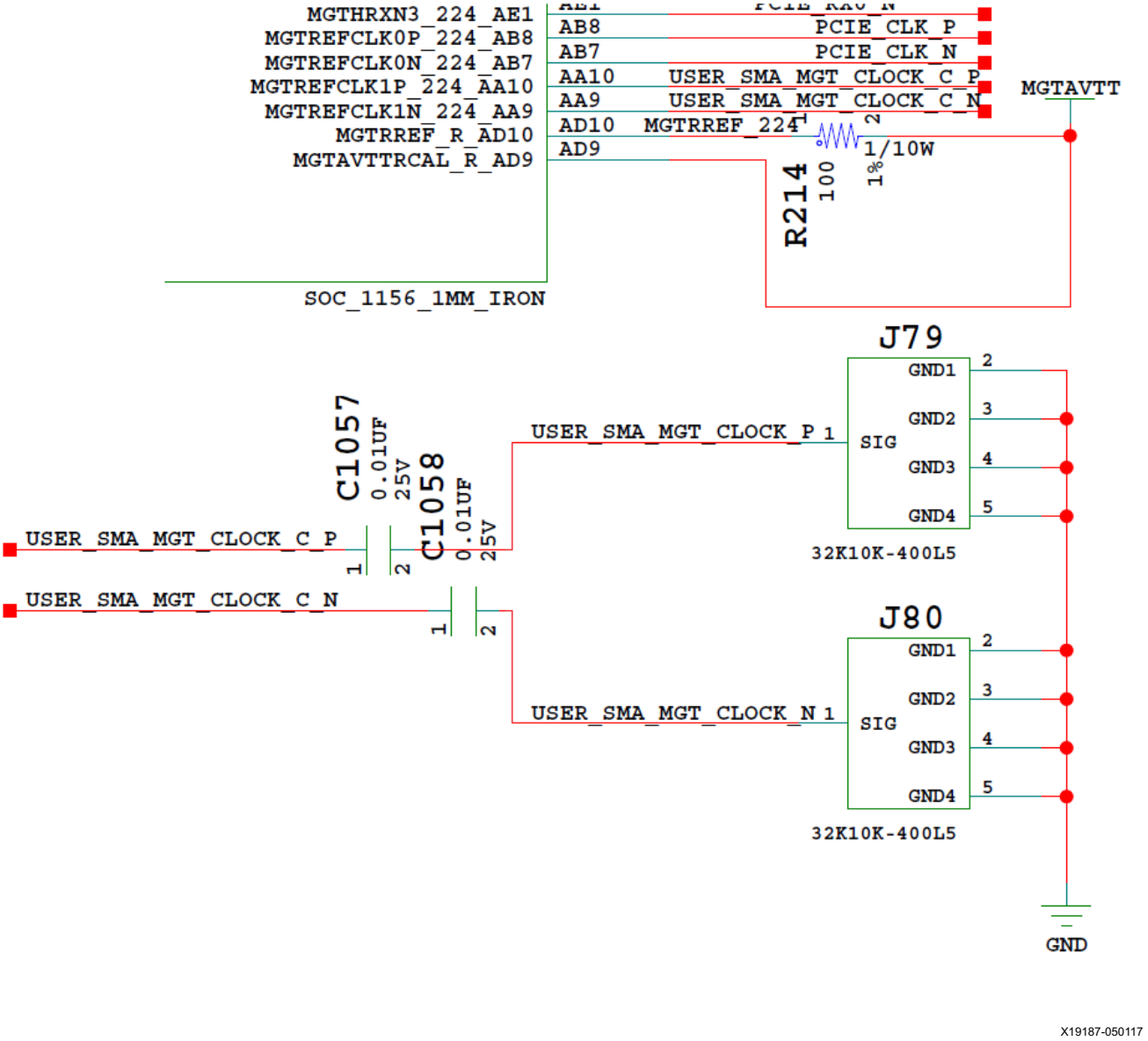


Figure 3-11: **User SMA MGT Clock**

GEM3 Ethernet (MIO 64-77)

[Figure 2-1, callout 12]

The PS-side Gigabit Ethernet MAC (GEM) implements a 10/100/1000 Mb/s Ethernet interface (see Figure 3-12), which connects to a TI DP83867IRPAP Ethernet RGMII PHY before being routed to an RJ45 Ethernet connector. The RGMII Ethernet PHY is boot strapped to PHY address `5'b01100` (`0x0C`) and Auto Negotiation is set to Enable. Communication with the device is covered in the DP83867 RGMII PHY data sheet [Ref 20].

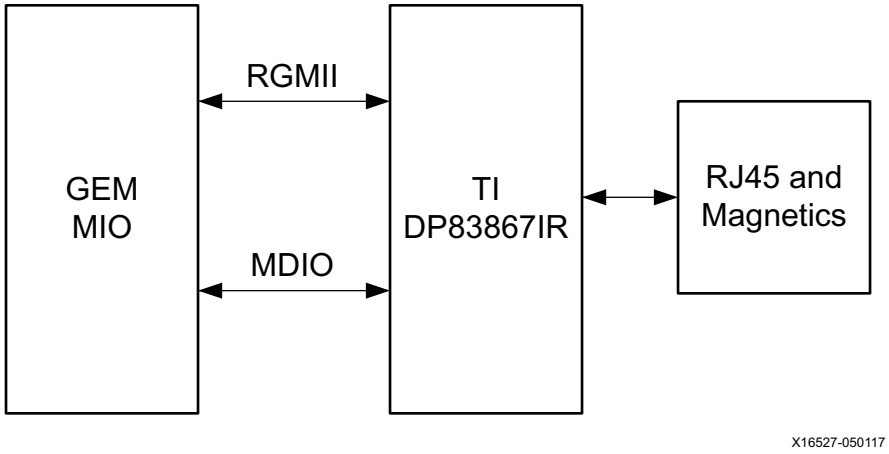


Figure 3-12: **Ethernet Block Diagram**

10/100/1000 MHz Tri-Speed Ethernet PHY

[Figure 2-1, callout 12]

The ZCU106 board uses the TIDP83867IRPAP Ethernet RGMII PHY [Ref 20] (U98) for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1000 Mb/s. The board supports RGMII mode only. The PHY connection to a user-provided Ethernet cable is through a Wurth 7499111221A RJ-45 connector (P12) with built-in magnetics.

The Ethernet connections from XCZU7EV MPSoC U1 to the DP83867IRPAP PHY device at U98 are listed in Table 3-14.

Table 3-14: **DP83867 PHY Connections to XCZU7EV MPSoC**

XCZU7EV (U1) Pin	Net Name	DP83867 PHY U98	
		Pin #	Pin Name
J31	MIO64_ENET_TX_CLK	40	GTX_CLK
J32	MIO65_ENET_TX_D0	38	TX_DO
J34	MIO66_ENET_TX_D1	37	TX_D1
K28	MIO67_ENET_TX_D2	36	TX_D2

Table 3-14: **DP83867 PHY Connections to XCZU7EV MPSoC *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	DP83867 PHY U98	
		Pin #	Pin Name
K29	MIO68_ENET_TX_D3	35	TX_D3
K30	MIO69_ENET_TX_CTRL	52	TX_EN_TX_CTRL
K31	MIO70_ENET_RX_CLK	43	RX_CLK
K32	MIO71_ENET_RX_D0	44	RX_DO
K33	MIO72_ENET_RX_D1	45	RX_D1
K34	MIO73_ENET_RX_D2	46	RX_D2
L29	MIO74_ENET_RX_D3	47	RX_D3
L30	MIO75_ENET_RX_CTRL	53	RX_DV_RX_CTRL
L33	MIO76_ENET_MDC	20	MDC
L34	MIO77_ENET_MDIO	21	MDIO

Ethernet PHY Reset

The DP83867IRPAP PHY U98 reset circuit is shown in Figure 3-13. The DP83867IRPAP can be reset by the SW9 pushbutton (U59.6), the MAX16025 U22 MPSoC PS-side POR reset device (U59.1), or the I2C0 connected U97 TCA6416A I/O expander port P06 pin 10 (U59.3).

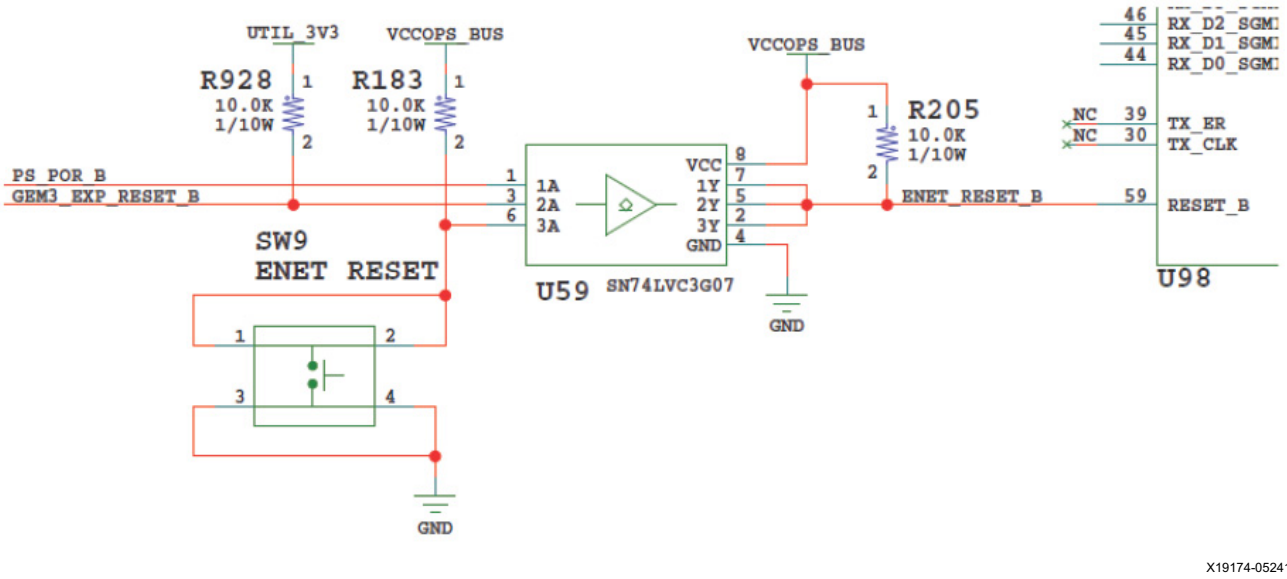


Figure 3-13: **Ethernet PHY Reset Circuit**

Ethernet PHY LED Interface

[Figure 2-1, callout 12]

The DP83867IRPAP PHY U98 LED interface (LED_0, LED_2) uses the two LEDs embedded in the P12 RJ45 connector bezel. LED_1 is LED DS27, which is located on the top of the board just above the P12 Ethernet RJ45 connector (item 12 in Table 2-1).The LED functional description is listed in Table 3-15.

Table 3-15: **Ethernet PHY LED Functional Description**

Pin		Type	Description
Name	Number		
LED_2	61	S, I/O, PD	By default, this pin indicates receive or transmit activity. Additional functionality is configurable using LEDCR1[11:8] register bits. ***Note:*** This pin is a strap configuration pin for RGZ devices only.
LED_1	62	S, I/O, PD	By default, this pin indicates that 100BASE-T link is established. Additional functionality is configurable using LEDCR1[7:4] register bits.
LED_0	63	S, I/O, PD	By default, this pin indicates that link is established. Additional functionality is configurable using LEDCR1[3:0] register bits.

The LED functions can be re-purposed with a LEDCR1 register write available via the PHY's management data interface, MDIO/MDC. LED_2 is assigned to the activity indicator (ACT) and LED_0 indicates link established. For more Ethernet PHY details, see the TI DS83867 data sheet [Ref 20].

CP2108 USB UART Interface

[Figure 2-1, callout 13]

The CP2108 quad USB-UART on the ZCU106 board provides four level-shifted UART connections through single micro-B USB connector J83. Channel 0 and 1 are PS-side MIO connections described in the UART0 (MIO 18-19) section. Channel 2 is a PL-side connection and Channel 3 is connected to MSP430 system controller U41. The USB UART interface circuit is shown in Figure 3-14. The Silicon Labs CP2108 data sheet is available on the Silicon Labs website [Ref 19].

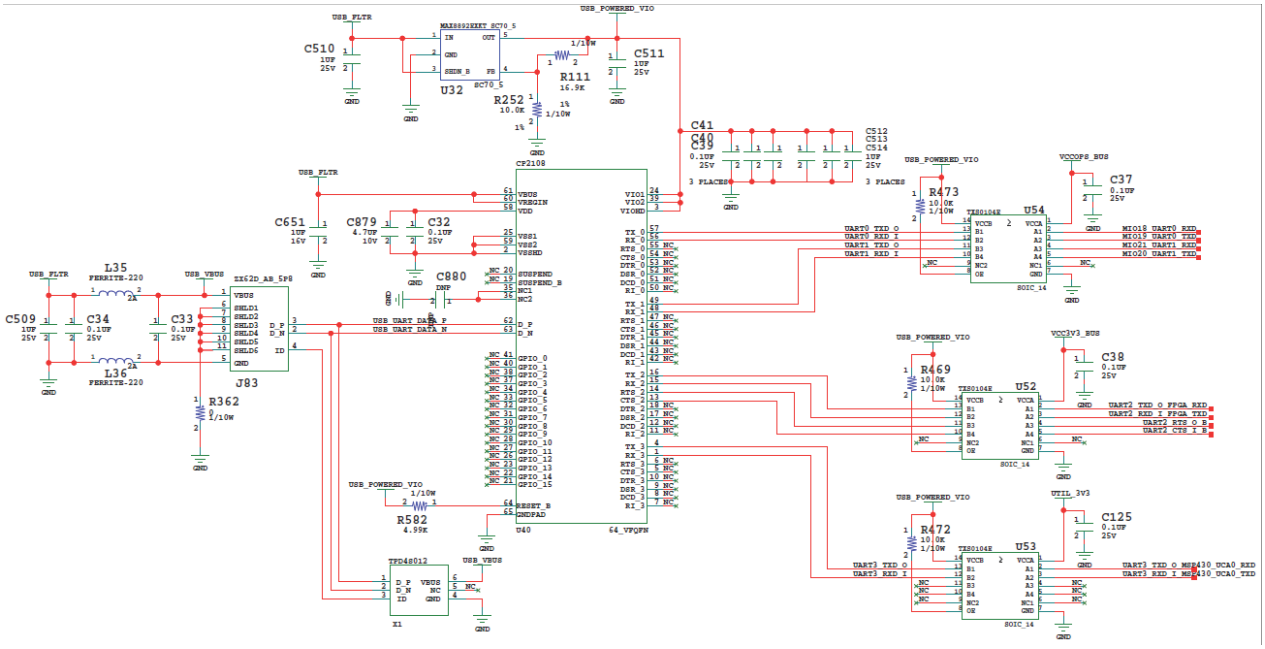


Figure 3-14: **USB UART Interface**

CP2108 Channel 2 PL-Side UART Interface

The CP2108 channel 2 bank 64 PL-side UART interface circuit is shown in Figure 3-15. The connections from XCZU7EV MPSoC U1 to CP2108 U40 via TSX0104E level shifter U52 are listed in Table 3-16.

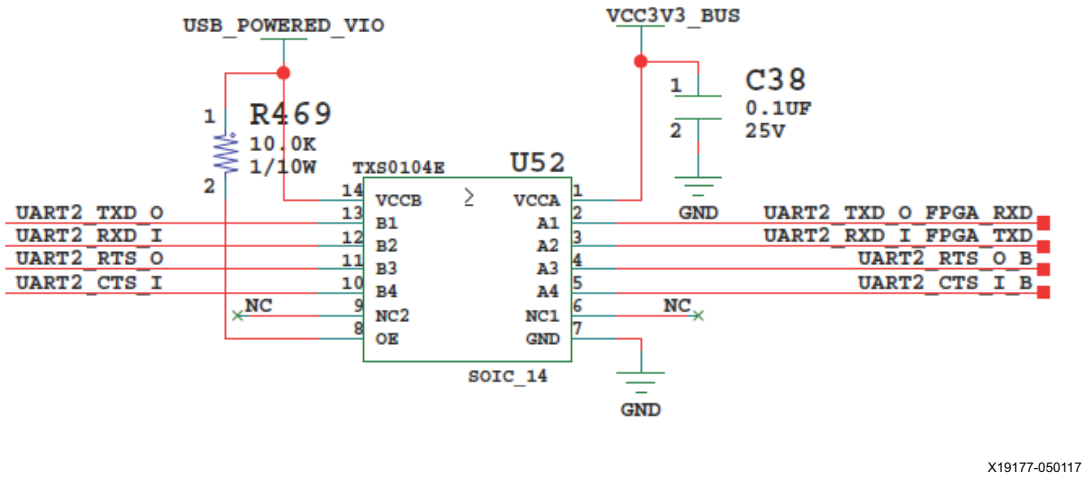


Figure 3-15: **PL-Side USB UART Interface**

Table 3-16: **XCZU7EV U1 to CP2108 U40 Connections via L/S U52**

XCZU7EV (U1) Pin	Net Name	CP2108 U40	
		Pin Name	Pin #
AH17	UART2_TXD_O_FPGA_RXD	TX_2	16
AL17	UART2_RXD_I_FPGA_TXD	RX_2	15
AM15	UART2_RTS_O_B	RTS_2	14
AP17	UART2_RTS_I_B	CTS_2	13

CP2108 Channel 3 MSP430 UART Interface

The CP2108 channel 3 MSP430 UART interface circuit is shown in Figure 3-16. The connections from MSP430 U41 to CP2108 U40 via TSX0104E level shifter U53 are listed in Table 3-17.

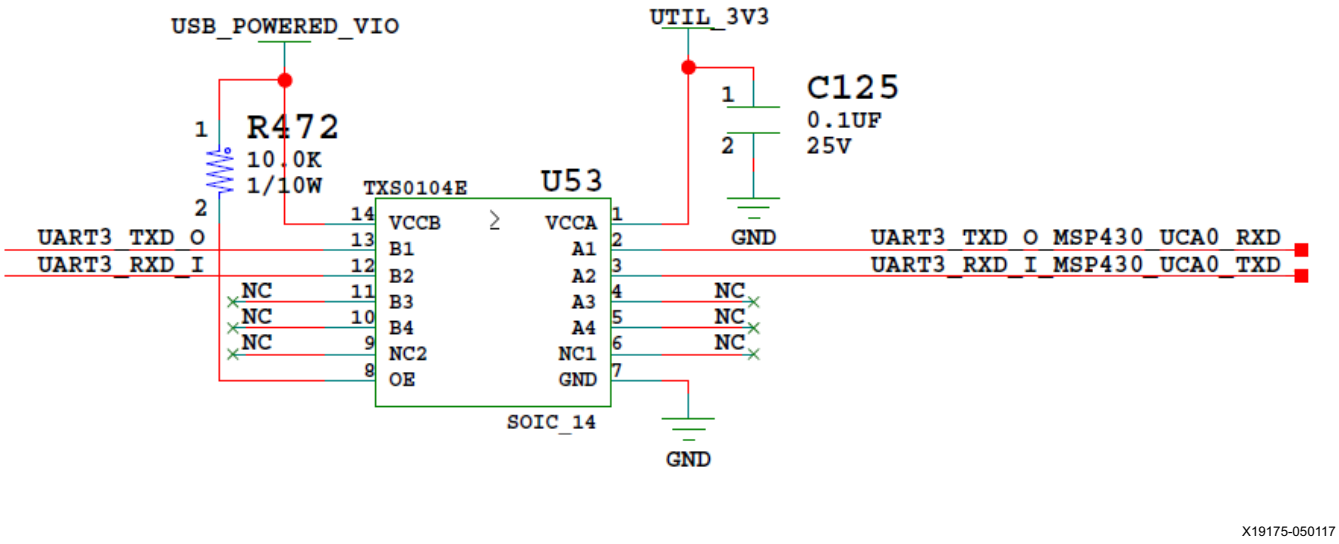


Figure 3-16: **MSP430 USB UART Interface**

Table 3-17: **MSP430 U41 to CP2108 U40 Connections via L/S U53**

MSP430 U41		Net Name	CP2108 U40	
Pin Name	Pin #		Pin Name	Pin #
P3_3	26	UART3_TXD_O_MSP430_UCA0_RXD	TX_3	4
P3_3	25	UART3_RXD_I_MSP430_UCA0_TXD	RX_3	1

GPIO (MIO 13, 38)

These two GPIO bits are connected to the U41 MSP430 system controller for general purpose signaling or communications between the Zynq UltraScale+ MPSoC device and the MSP430 system controller. These signals are level-shifted by TSX0108E U141. The connections between the U41 system controller and the XCZU7EV MPSoC are listed in Table 3-18.

Table 3-18: **System Controller U41 GPIO Connections to XCZU7EV U1**

XCZU7EV (U1) Pin	Net Name	MSP430 U41	
		Pin Name	Pin #
AH17	MIO13_PS_GPIO2	20	P1_7
AL17	MIO38_PS_GPIO1	19	P1_6

I2C0 (MIO 14-15)

I2C0 connects to MPSoC U1 PS bank 500 and PL bank 65, and to system controller U41, as shown in Figure 3-18. I2C0 connects to two GPIO 16-bit port expanders (TCA6416A U61 and U97) and an I2C multiplexer (PCA9544A U60) for controlling resets and power system enable pins, and accepting various alarm inputs without requiring the PL-side to be configured. TCA6416A U97 is pin-strapped to respond to I2C address `0x20`, and U61 to `0x21`. The PCA9544A U60 multiplexer is set to `0x75`.

The I2C0 bus also provides access to the PMBus power controllers and PS-side and PL-side INA226 power monitors via the U60 PCA9544A multiplexer. All PMBus controlled Maxim regulators are tied to the MAXIM_PMBUS, while the INA226 power monitors are separated on to PS_PMBUS and PL_PMBUS. Figure 3-17 shows the I2C0 bus topology. Table 3-19 lists the I2C0 port expander TCA6416A U61 connections and Table 3-20 lists the TCA6416A U97 connections. The devices on each bus of the I2C0 multiplexer U60 are identified in Table 3-21 and the multiplexer bus connections are listed in Table 3-22.

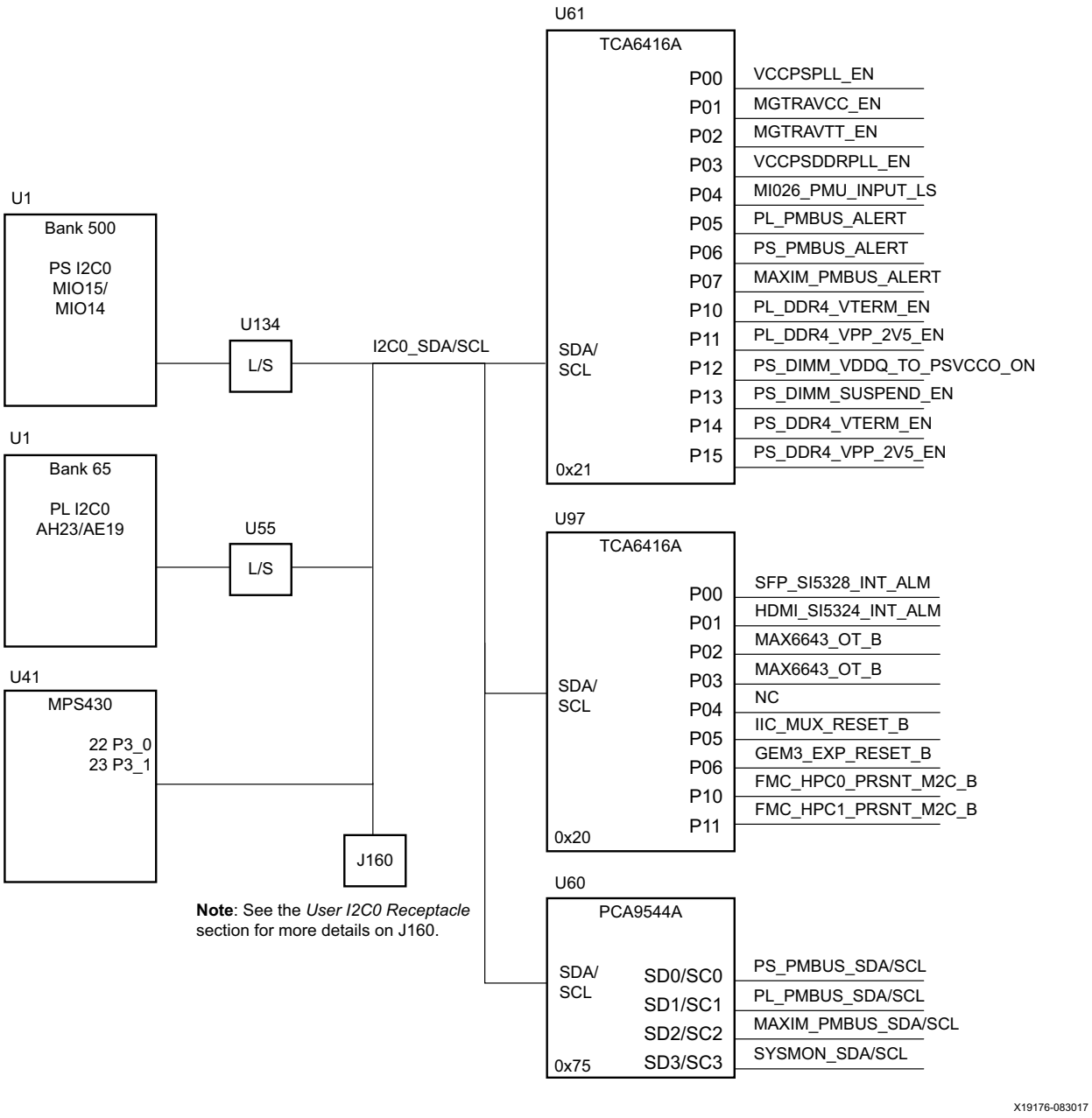


Figure 3-17: **I2C0 Bus Topology**

Table 3-19: **I2C0 Port Expander TCA6416A U61 Connections**

TCA6416A U61		Schematic Net Name	Connected To			
Pin Name	Pin No.		Pin Name	Pin No.	Reference Designator	Device
SDA	23	I2C0_SDA	See connections shown in Figure 3-17. TCA6416A U61 Addr. 0x21			
SCL	22	I2C0_SCL				
P00	4	VCCPSPLL_EN	2	B	U140	SN74LVC1G08 enable gate for respective power rail
P01	5	MGTRAVCC_EN	2	B	U112	
P02	6	MGTRAVTT_EN	2	B	U130	
P03	7	VCCPSDDRPLL_EN	2	B	U142	
P04	8	MIO26_PMU_INPUT_LS	4	B	U147	SN74AVC1T45
P05	9	PL_PMBUS_ALERT	3	ALERT	U16,U65,U74, U75,U79,U80, U81,U84	INA226 OP AMPS
P06	10	PS_PMBUS_ALERT	3	ALERT	U15,U76,U77,U78,U 87,U85,U86,U88, U92,U93	INA226 OP AMPS
P07	11	MAXIM_PMBUS_ALERT	9,11,13	ALERT	J84.7,U4,U8,U7 U9,U10,U13,U18, U46,U47,U49,U63, U95,U96	MAX15301:9, MAX15303:11, MAX20751:13
P10	13	PL_DDR4_VTERM_EN	7	EN	U35	TPS51200
P11	14	PL_DDR4_VPP_2V5_EN	5	EN	U38	MAX15027
P12	15	PS_DIMM_VDDQ_TO_PSVCCO_ON	C2	ON	U57	TPS22924
P13	16	PS_DIMM_SUSPEND_EN	1	A	U26	OR-GATE
P14	17	PS_DDR4_VTERM_EN	7	EN	U36	TPS51200
P15	18	PS_DDR4_VPP_2V5_EN	5	EN	U39	MAX15027

Table 3-20: **I2C0 Port Expander TCA6416A U97 Connections**

TCA6416A U97		Schematic Net Name	Connected To			
Pin Name	Pin No.		Pin #	Pin Name	Reference Designator	Device
SDA	23	I2C0_SDA	See connections shown in Figure 3-17. TCA6416A U97 Addr. 0x20			
SCL	22	I2C0_SCL				
P00	4	SFP_SI5328_INT_ALM	3	INT_C1B	U20	SI5328B
P01	5	HDMI_SI5324_INT_ALM	3	INT_C1B	U108	SI5319C
P02	6	MAX6643_OT_B	9	OT_B	U128	MAX6643
P03	7	MAX6643_FANFAIL_B	4	FANFAIL_B	U128	MAX6643
P05	9	IIC_MUX_RESET_B	3	RESET_B	U34,U135	TCA9548A
P06	10	GEM3_EXP_RESET_B	3	2A	U59	SN74LVC3G07
P10	13	FMC_HPC0_PRSNT_M2C_B	4	OE	U27,J5.H2	NC7SZ66,FMC0
P11	14	FMC_HPC1_PRSNT_M2C_B	4	OE	U24,J4.H2	NC7SZ66,FMC1

Table 3-21: **I2C0 Multiplexer PCA9544A U60 Address 0x75 Connections**

U60 I2C Mux Port	MUX'd I2C Bus	Reference Designator	Device
0	PS_PMBUS	U76,U77,U78,U87,U85,U86,U93,U88,U15,U92	INA226 Power monitor
1	PL_PMBUS	U79,U81,U80,U84,U16,U65,U74,U75	INA226 Power monitor
2	MAXIM_PMBUS	J84.3,U47,U7,U6,U10,U9,U63,U95,U96,U46,U4,U18, U13,U49,U8	PMBus connector, voltage regulators
3	SYSMON	U135,U1	I2C1 MUX, MPSoC

Note: The PS_PMBUS and PL_PMBUS INA226 power monitor device I2C addresses are listed in Table 3-22. The MAXIM_PMBUS power system device I2C addresses are listed in Table 3-22 and Table 3-54.

Table 3-22: **I2C0 U60 Address 0x75 MUX Target Bus Connections**

Reference Designator	Address	Device
PS_PMBUS (U60 Port 0)		
U76	0x40	INA226 VCCPSINTFP
U77	0x41	INA226 VCCPSINTLP
U78	0x42	INA226 VCCPSAUX
U87	0x43	INA226 VCCPSPLL
U85	0x44	INA226 MGTRAVCC
U86	0x45	INA226 MGTRAVTT
U93	0x46	INA226 VCCO_PSDDR_504
U88	0x47	INA226 VCCOPS
U15	0x4A	INA226 VCCOPS3
U92	0x4B	INA226 VCCPSDDRPLL
PL_PMBUS (U60 Port 1)		
U79	0x40	INA226 VCCINT
U81	0x41	INA226 VCCBRAM
U80	0x42	INA226 VCCAUX
U84	0x43	INA226 VCC1V2
U16	0x44	INA226 VCC3V3
U65	0x45	INA226 VADJ_FMC
U74	0x46	INA226 MGTAVCC
U75	0x47	INA226 MGTAVTT
MAXIM_PMBUS (U60 Port 2)		
J84	NA	PMBUS CONN. SDA PIN 3/SCL PIN 1
U47	0x13	MAX15301 VCCINT
U7	0x14	MAX15303 VCCBRAM
U6	0x15	MAX15303 VCCAUX
U10	0x16	MAX15303 VCC1V2
U9	0x17	MAX15303 VCC3V3
U63	0x18	MAX15301 VADJ_FMC
U95	0x72	MAX20751 MGTAVCC
U96	0x73	MAX20751 MGTAVCC
U46	0x0A	MAX15301 VCCPSINTFP
U4	0x0B	MAX15303 VCCPSINTLP
U18	0x1D	MAX15303 DDR4_DIMM_VDDQ
U13	0x10	MAX15303 VCCOPS

Table 3-22: **I2C0 U60 Address 0x75 MUX Target Bus Connections *(Cont'd)***

Reference Designator	Address	Device
U49	0x1A	MAX15301 UTIL_3V3
U8	0x1B	MAX15303 UTIL_5V0
SYSMON_SDA/SCL (U60 Port 3) (level-shifted via U137)		
U1	0x32	U1 BANK 28 B20/A22

I2C1 (MIO 16-17)

The PS-side I2C1 interface provides access to I2C peripherals through a set of I2C switches. The I2C1 PS-side connection is shared with the PL-side and the system controller. Figure 3-18 shows a high-level view of the I2C1 bus connectivity represented in Table 3-23 and Table 3-24. TCA9548A U34 is set to 0x74 and TCA9548A U135 is set to 0x75.

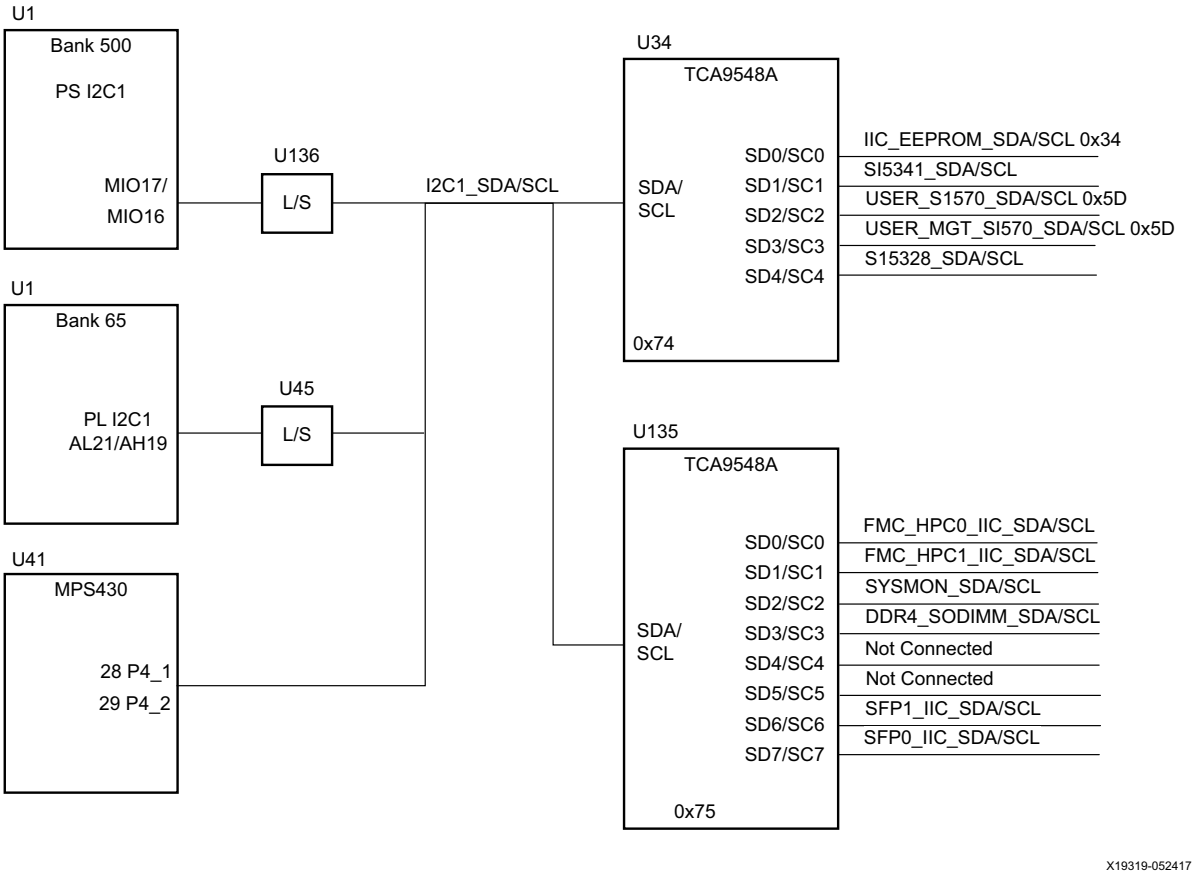


Figure 3-18: **I2C1 Bus Topology**

Table 3-23: **I2C1 TCA9548A U34 Multiplexer Connections**

U34 I2C1 Mux (Addr 0x74) Port	I2C1 Bus Device	Target Device Address
0	EEPROM U23	0X34
1	Si5341 clock U69	0X36
2	USER Si570 clock U42	0X5D
3	USER MGT Si570 clock U56	0X5D
4	Si5328 (clock recovery) U20	0X68
5	No connection	NA
6	No connection	NA
7	No connection	NA

Table 3-24: **I2C1 TCA9548A U135 Multiplexer Connections**

U135 I2C1 Mux (Addr 0x75) Port	I2C1 Bus Device	Target Device Address
0	FMC HPC0 J5	0X##
1	FMC HPC1 J4	0X##
2	SYSMON U1 bank 28	0X32
3	DDR4 SODIMM SKT. J1	0X51
4	No connection	NA
5	No connection	NA
6	SFP1 P2	0X50
7	SFP0 P1	0X50

UART0 (MIO 18-19)

This is the primary Zynq UltraScale+ MPSoC PS-side UART interface and is connected to the U40 CP2108 USB-to-Quad-UART bridge with port assignments as listed in Table 3-25. PS-side UART0 is accessed through the U40 CP2108 USB-to-Quad-UART bridge port 0. The CP2108 channel 0 PS-side UART interface circuit is shown in Figure 3-19. The connections from XCZU7EV U1 to CP2108 U40 via L/S U54 are listed in Table 3-26.

IMPORTANT: *Use SiLabs CP210X VCP driver version 6.7.0 or later for proper USB enumeration as identified in Table 3-27.*

Table 3-25: **CP2108 UART Assignments**

CP2108 U40	Zynq UltraScale+ MPSoC
UART0	PS_UART0 (MIO 18-19)
UART1	PS_UART1 (MIO 20-21)
UART2	PL-UART (HD bank 64)
UART3	U41 system controller UART

UART1 (MIO 20-21)

PS-side UART1 is accessed through the U40 CP2108 USB-to-Quad-UART bridge port 1. The CP2108 channel 1 PS-side UART interface circuit is shown in Figure 3-19. The connections from XCZU7EV U1 to CP2108 U40 via L/S U54 are listed in Table 3-26.

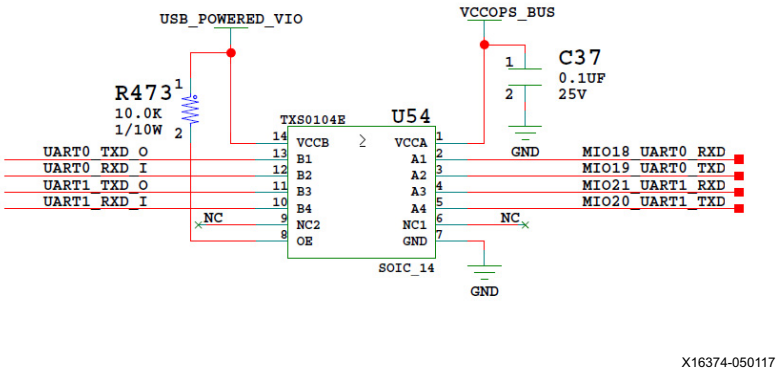


Figure 3-19: **CP2108 Channels 0 and 1 PS-Side UART Interface**

Table 3-26: **XCZU7EV U1 PS-Side to CP2108 U40 Connections via L/S U54**

XCZU7EV U1		Net Name	CP2108 U40	
Pin Name	**Pin #**	**Net Name**	**Pin Name**	**Pin #**
PS_MIO18	F27	MIO18_UART0_RXD	TX_0	57
PS_MIO19	B28	MIO19_UART0_TXD	RX_0	56
PS_MIO21	C28	MIO21_UART1_RXD	TX_1	49
PS_MIO20	E29	MIO20_UART1_TXD	RX_1	48

GPIO (MIO 22-23)

PS-side pushbutton SW19 is connected to MIO22 (pin U1.F28). PS-side LED DS50, physically placed adjacent to the pushbutton, is connected to MIO23 (pin U1.B29).

CAN1 (MIO 24-25)

The PS-side CAN bus TX and RX MIO nets are wired through TXS0104E level-translator U33 and TI SN65HVD232 CAN-bus transceiver U122 to the 0.1 inch pitch 8-pin male header J98 (see Figure 3-20 and Figure 3-21).

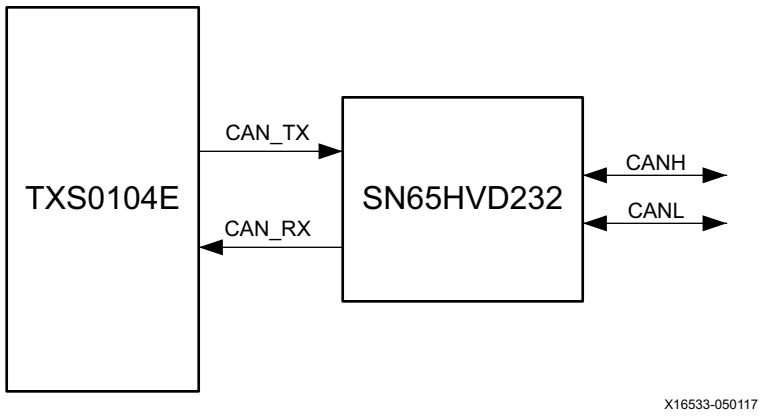


Figure 3-20: **PS-Side CAN Bus Interface Diagram**

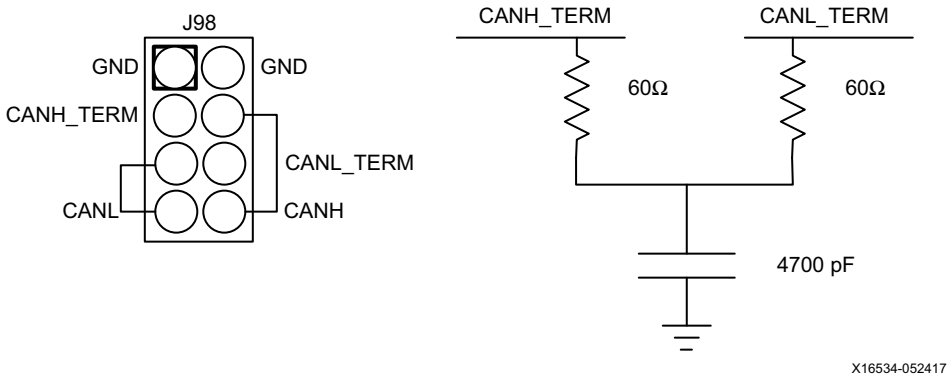


Figure 3-21: **PS-Side CAN Bus Interface Connector**

Platform Management Unit GPI (MIO 26)

PS-side MIO 26 is reserved as an input to the platform management unit (PMU) for indicating a warm boot. PS bank 501 MIO26 (U1.A29) is connected to the I2C0 U61 TCA6416APWR bus expander (port P04 U61.8) through L/S U147 SN74AVC1T45. See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] for more details on the PMU interface.

DisplayPort DPAUX (MIO 27-30)

The Zynq UltraScale+ MPSoC provides a VESA DisplayPort 1.2 source-only controller that supports up to two lanes of main link data at rates of 1.62 Gb/s, 2.70 Gb/s, or 5.40 Gb/s. The DisplayPort standard defines an auxiliary channel that uses LVDS signaling at a 1 Mb/s data rate, which is translated from single-ended MIO signals to the differential DisplayPort AUX channel, DPAUX (see Table 3-27). The DisplayPort circuit is shown in Figure 3-22.

Table 3-27: **DPAUX/MIO Connections**

XCZU7EV (U1) Pin	Net Name	Level Shifter U114	
		Pin Name	Pin #
A33	MIO30_DP_AUX_IN	2A1	8
A32	MIO29_DP_OE	1A2	7
A31	MIO28_DP_HPD	2A2	9
A30	MIO27_DP_AUX_OUT	1A1	6

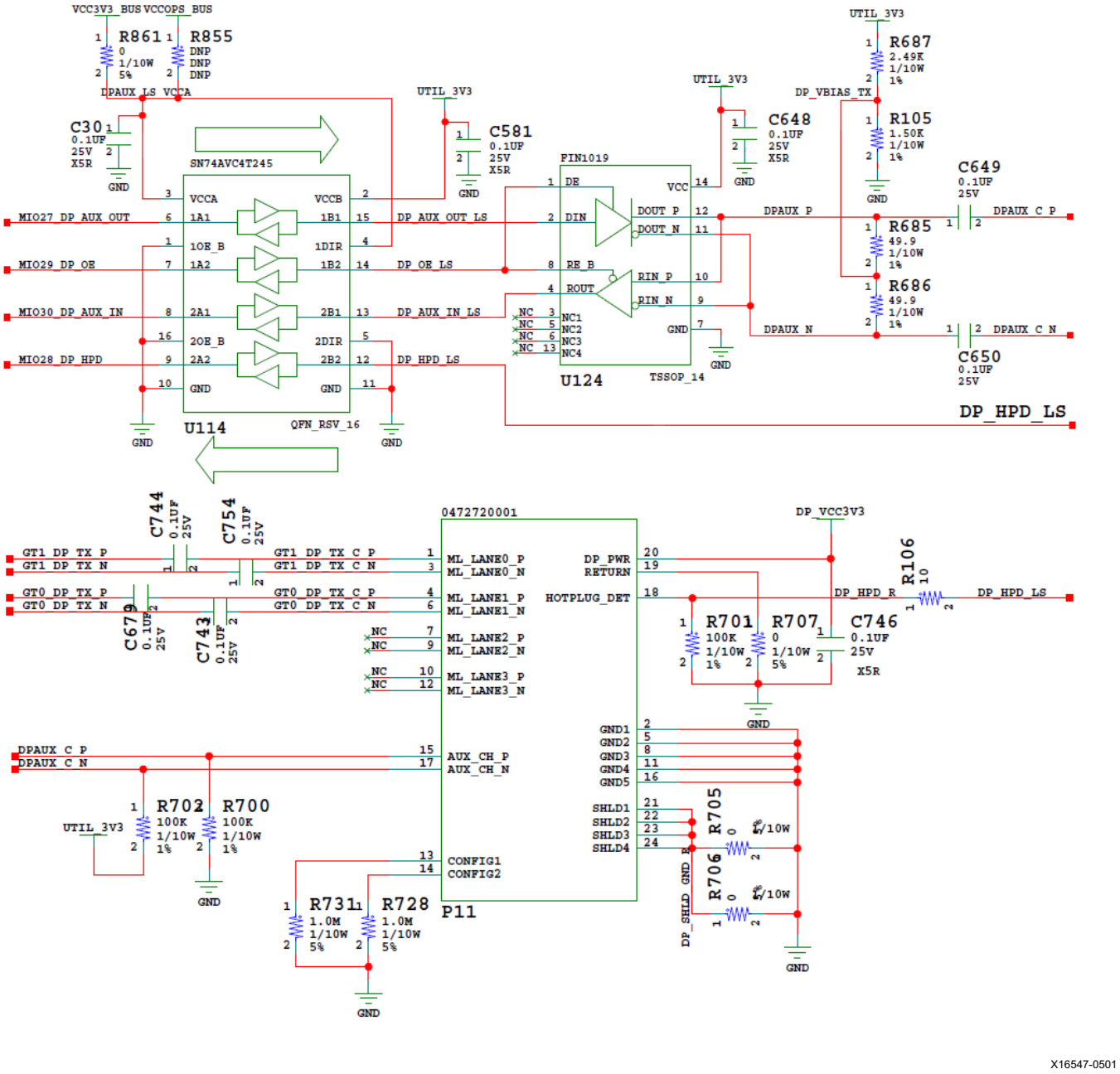


Figure 3-22: **DisplayPort Circuit**

PMU GPO (MIO 32-37)

The PMU within the Zynq UltraScale+ MPSoC signals power domain changes using the PMU output pins for deep-sleep mode. The Zynq UltraScale+ MPSoC PMU GPO pins are connected to inputs of the MSP430 system controller via TXS0108E level-shifter U141. The connections from MPSoC U1 bank 501 to MSP430 U41 are listed in Table 3-28.

Table 3-28: **XCZU7EV U1 to MSP430 Connections**

XCZU7EV (U1) Pin	Net Name	MSP430 U41	
		Pin Name	Pin #
C33	MIO37_PMU_GPO5	P1_0	13
C32	MIO36_PMU_GPO4	P1_1	14
C31	MIO35_PMU_GPO3	P1_2	15
B34	MIO34_PMU_GPO2	P1_3	16
B33	MIO33_PMU_GPO1	P1_4	17
B31	MIO32_PMU_GPO0	P1_5	18

Through the I2C0 bus MPSoC MIO pins, the PMU has access to the board power controllers and power monitors. See Figure 3-17, page 61 for more details.

See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] for more details about the PMU interface.

HDMI Video Output

[Figure 2-1, callout 14]

The ZCU106 board provides an HDMI® video output using a TI SN65DP159RGZ re-timer at U94. The output is provided on a TE Connectivity 1888811-1 right-angle dual-stacked HDMI type-A receptacle at P7. The SN65DP159RGZ device is a dual mode DisplayPort to transition-minimized differential signal (TMDS) re-timer supporting digital video interface (DVI) 1.0, HDMI 1.4b, and 2.0 output signals.

The SN65DP159RGZ device supports the dual mode standard version 1.1 type 1 and type 2 through the digital down converter (DDC) link or AUX channel. The SN65DP159RGZ device supports data rates up to 6 Gb/s per data lane to support Ultra HD (4K x 2K/60 Hz) 8-bits per color high-resolution video and HDTV with 16-bit color depth at 1080p (1920 x 1080/60 Hz). The SN65DP159RGZ device can automatically configure itself as a re-driver at data rates <1 Gb/s, or as a re-timer at more than this data rate. This feature can be turned off with I2C programming.

The HDMI block diagram, the TX interface circuit, and the RX interface circuit are shown in Figure 3-23, Figure 3-24, and Figure 3-25, respectively. The XCZU7EV MPSoC U1 to HDMI circuit connections are listed in Table 3-29.

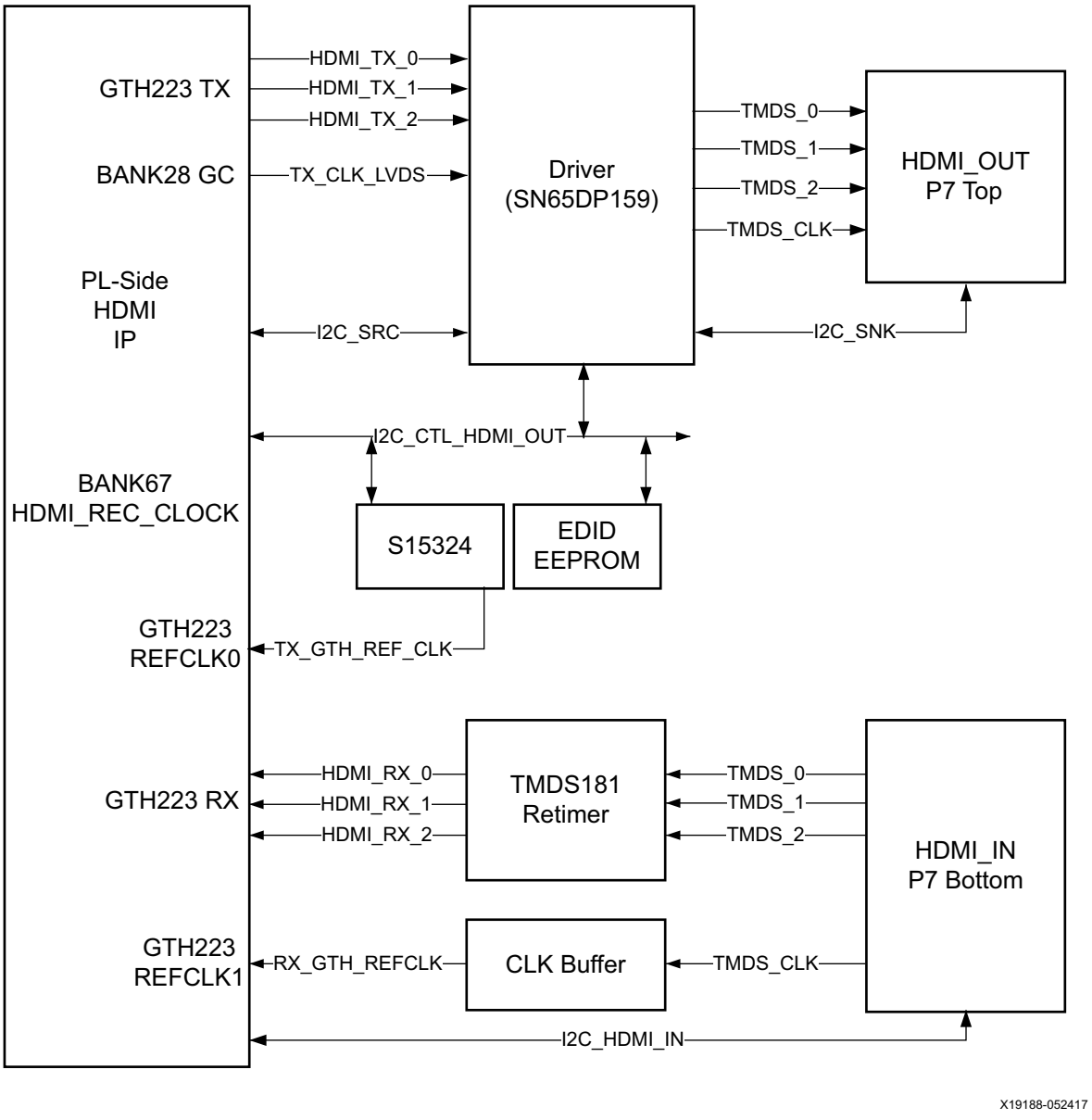


Figure 3-23: **HDMI Interface Block Diagram**

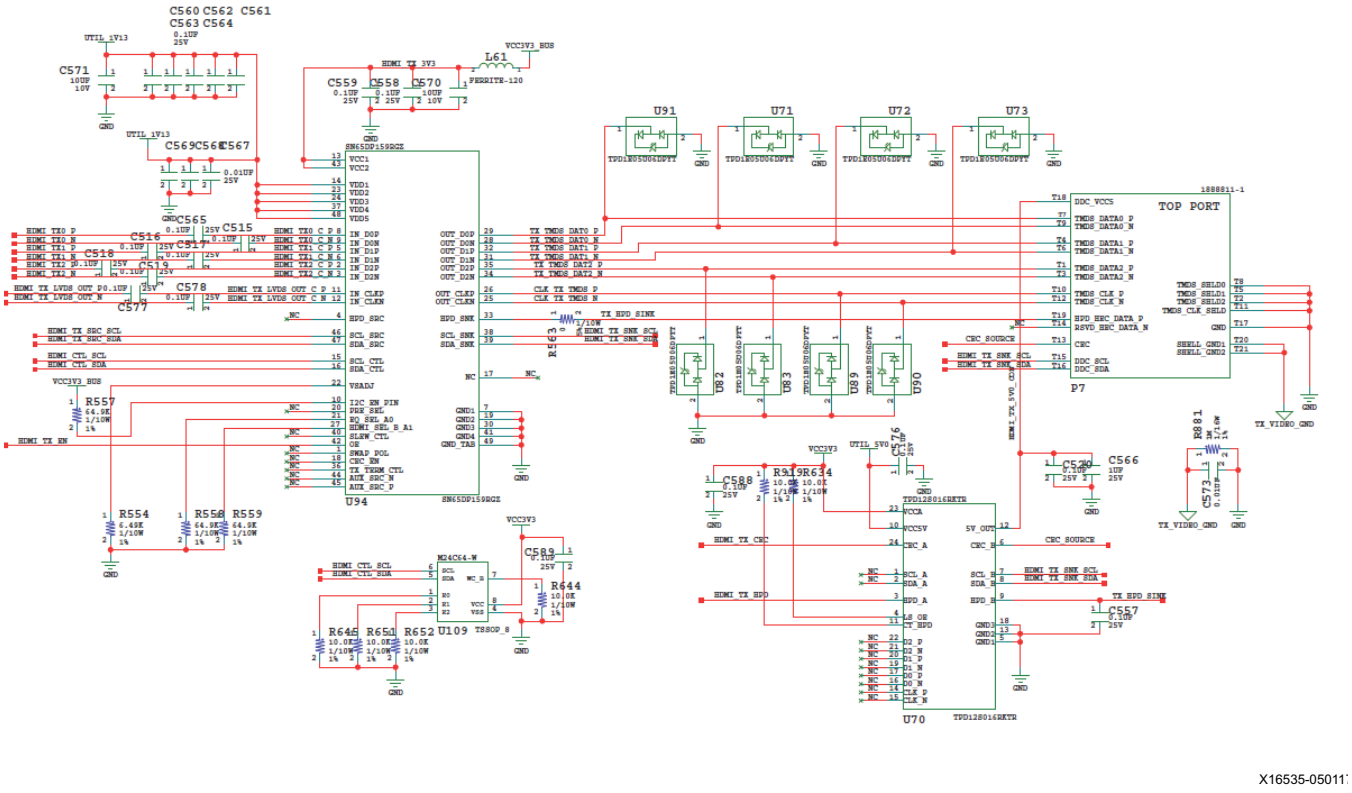


Figure 3-24: **HDMI TX Interface Circuit**

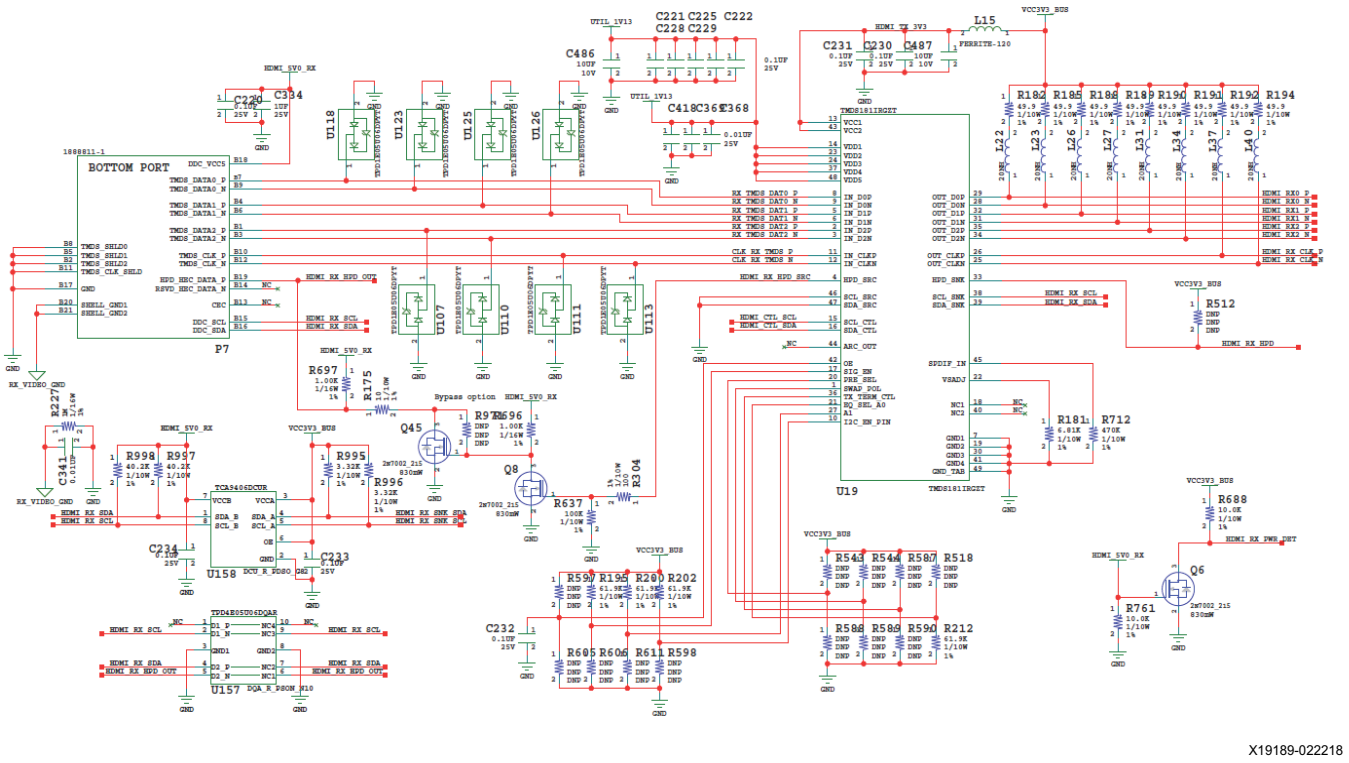


Figure 3-25: **HDMI RX Interface Circuit**

Table 3-29: **HDMI Connections to FPGA U1**

XCZU7EV (U1) Pin	Schematic Net Name	I/O Standard	Connected Component		
			Pin	Name	Device
AN6	HDMI_TX0_P	(1)	8	IN_D0P	SN65DP159 (U94)
AN5	HDMI_TX0_N	(1)	9	IN_D0N	
AM4	HDMI_TX1_P	(1)	5	IN_D1P	
AM3	HDMI_TX1_N	(1)	6	IN_D1N	
AL6	HDMI_TX2_P	(1)	2	IN_D2P	
AL5	HDMI_TX2_N	(1)	3	IN_D2N	
G21	HDMI_TX_LVDS_OUT_P	LVDS	11	IN_CLKP	
F21	HDMI_TX_LVDS_OUT_N	LVDS	12	IN_CLKN	
N8	HDMI_TX_SRC_SCL	LVCMOS33	46	SCL_SRC	
N9	HDMI_TX_SRC_SDA	LVCMOS33	47	SDA_SRC	
N11	HDMI_TX_EN	LVCMOS33	42	OE	
M12	HDMI_TX_CEC	LVCMOS33	24	CEC_A	TPD12S016RK (U70)
N13	HDMI_TX_HPD	LVCMOS33	3	HPD_A	

Table 3-29: **HDMI Connections to FPGA U1 *(Cont'd)***

XCZU7EV (U1) Pin	Schematic Net Name	I/O Standard	Connected Component		
			Pin	Name	Device
G8	HDMI_SI5324_LOL	LVCMOS33	18	LOL	SI5324C (U108)
H8	HDMI_SI5324_RST	LVCMOS33	1	RST_B	
G14	HDMI_REC_CLOCK_C_P	LVDS	16	CKIN1_P	
F13	HDMI_REC_CLOCK_C_N	LVDS	17	CKIN1_N	
AD8	HDMI_SI5324_OUT_C_P	(1)	28	CKOUT1_P	
AD7	HDMI_SI5324_OUT_C_N	(1)	29	CKOUT1_N	
AP4	HDMI_RX0_C_P	(1)	B7	TMDS_DATA0_P	HDMI bottom port (P7)
AP3	HDMI_RX0_C_N	(1)	B9	TMDS_DATA0_N	
AN2	HDMI_RX1_C_P	(1)	B4	TMDS_DATA1_P	
AN1	HDMI_RX1_C_N	(1)	B6	TMDS_DATA1_N	
AL2	HDMI_RX2_C_P	(1)	B1	TMDS_DATA2_P	
AL1	HDMI_RX2_C_N	(1)	B3	TMDS_DATA2_N	
AC10	HDMI_RX_CLK_C_P	(1)	B10	TMDS_CLK_P	
AC9	HDMI_RX_CLK_C_N	(1)	B12	TMDS_CLK_N	
M8	HDMI_RX_PWR_DET	LVCMOS33	3	D	Q46
M10	HDMI_RX_HPD	LVCMOS33	1	G	Q41
N12	HDMI_CTL_SCL	LVCMOS33	15	SCL_CTL	(2)
P12	HDMI_CTL_SDA	LVCMOS33	16	SDA_CTL	
M9	HDMI_RX_SNK_SCL	LVCMOS33	4	SCL_A	TCA9406DCUR (U158)
M11	HDMI_RX_SNK_SDA	LVCMOS33	5	SDA_A	

Notes:

1. U1 MGT (I/O standards do not apply).
2. TMDS181IRG (U19), SN65DP159 (U94), M24C64-W (U109), and SI5324C (U108).

HDMI Clock Recovery

[Figure 2-1, callout 41]

The ZCU106 board includes a Silicon Labs Si5319C jitter attenuator U108 (2 kHz – 945 MHz). The FPGA can output the RX recovered clock to a differential I/O pair on I/O bank 67 (HDMI_REC_CLOCK_C_P, pin G14 and HDMI_REC_CLOCK_C_N, pin F13) for jitter attenuation. The jitter attenuated clock (HDMI_SI5324_OUT_C_P (U108 pin 28), HDMI_SI5324_OUT_C_N (U108 pin 29) is then routed as a series capacitor coupled reference clock to GTH Quad 223 inputs MGTREFCLK0P (U1 pin AD8) and MGTREFCLK0N (U1 pin AD7).

The Si5319C jitter attenuator is used to generate the reference clock for the HDMI transmitter subsystem. When the HDMI transmitter is used in standalone mode, the Si5319C operates in free-running mode and uses an external oscillator as the reference. When the HDMI transmitter is used in pass-through mode, the Si5319C generates a jitter-attenuated reference clock to drive the HDMI transmitter subsystem with a phase-aligned version of the HDMI Rx subsystem HMDI Rx TMDS clock, so that they are phase aligned. The SI5319C clock and jitter enable functions are controlled by HDMI IP. Communication with the SI5319C is available over the HDMI_CTL_SDA/SCL bus connected to the XCZU7EV MPSoC U1 PL bank 87. The jitter attenuated clock circuit is shown in Figure 3-26.

IMPORTANT: *The Silicon Labs Si5319C U108 pin 1 reset net HDMI_SI5324_RST must be driven High to enable the device. U108 pin 1 net HDMI_SI5324_RST is connected to FPGA U1 bank 87 pin H8.*

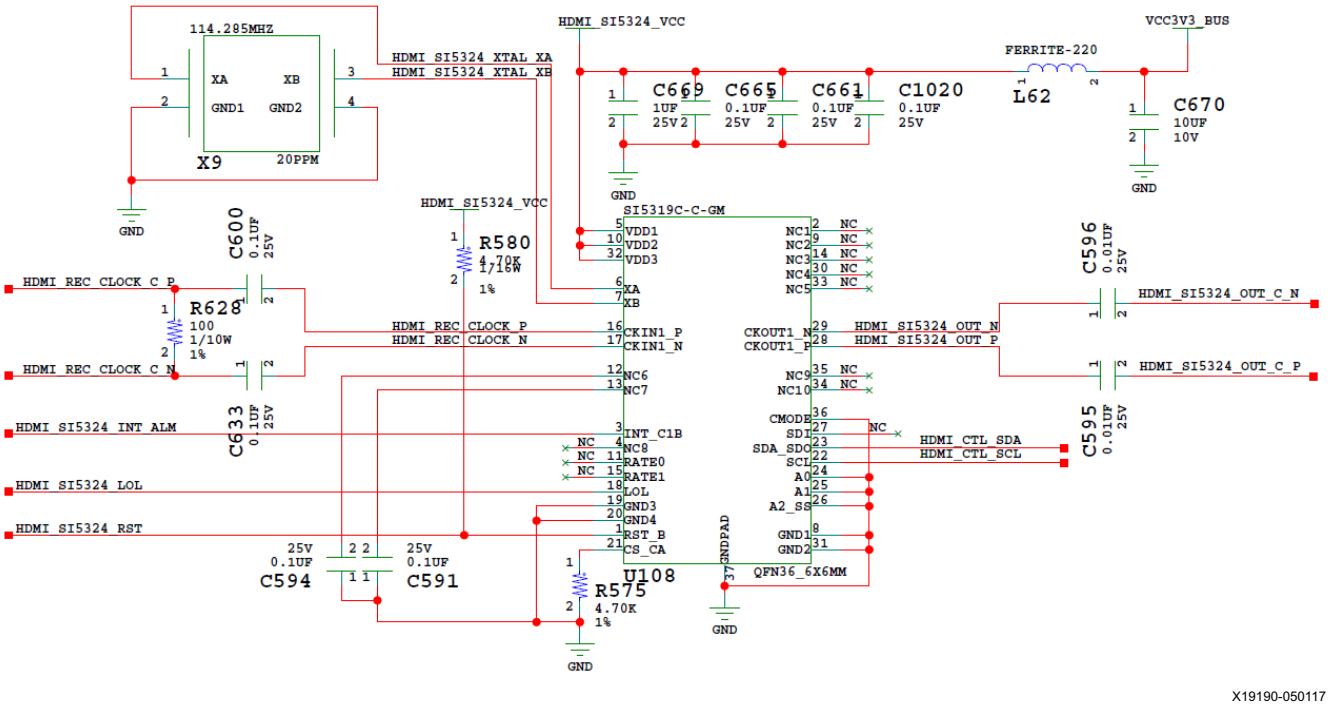


Figure 3-26: **HDMI Interface Clock Recovery**

SDI Video

[Figure 2-1, callout 45]

12G-SDI and SMPTE ST-2082-1 define a bit-serial data interface for the transport of 12 Gb/s [nominal] component digital signals or packetized data along with the mapping of various source image formats to the bit-serial data structure. The SDI video circuit is shown in Figure 3-27.

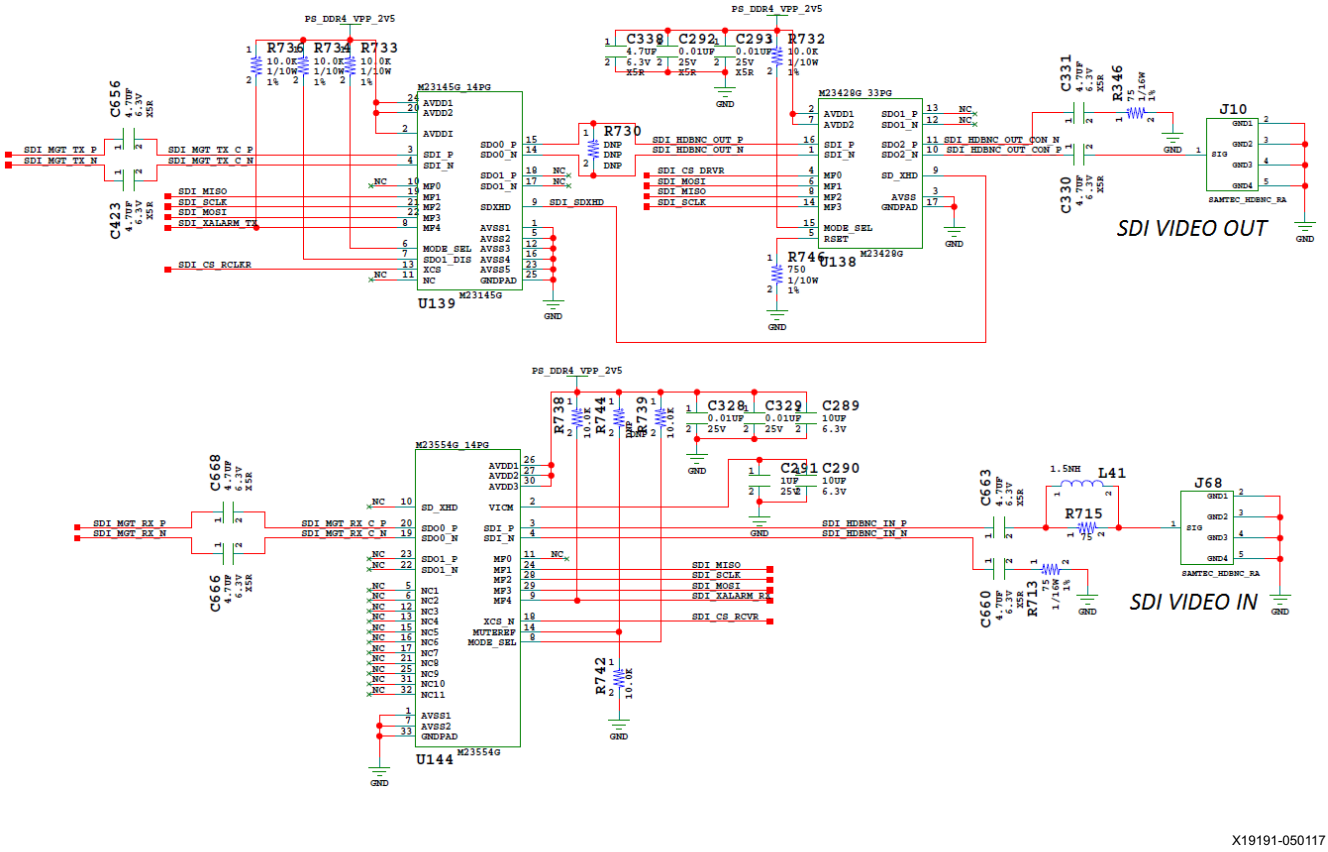


Figure 3-27: **SDI Video**

The SDI video circuit connections to the XCZU7EV MPSoC U1 are listed in Table 3-30.

Table 3-30: **SDI Video Connections to MPSoC U1**

XCZU7EV (U1) Pin	Schematic Net Name	I/O Standard	Connected Component		
			Pin	Name	Device
H23	SDI_MISO(4)	LVCMOS18	19	MF1	U139 M23145G
			8	MF2	U138 M23428G
			24	MF1	U144 M23544G
B21	SDI_SCLK(3)	LVCMOS18	21	MF2	U139 M23145G
			14	MF3	U138 M23428G
			28	MF2	U144 M23544G
L21	SDI_MOSI(3)	LVCMOS18	22	MF3	U139 M23145G
			6	MF1	U138 M23428G
			29	MF3	U144 M23544G
C14	SDI_XALARM_TX(4)	LVCMOS18	8	MF4	U139 M23145G
A9	SDI_CS_RCLKR(3)	LVCMOS18	13	XCS	
AC5	SDI_MGT_TX_N(2)	(1)	4	SDI_N	
AC6	SDI_MGT_TX_P(2)	(1)	3	SDI_P	
J19	SDI_CS_DRVR(3)	LVCMOS18	4	MF0	U138 M23428G
J20	SDI_CS_RCVR(3)	LVCMOS18	18	XCS_N	U144 M23544G
E13	SDI_XALARM_RX(4)	LVCMOS18	9	MF4	
AC1	SDI_MGT_RX_N(2)	(1)	19	SDO0_N	
AC2	SDI_MGT_RX_P(2)	(1)	20	SDO0_P	

Notes:

1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.
3. Level-shifted V_{ADJ_FMC} to PS_DDR4_VPP_2V5 (1.8V-to-2.5V) at U146 SN74AVC8T245.
4. Level-shifted V_{ADJ_FMC} to PS_DDR4_VPP_2V5 (1.8V-to-2.5V) at U145 SN74AVC4T245.

AES3 Audio

[Figure 2-1, callout 44]

AES3 (also referred to as AES/EBU) is a standard for the exchange of digital audio signals between professional audio devices. AES3 was jointly developed by the Audio Engineering Society (AES) and the European Broadcasting Union (EBU). An AES3 signal can carry two channels of PCM audio over several transmission media including balanced lines, unbalanced lines, and optical fiber. AES3 has been incorporated into the International Electrotechnical Commission's standard IEC 60958. Ref_1_IEC 60958-1 2008, Ref_2_IEC_60958-1_2ndEd_2004-03. The AES3 audio circuit is shown in Figure 3-28 and the connections are listed in Table 3-31.

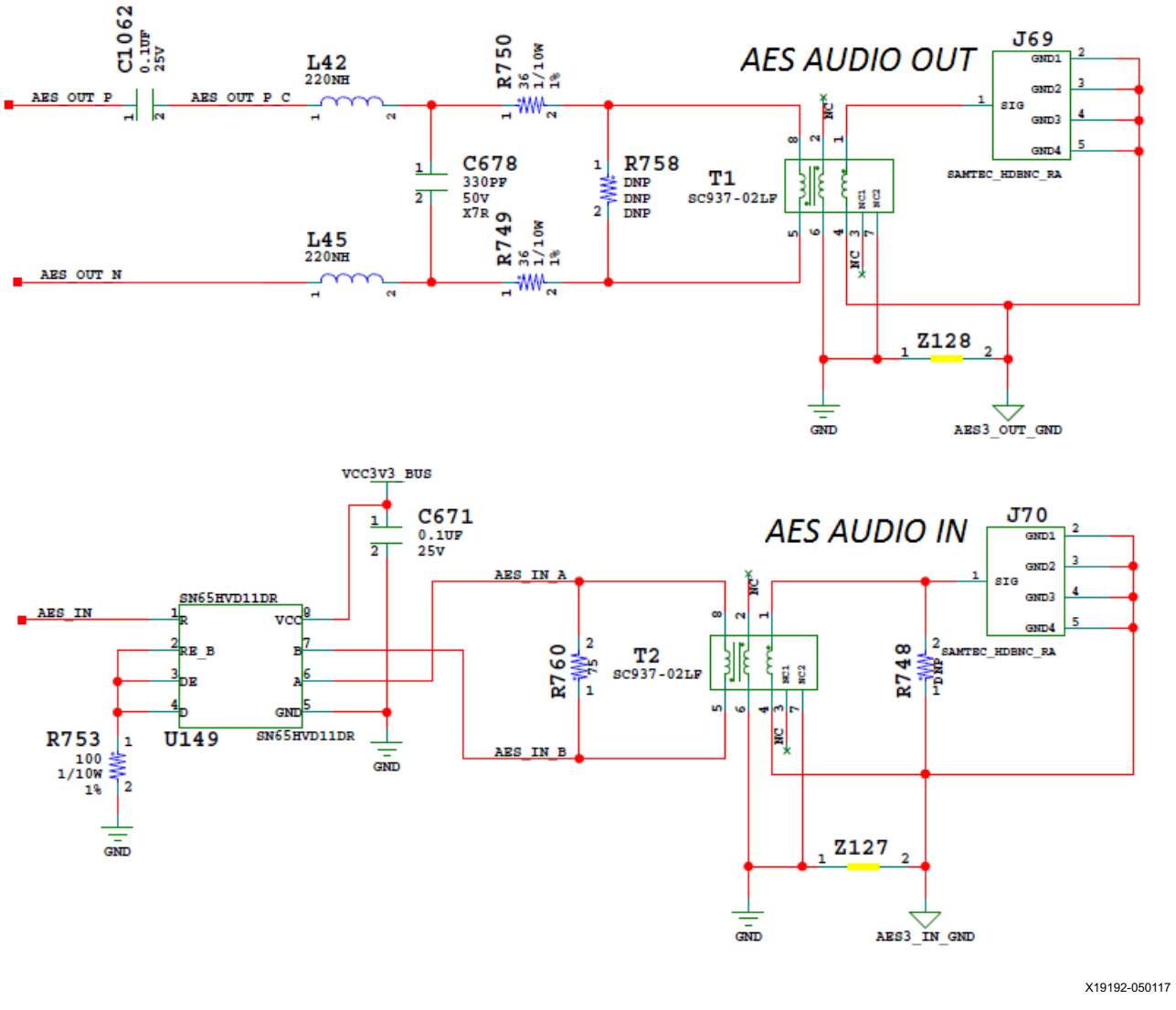


Figure 3-28: **AES Audio**

Table 3-31: **AES3 Audio Connections to MPSoC U1**

XCZU7EV (U1) Pin	Schematic Net Name	I/O Standard	Connected Component		
			Pin	Name	Device
G7	AES_IN	LVCMOS33	1	R	U149 SN65HVD11DR
AE13	AES_OUT_P(1)	(3)	8		T1 SC937-02LF
AF13	AES_OUT_N(2)	(3)	5		

Notes:

1. Series resistor, inductor, and capacitor coupled.
2. Series resistor and inductor coupled.
3. Transformer coupled by T1 SC937-02LF.

SFP/SFP+ Connectors

[Figure 2-1, callout 18]

The ZCU106 board contains a small form-factor pluggable (SFP+) 1x2 dual-connector (P1, P2) and cage assembly that accepts SFP or SFP+ modules. Figure 3-29 shows a typical SFP+ module connector circuitry implementation. Table 3-32 lists the connections between the dual connectors and the XCZU7EV MPSoC.

Note: The SFPx_TX_DISABLE_TRANS default 2-pin jumper is On, which means the SFPx_TX_DISABLE_TRANS net is pulled Low, enabling the TX output of the SFP module.

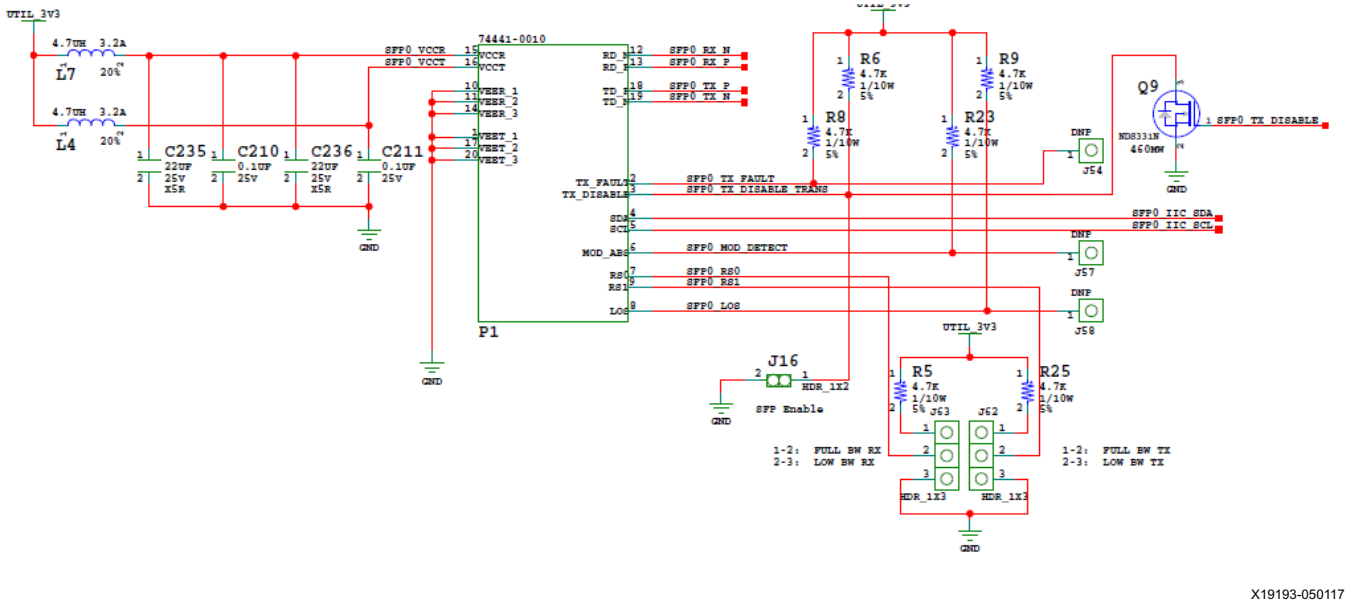


Figure 3-29: **Typical SFP Interface**

Table 3-32: **ZCU106 FPGA U1 to SFP0 and SFP1 Module Connections**

XCZU7EV (U1) Pin	Net Name	Pin No.	Pin Name	SFP/SFP+ Module
Y4	SFP0_TX_P	18	TD_P	P1
Y3	SFP0_TX_N	19	TD_N	
AA2	SFP0_RX_P	13	RD_P	
AA1	SFP0_RX_N	12	RD_N	
AE22	SFP0_TX_DISABLE_B	3	TX_DISABLE	
W6	SFP1_TX_P	18	TD_P	P2
W5	SFP1_TX_N	19	TD_N	
W2	SFP1_RX_P	13	RD_P	
W1	SFP1_RX_N	12	RD_N	
AF20	SFP1_TX_DISABLE_B	3	TX_DISABLE	

Notes:

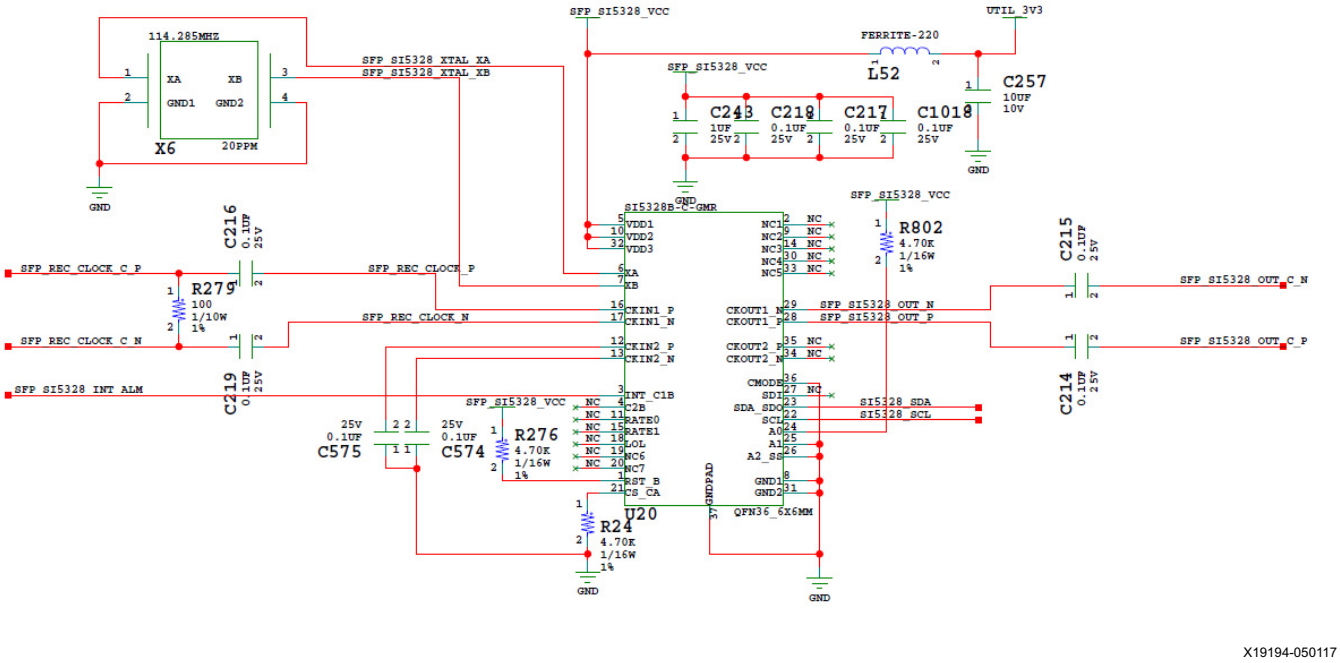
1. SFPx_TX_DISABLE_B nets implement the LVCMOS33 standard.

SFP/SFP+ Clock Recovery

[Figure 2-1, callout 11]

The ZCU106 board includes a Silicon Labs Si5328B jitter attenuator U20 (8 kHz – 808 MHz). The FPGA can output the RX recovered clock to a differential I/O pair on I/O bank 68 (SFP_REC_CLOCK_C_P, pin H11 and SFP_REC_CLOCK_C_N, pin G11) for jitter attenuation. The jitter attenuated clock (SFP_SI5328_OUT_C_P (U20 pin 28), SFP_SI5328_OUT_C_N (U20 pin 29)) is then routed as a series capacitor coupled reference clock to GTH Quad 225 inputs MGTREFCLK1P (U1 pin W10) and MGTREFCLK1N (U1 pin W9).

The primary purpose of this clock is to support synchronous protocols such as CPRI or OBSAI to perform clock recovery from a user-supplied SFP/SFP+ module and use the jitter attenuated recovered clock to drive the reference clock inputs of a GTH transceiver. The system controller configures the SI5328B in free-run mode (see TI MSP430 System Controller, page 116). The jitter attenuated clock circuit is shown in Figure 3-30.



X19194-050117

Figure 3-30: **SFP/SFP+ Clock Recovery**

User PMOD GPIO Headers

[Figure 2-1, callout 20, 21]

The ZCU106 evaluation board supports two PMOD GPIO headers J55 (right-angle female) and J87 (vertical male). The 3.3V PMOD nets are level-shifted and wired to the XCZU7EV device U1 banks 28, 66, and 68. Figure 3-31 shows the GPIO PMOD headers J55 and J87. Table 3-33 lists the connections between the XCZU7EV MPSoC and the PMOD connectors. Maximum PMOD interface speed is 110 Mb/s.

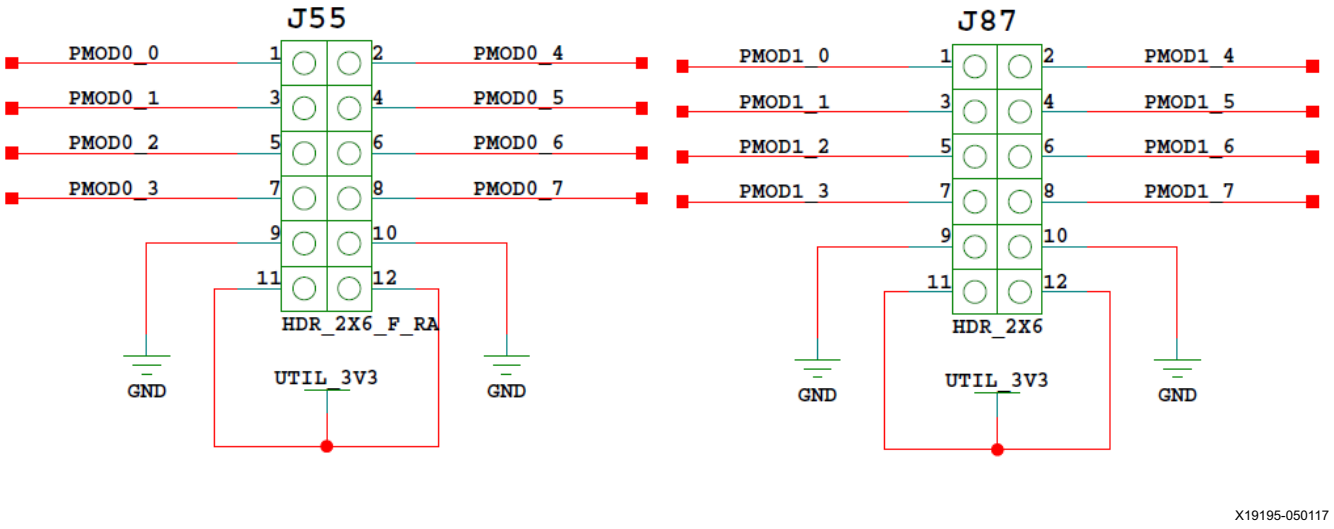


Figure 3-31: **PMOD Connectors**

Table 3-33: **XCZU7EV U1 to PMOD Connections**

XCZU7EV (U1) Pin	Net Name	I/O Standard	PMOD Pin
B23	PMOD0_0	LVCMOS18	J55.1
A23	PMOD0_1	LVCMOS18	J55.3
F25	PMOD0_2	LVCMOS18	J55.5
E20	PMOD0_3	LVCMOS18	J55.7
K24	PMOD0_4	LVCMOS18	J55.2
L23	PMOD0_5	LVCMOS18	J55.4
L22	PMOD0_6	LVCMOS18	J55.6
D7	PMOD0_7	LVCMOS18	J55.8
AN8	PMOD1_0	LVCMOS18	J87.1
AN9	PMOD1_1	LVCMOS18	J87.3
AP11	PMOD1_2	LVCMOS18	J87.5
AN11	PMOD1_3	LVCMOS18	J87.7
AP9	PMOD1_4	LVCMOS18	J87.2

Table 3-33: **XCZU7EV U1 to PMOD Connections *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	I/O Standard	PMOD Pin
AP10	PMOD1_5	LVCMOS18	J87.4
AP12	PMOD1_6	LVCMOS18	J87.6
AN12	PMOD1_7	LVCMOS18	J77.8

Prototype Header

[Figure 2-1, callout 42]

The ZCU106 evaluation board provides a 2x12 male pin prototype header J3 that makes ten GPIO connections available. Figure 3-32 shows connector J3 with its MPSoC (U1) connections.

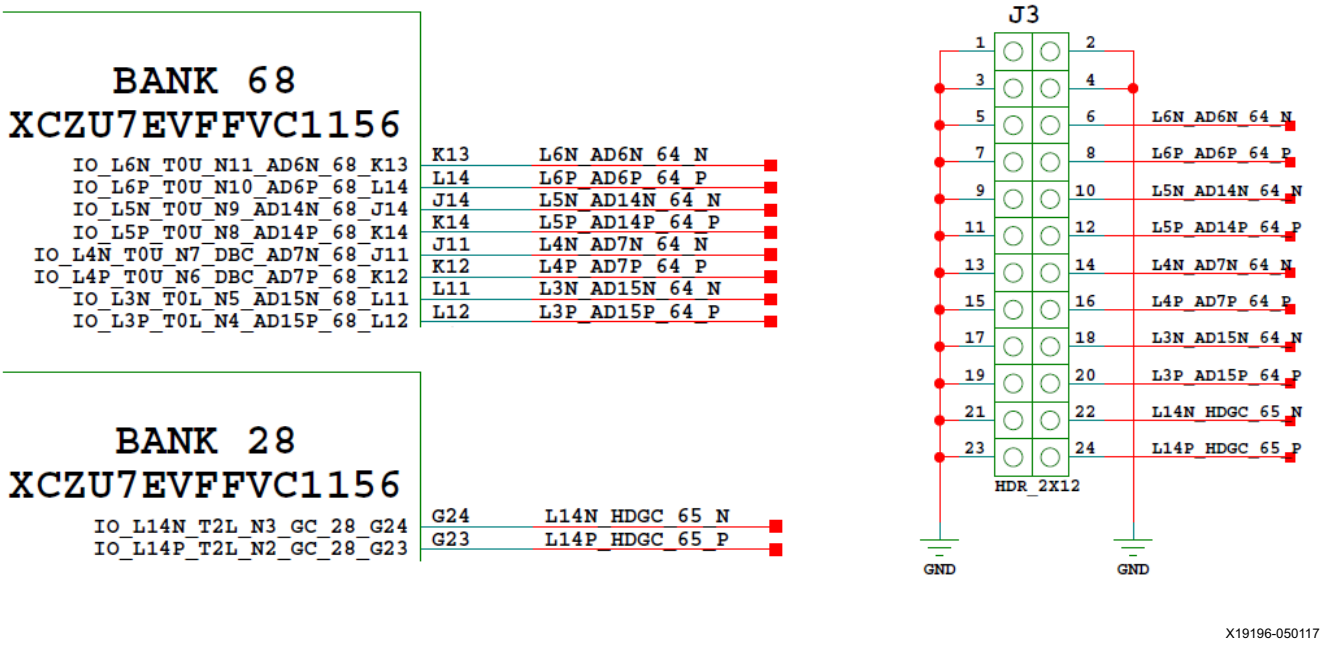


Figure 3-32: **Prototype Header J3**

Table 3-34 lists the connections between the XCZU7EV MPSoC and the prototype header.

Table 3-34: **Prototype Header J3 Connections to the XCZU7EV MPSoC**

XCZU7EV (U1) Pin	Net Name	I/O Standard	Prototype Header J3 Pin
L14	L6P_AD6P_64_P	LVCMOS18	8
K13	L6N_AD6N_64_N	LVCMOS18	6
K14	L5P_AD14P_64_P	LVCMOS18	12
J14	L5N_AD14N_64_N	LVCMOS18	10
K12	L4P_AD7P_64_P	LVCMOS18	16
J11	L4N_AD7N_64_N	LVCMOS18	14
L12	L3P_AD15P_64_P	LVCMOS18	20
L11	L3N_AD15N_64_N	LVCMOS18	18
G23	L14P_HDGC_65_P	LVCMOS18	24
G24	L14N_HDGC_65_N	LVCMOS18	22

User I2C0 Receptacle

[Figure 2-1, callout 21]

The ZCU106 evaluation board supports a PMOD 2X6 receptacle (right-angle female) J160. Figure 3-33 shows the I2C0 PMOD receptacle J160. The I2C0 nets are a branch of the I2C0 main bus (see Figure 3-17, page 61 and I2C0 (MIO 14-15), page 60 for more details).

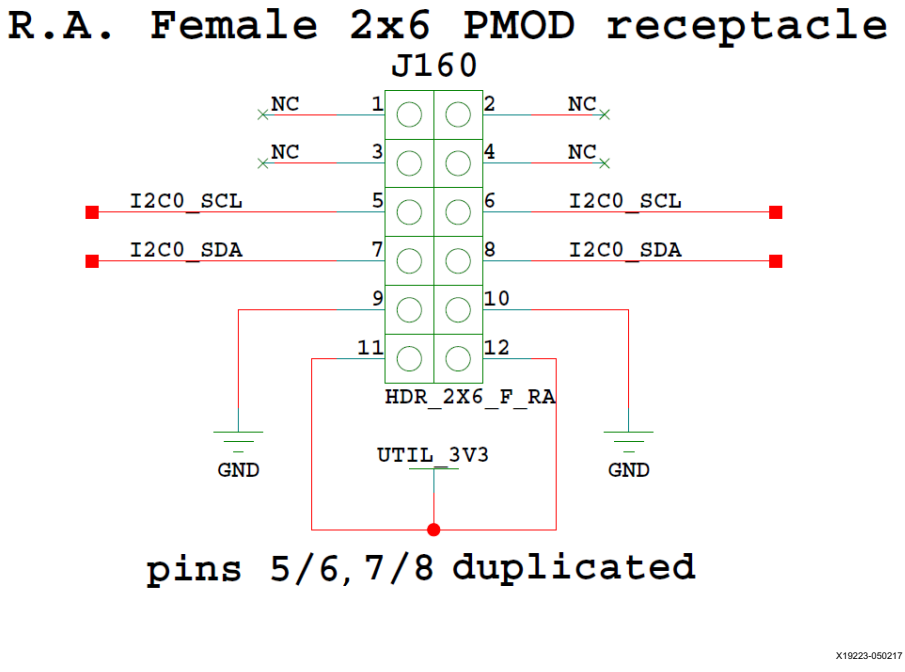


Figure 3-33: **J160 PMOD I2C0 Right-Angle Receptacle**

User I/O

[Figure 2-1, callouts 22-25]

The ZCU106 board provides these user and general purpose I/Os:

- Eight user LEDs (callout 22)
  - GPIO_LED[7-0]: DS38, DS37, DS39, DS40, DS41, DS42, DS43, DS44
- Five user pushbuttons and CPU reset switch (callouts 24 and 25)
  - GPIO_SW_[NESWC]: SW18, SW17, SW16, SW14, SW15
  - CPU_RESET: SW20
- 8-position user DIP switch (callout 23)
  - GPIO_DIP_SW[7:0]: SW13

Figure 3-34 through Figure 3-36 show the GPIO circuits. Table 3-35 lists the GPIO to XCZU9EG U1 connections.

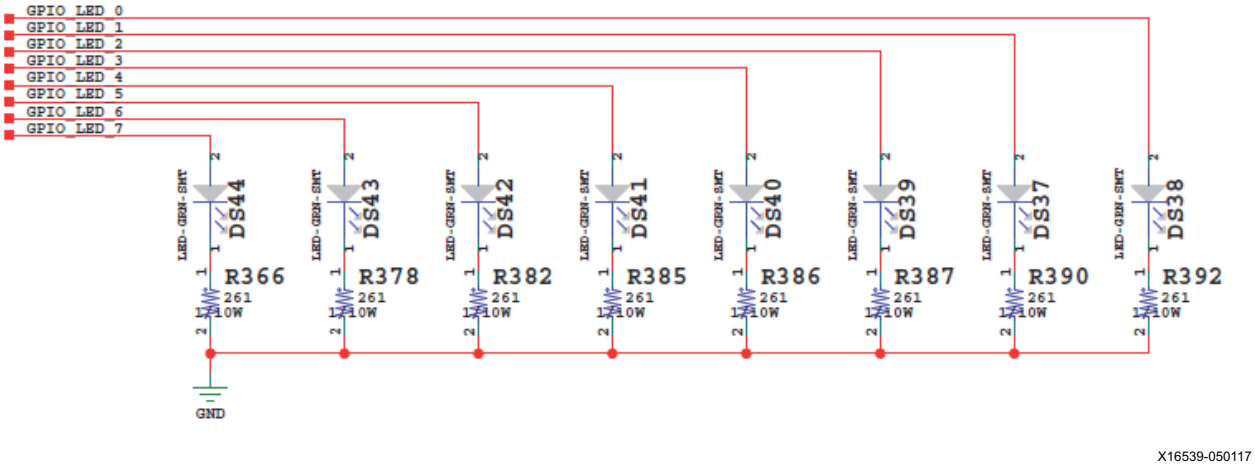


Figure 3-34: **GPIO LEDs**

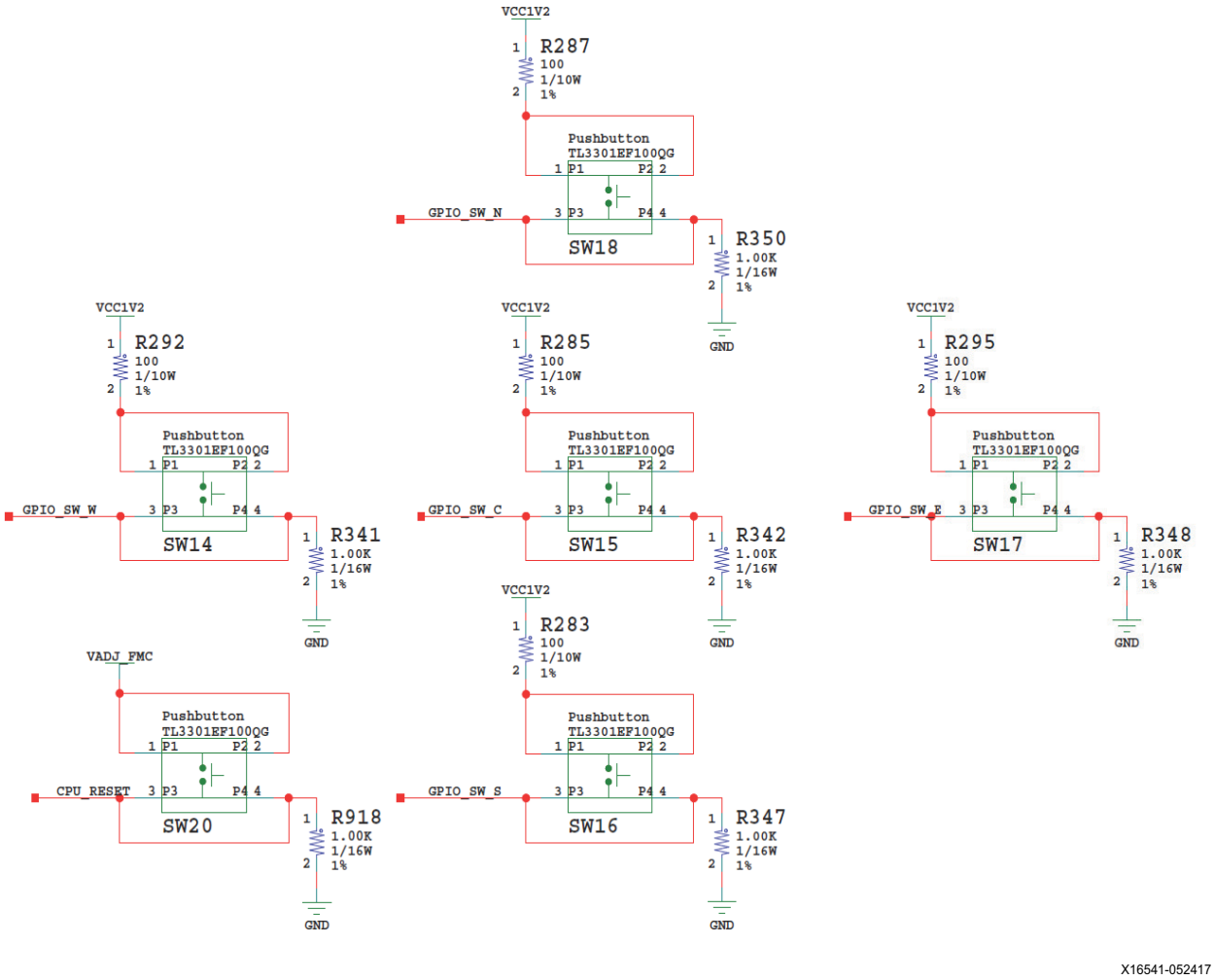


Figure 3-35: **GPIO Pushbutton Switches**

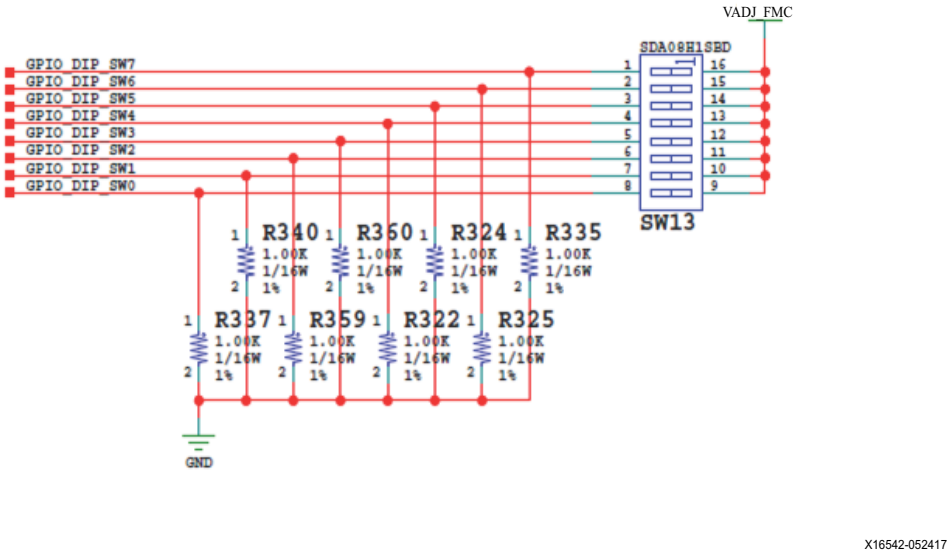


Figure 3-36: **GPIO 8-Pole DIP Switch**

Table 3-35: **XCZU7EV U1 to GPIO Connections**

XCZU7EV (U1) Pin	Net Name	I/O Standard	Device
GPIO LEDs (Active High)(1)			
AL11	GPIO_LED_0	LVCMOS12	DS38.2
AL13	GPIO_LED_1	LVCMOS12	DS37.2
AK13	GPIO_LED_2	LVCMOS12	DS39.2
AP8	GPIO_LED_3	LVCMOS12	DS40.2
AM8	GPIO_LED_4	LVCMOS12	DS41.2
AM9	GPIO_LED_5	LVCMOS12	DS42.2
AM10	GPIO_LED_6	LVCMOS12	DS43.2
AM11	GPIO_LED_7	LVCMOS12	DS44.2
Directional Pushbuttons (Active High)			
AG13	GPIO_SW_N	LVCMOS12	SW18.3
AC14	GPIO_SW_E	LVCMOS12	SW17.3
AK12	GPIO_SW_W	LVCMOS12	SW14.3
AP20	GPIO_SW_S	LVCMOS12	SW16.3
AL10	GPIO_SW_C	LVCMOS12	SW15.3
CPU Reset Pushbutton (Active High)			
G13	CPU_RESET	LVCMOS18	SW20.3
GPIO DIP SW (Active High)			
A17	GPIO_DIP_SW0	LVCMOS18	SW13.8
A16	GPIO_DIP_SW1	LVCMOS18	SW13.7

Table 3-35: **XCZU7EV U1 to GPIO Connections *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	I/O Standard	Device
B16	GPIO_DIP_SW2	LVCMOS18	SW13.6
B15	GPIO_DIP_SW3	LVCMOS18	SW13.5
A15	GPIO_DIP_SW4	LVCMOS18	SW13.4
A14	GPIO_DIP_SW5	LVCMOS18	SW13.3
B14	GPIO_DIP_SW6	LVCMOS18	SW13.2
B13	GPIO_DIP_SW7	LVCMOS18	SW13.1

Notes:
1. LEDs are driven through U106 level-shifter (1.2V-to-3.3V).

Power and Status LEDs

[Figure 2-1, area of callout 22]

Table 3-36 defines the power and status LEDs. For user controlled LEDs, see User I/O, page 86.

Table 3-36: **Power and Status LEDs**

Ref. Des.	Net Name	LED Color	Description
DS1	FPGA_INIT_B	Green/Red	Green: FPGA initialization was successful Red: FPGA initialization is in progress
DS2	VCC12_SW	Green	12 VDC power on
DS3	VCCAUX_PGOOD	Green	VCCAUX 1.8 VDC power on
DS4	VCC3V3_PGOOD	Green	VCC3V3 3.3 VDC power on
DS5	VCCINT_PGOOD	Green	VCCINT 0.85 VDC power on
DS6	VADJ_FMC_PGOOD	Green	VADJ_FMC 1.8 VDC (nominal) power on
DS7	VCC1V2_PGOOD	Green	VCC1V2 1.2 VDC power on
DS8	VCCBRAM_PGOOD	Green	VCCBRAM 0.85 VDC power on
DS9	MGTAVTT_PGOOD	Green	MGTAVTT 1.2 VDC power on
DS10	MGTAVCC_PGOOD	Green	MGTAVCC 0.9 VDC power on
DS11	VCCPSINTFP_PGOOD	Green	VCCPSINTFP 0.85 VDC power on
DS12	MGTRAVCC_PGOOD	Green	MGTRAVCC 0.85 VDC power on
DS13	MGTVCCAUX_PGOOD	Green	MGTVCCAUX 1.81 VDC power on
DS14	VCCPSAUX_PGOOD	Green	VCCPSAUX 1.81 VDC power on
DS15	VCCPSPLL_PGOOD	Green	VCCPSPLL 1.2 VDC power on
DS16	VCCPSINTLP_PGOOD	Green	VCCPSINTLP 0.85 VDC power on
DS17	DDR4_DIMM_VDDQ_PGOOD	Green	DDR4_DIMM_VDDQ 1.2 VDC power on
DS18	MGTRAVTT_PGOOD	Green	MGTRAVTT 1.81 VDC power on

Table 3-36: **Power and Status LEDs *(Cont'd)***

Ref. Des.	Net Name	LED Color	Description
DS19	PS_DDR4_VPP_2V5	Green	PS_DDR4_VPP_2V5 2.5 VDC power on
DS20	PL_DDR4_VPP_2V6	Green	PL_DDR4_VPP_2V5 2.5 VDC power on
DS21	VCCOPS_PGOOD	Green	VCCOPS 1.80 VDC power on
DS22	UTIL_5V0_PGOOD	Green	UTIL_5V0 5 VDC power on
DS24	VCCPSDDRPLL_PGOOD	Green	VCCPSDDRPLL 1.81 VDC power on
DS25	UTIL_3V3_PGOOD	Green	UTIL_3V3 3.3 VDC power on
DS26	VCCOPS3_PGOOD	Green	VCCOPS3 1.81 VDC power on
DS27	ENET_LED_1	Green	EHPY U98 1000BASE-T link is established
DS29	UTIL_1V8	Green	UTIL_1V8 1.8VDC power on
DS30	PL_DDR4_VTERM_0V60_PGOOD	Green	PL_DDR4_VTERM 0.6VDC power on
DS31	PS_DDR4_VTERM_0V60_PGOOD	Green	PS_DDR4_VTERM 0.6VDC power on
DS32	DONE	Green	MPSoC U1 bit file download is complete.
DS33	PS_ERR_STATUS(1)	Green	PS error status indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status.
DS34	DP_VCC3V3	Green	Display port 3.3VDC power on
DS35	PS_ERR_OUT(1)	Red	PS error out is asserted for accidental loss of power, an error in the PMU that holds the CSU in reset, or an exception in the PMU.
DS36	POR_RST_B	Red	POR U22 asserts RST_B low when any of the monitored voltages (IN_) falls below its respective threshold, any EN_ goes low, or MR is asserted.
DS37-DS44	GPIO_LED_1, GPIO_LED_[0,2:7]	Green	USER GPIO LEDs
DS46	MSP430_LED1	Green	MSP430 U41 GPIO LED
DS47	MSP430_LED0	Green	MSP430 U41 GPIO LED
DS49	UTIL_1V13_PG	Green	UTIL_1V13 1.13VDC power on
DS50	MIO23_LED	Green	MPSoC U1 Bank 500 GPIO LED
DS51	USB3 MIC2544 U121 FLG	Green	PS USB 3.0 ULPI VBUS power error

Notes:

1. See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] for more information about Zynq UltraScale+ MPSoC configuration pins.

Figure 3-37 shows the power and status LEDs area of the board.

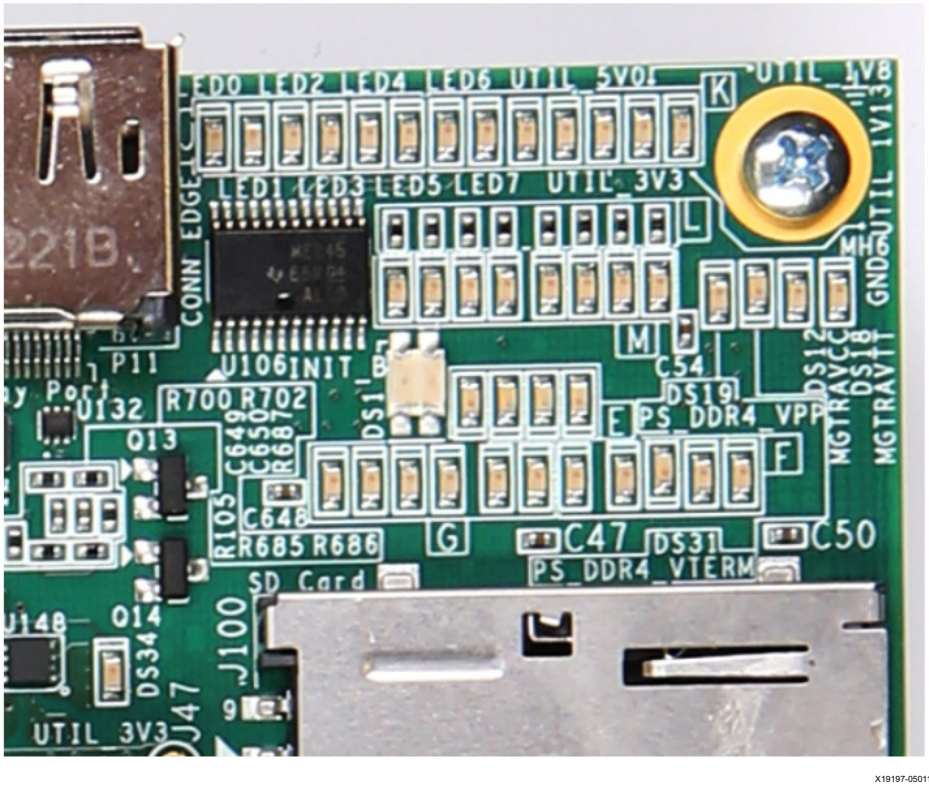


Figure 3-37: **Power and Status LEDs**

GTH Transceivers

[Figure 2-1, callout 1]

The Zynq UltraScale+ XCZU7EV MPSoC has 20 GTH gigabit transceivers (16.3 Gb/s capable) on the PL-side.

The GTH transceivers in the XCZU7EV device are grouped into four channels referred to as Quads. The reference clock for a Quad can be sourced from the Quad above or the Quad below the GTH Quad of interest. There are five GTH Quads on the ZCU106 board with connectivity as listed here:

Quad 223:

- MGTREFCLK0 - HDMI_SI5324_OUT_C_P/N
- MGTREFCLK1 - HDMI_RX_CLK_C_P/N
- Contains three GTH transceivers allocated to HDMI_TX/RX[2:0]_P/N
- Contains one GTH transceiver allocated to FMC_HPC1_DP0_C2M/M2C_P/N

Quad 224:

- MGTREFCLK0 - PCIE_CLK_P/N
- MGTREFCLK1 - USER_SMA_MGT_CLOCK_C_P/N
- Contains four GTH transceivers allocated to PCIE_TX/RX[0:3]_P/N

Quad 225:

- MGTREFCLK0 - FMC_HPC1_GBTCLK0_M2C_C_P/N
- MGTREFCLK1 - SFP_SI5328_OUT_C_P/N
- Contains one GTH transceiver allocated to SDI_MGT_TX/RX_P/N
- Contains one GTH transceiver allocated to SMA_MGT TX/RX_P/N
- Contains two GTH transceivers allocated to SFP[0:1]_TX/RX_P/N

Quad 226:

- MGTREFCLK0 - FMC_HPC0_GBTCLK0_M2C_C_P/N
- MGTREFCLK1 - USER_MGT_SI570_CLOCK1_C_P/N
- Contains four GTH transceivers allocated to FMC_HPC0_DP[0:3]_C2M/M2C_P/N

Quad 227:

- MGTREFCLK0 - FMC_HPC0_GBTCLK1_M2C_C_P/N
- MGTREFCLK1 - USER_MGT_SI570_CLOCK2_C_P/N
- Contains four GTH transceivers allocated to FMC_HPC0_DP[4:7]_C2M/M2C_P/N

GTH transceiver interface assignments on the ZCU106 are shown in Figure 3-38.

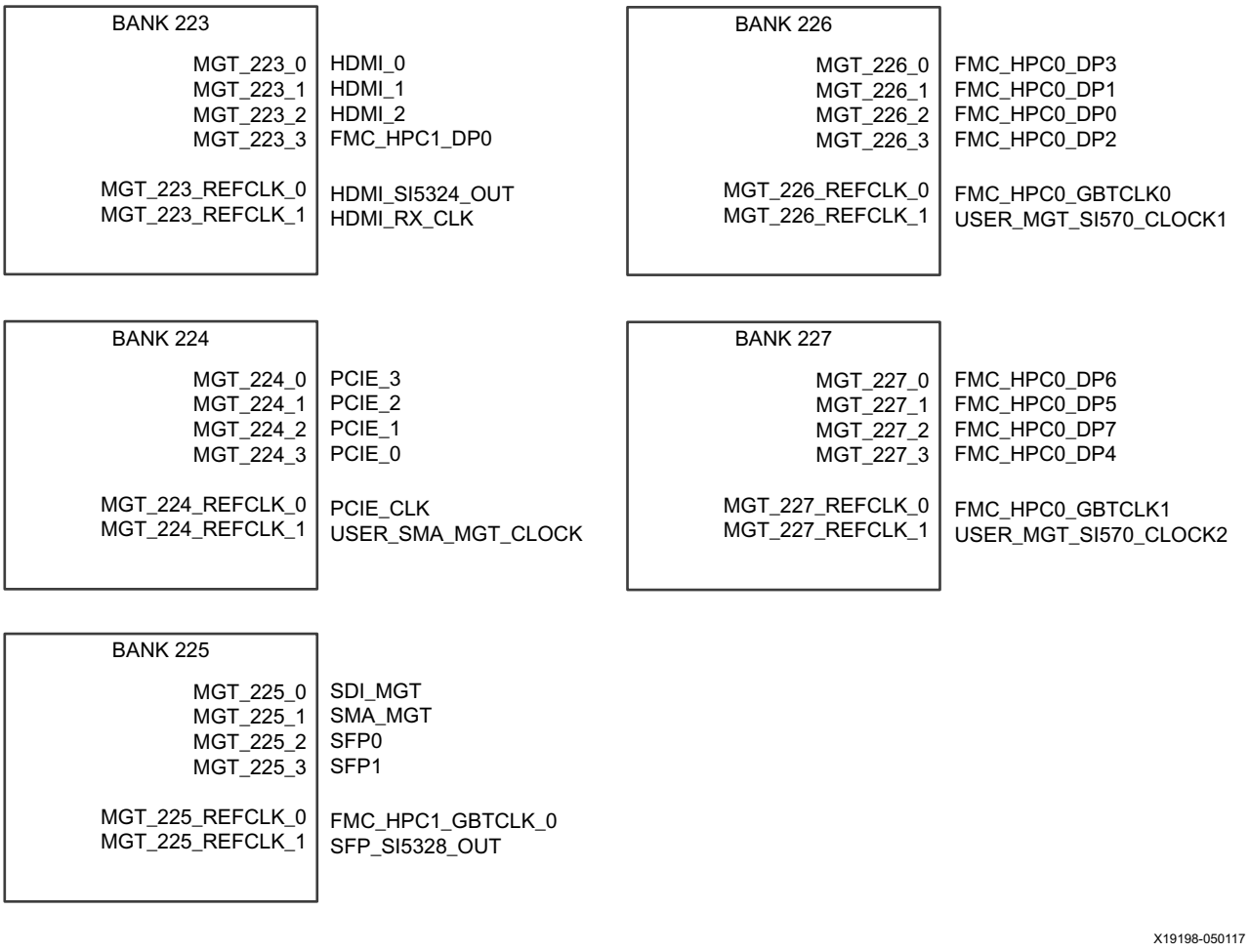


Figure 3-38: **GTH Transceiver Bank Assignments**

FMC HPC_0

Eight MGTs in a common FPGA column are provided by PL-side MGT banks 226 and 227. Available MGT reference clocks include the FMC defined GBT clocks 0 and 1 for HPC0, and a programmable Si570 buffered 1-to-2 clock. Additional MGT reference clocks are located in adjacent MGT banks.

FMC HPC_1

One MGT is provided by PL-side MGT bank 223. Available MGT reference clocks include the two HDMI associated clocks HDMI_RX_CLK and HDMI_SI5324_OUT. Additional MGT reference clocks are located in adjacent MGT banks.

SFP+

Two PL-side GTH transceivers in bank 228 are provided for the Quad SFP+ interface. Available GTH transceiver reference clocks include the FMC defined GBT clock 0 for HPC1 and a jitter attenuated recovered clock from a Si5328. SFP+ modules typically provide an I2C based control interface. This I2C interface is accessible for each individual SFP+ module through the I2C multiplexer topology on the ZCU106.

HDMI

Three PL-side GTH transceivers are dedicated for HDMI source and sink. Modes supported are 4K, 2K at 60 f/s, and 2160p60. External circuitry for interfacing TMDS signals with the GTH transceivers is required.

SMA

One MGT in bank 225 is provided on TX and RX SMA connector pairs. Available MGT clocks include the FMC defined GBT clock 0 for HPC1 and a jitter attenuated recovered clock from a Si5328. Table 3-37 through Table 3-41 list the five GTH transceiver bank (223-227) connections.

Table 3-37: **GTH Transceiver Bank 223 Interface Connections**

XCZU7EV (U1) Pin	XCZU7EV Pin Name	Schematic Net Name(2)	Connected To		
			Pin No.	Pin Name	Device
AN6	MGTHTXP0	HDMI_TX0_P	8	IN_D0P	SN65DP159RGZ HDMI re-timer U94
AN5	MGTHTXN0	HDMI_TX0_N	9	IN_D0N	
AM4	MGTHTXP1	HDMI_TX1_P	5	IN_D1P	
AM3	MGTHTXN1	HDMI_TX1_N	6	IN_D1N	
AL6	MGTHTXP2	HDMI_TX2_P	2	IN_D2P	
AL5	MGTHTXN2	HDMI_TX2_N	3	IN_D2N	
AP4	MGTHRXP0	HDMI_RX0_C_P(1)	B7	TMDS_DATA0_P	P7 MOLEX HDMI bottom port
AP3	MGTHRXN0	HDMI_RX0_C_N(1)	B9	TMDS_DATA0_N	
AN2	MGTHRXP1	HDMI_RX1_C_P(1)	B4	TMDS_DATA1_P	
AN1	MGTHRXN1	HDMI_RX1_C_N(1)	B6	TMDS_DATA1_N	
AL2	MGTHRXP2	HDMI_RX2_C_P(1)	B1	TMDS_DATA2_P	
AL1	MGTHRXN2	HDMI_RX2_C_N(1)	B3	TMDS_DATA2_N	
AC10	MGTREFCLK1P	HDMI_RX_CLK_C_P(1)	B10	TMDS_CLK_P	
AC9	MGTREFCLK1N	HDMI_RX_CLK_C_N(1)	B12	TMDS_CLK_N	
AJ6	MGTHTXP3	FMC_HPC1_DP0_C2M_P	C2	DP0_C2M_P	FMC HPC1 J4
AJ5	MGTHTXN3	FMC_HPC1_DP0_C2M_N	C3	DP0_C2M_N	
AK4	MGTHRXP3	FMC_HPC1_DP0_M2C_P	C6	DP0_M2C_P	
AK3	MGTHRXN3	FMC_HPC1_DP0_M2C_N	C7	DP0_M2C_N	
AD8	MGTREFCLK0P	HDMI_SI5324_OUT_C_P(1)	28	CKOUT1_P	SI5319C JITTER ATTEN. U108
AD7	MGTREFCLK0N	HDMI_SI5324_OUT_C_N(1)	29	CKOUT1_N	

Notes:

1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.

Table 3-38: **GTH Transceiver Bank 224 Interface Connections**

XCZU7EV (U1) Pin	XCZU7EV Pin Name	Schematic Net Name[2]	Connected To		
			Pin No.	Pin Name	Device
AH4	MGTHTXP0	PCIE_TX3_P[1]	A29	PERp3	PCIe 4-lane edge connector P3
AH3	MGTHTXN0	PCIE_TX3_N[1]	A30	PERn3	
AJ2	MGTHTXP1	PCIE_RX3_P	B27	PETp3	
AJ1	MGTHTXN1	PCIE_RX3_N	B28	PETn3	
AG6	MGTHTXP2	PCIE_TX2_P[1]	A25	PERp2	
AG5	MGTHTXN2	PCIE_TX2_N[1]	A26	PERn2	
AG2	MGTHRXP0	PCIE_RX2_P	B23	PETp2	
AG1	MGTHRXN0	PCIE_RX2_N	B24	PETn2	
AE6	MGTHRXP1	PCIE_TX1_P[1]	A21	PERp1	
AE5	MGTHRXN1	PCIE_TX1_N[1]	A22	PERn1	
AF4	MGTHRXP2	PCIE_RX1_P	B19	PETp1	
AF3	MGTHRXN2	PCIE_RX1_N	B20	PETn1	
AD4	MGTHTXP3	PCIE_TX0_P[1]	A16	PERp0	
AD3	MGTHTXN3	PCIE_TX0_N[1]	A17	PERn0	
AE2	MGTHRXP3	PCIE_RX0_P	B14	PETp0	
AE1	MGTHRXN3	PCIE_RX0_N	B15	PETn0	
AB8	MGTREFCLK0P	PCIE_CLK_P[1]	A13	REFCLK+	
AB7	MGTREFCLK0N	PCIE_CLK_N[1]	A14	REFCLK-	
AA10	MGTREFCLK1P	USER_SMA_MGT_CLOCK_C_P	1	SIG	SMA J79
AA9	MGTREFCLK1N	USER_SMA_MGT_CLOCK_C_N	1	SIG	SMA J80

Notes:

1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.

Table 3-39: **GTH Transceiver Bank 225 Interface Connections**

XCZU7EV (U1) Pin	XCZU7EV Pin Name	Schematic Net Name[2]	Connected To		
			Pin No.	Pin Name	Device
AC6	MGTHTXP0	SDI_MGT_TX_P[1]	3	SDI_P	M23145G_14PG re-clocker
AC5	MGTHTXN0	SDI_MGT_TX_N[1]	4	SDI_N	
AC2	MGTHRXP0	SDI_MGT_RX_P[1]	20	SDO0_P	M23554G_14PG re-clocker
AC1	MGTHRXN0	SDI_MGT_RX_N[1]	19	SDO0_N	
AA6	MGTHTXP1	SMA_MGT_TX_P	1	SIG	MGT SMA J72
AA5	MGTHTXN1	SMA_MGT_TX_N	1	SIG	MGT SMA J42
AB4	MGTHRXP1	SMA_MGT_RX_C_P[1]	1	SIG	MGT SMA J74
AB3	MGTHRXN1	SMA_MGT_RX_C_N[1]	1	SIG	MGT SMA J73
Y4	MGTHTXP2	SFP0_TX_P	18	TD_P	SFP0 connector P1
Y3	MGTHTXN2	SFP0_TX_N	19	TD_N	
AA2	MGTHRXP2	SFP0_RX_P	13	RD_P	
AA1	MGTHRXN2	SFP0_RX_N	12	RD_N	
W6	MGTHTXP3	SFP1_TX_P	18	TD_P	SFP0 connector P2
W5	MGTHTXN3	SFP1_TX_N	19	TD_N	
W2	MGTHRXP3	SFP1_RX_P	13	RD_P	
W1	MGTHRXN3	SFP1_RX_N	12	RD_N	
Y8	MGTREFCLK0P	FMC_HPC1_GBTCLK0_M2C_C_P[1]	D4	GBTCLK0_M2C_P	FMC HPC1 J4
Y7	MGTREFCLK0N	FMC_HPC1_GBTCLK0_M2C_C_N[1]	D5	GBTCLK0_M2C_N	
W10	MGTREFCLK1P	SFP_SI5328_OUT_C_P[1]	28	CKOUT1_P	SI5328B U20
W9	MGTREFCLK1N	SFP_SI5328_OUT_C_N[1]	29	CKOUT1_N	

Notes:

1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.

Table 3-40: **GTH Transceiver Bank 226 Interface Connections**

XCZU7EV (U1) Pin	XCZU7EV Pin Name	Schematic Net Name[2]	Connected To		
			Pin No.	Pin Name	Device
U6	MGTHTXP0	FMC_HPC0_DP3_C2M_P	A30	DP3_C2M_P	FMC HPC0 J5
U5	MGTHTXN0	FMC_HPC0_DP3_C2M_N	A31	DP3_C2M_N	
V4	MGTHRXP0	FMC_HPC0_DP3_M2C_P	A10	DP3_M2C_P	
V3	MGTHRXN0	FMC_HPC0_DP3_M2C_N	A11	DP3_M2C_N	
T4	MGTHTXP1	FMC_HPC0_DP1_C2M_P	A22	DP1_C2M_P	
T3	MGTHTXN1	FMC_HPC0_DP1_C2M_N	A23	DP1_C2M_N	
U2	MGTHRXP1	FMC_HPC0_DP1_M2C_P	A2	DP1_M2C_P	
U1	MGTHRXN1	FMC_HPC0_DP1_M2C_N	A3	DP1_M2C_N	
R6	MGTHTXP2	FMC_HPC0_DP0_C2M_P	C2	DP0_C2M_P	
R5	MGTHTXN2	FMC_HPC0_DP0_C2M_N	C3	DP0_C2M_N	
R2	MGTHRXP2	FMC_HPC0_DP0_M2C_P	C6	DP0_M2C_P	
R1	MGTHRXN2	FMC_HPC0_DP0_M2C_N	C7	DP0_M2C_N	
N6	MGTHTXP3	FMC_HPC0_DP2_C2M_P	A26	DP2_C2M_P	
N5	MGTHTXN3	FMC_HPC0_DP2_C2M_N	A27	DP2_C2M_N	
P4	MGTHRXP3	FMC_HPC0_DP2_M2C_P	A6	DP2_M2C_P	
P3	MGTHRXN3	FMC_HPC0_DP2_M2C_N	A7	DP2_M2C_N	
V8	MGTREFCLK0P	FMC_HPC0_GBTCLK0_M2C_C_P[1]	D4	GBTCLK0_M2C_P	
V7	MGTREFCLK0N	FMC_HPC0_GBTCLK0_M2C_C_N[1]	D5	GBTCLK0_M2C_N	
U10	MGTREFCLK1P	USER_MGT_SI570_CLOCK1_C_P[1]	11	Q1_P	SI53340 U51 1-to-2 buffer
U9	MGTREFCLK1N	USER_MGT_SI570_CLOCK1_C_N[1]	12	Q1_N	

Notes:

1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.

Table 3-41: **GTH Transceiver Bank 227 Interface Connections**

XCZU7EV (U1) Pin	XCZU7EV Pin Name	Schematic Net Name[2]	Connected To		
			Pin No.	Pin Name	Device
M4	MGTHTXP0	FMC_HPC0_DP6_C2M_P	B36	DP6_C2M_P	FMC HPC0 J5
M3	MGTHTXN0	FMC_HPC0_DP6_C2M_N	B37	DP6_C2M_N	
N2	MGTHRXP0	FMC_HPC0_DP6_M2C_P	B16	DP6_M2C_P	
N1	MGTHRXN0	FMC_HPC0_DP6_M2C_N	B17	DP6_M2C_N	
L6	MGTHTXP1	FMC_HPC0_DP5_C2M_P	A38	DP5_C2M_P	
L5	MGTHTXN1	FMC_HPC0_DP5_C2M_N	A39	DP5_C2M_N	
L2	MGTHRXP1	FMC_HPC0_DP5_M2C_P	A18	DP5_M2C_P	
L1	MGTHRXN1	FMC_HPC0_DP5_M2C_N	A19	DP5_M2C_N	
K4	MGTHTXP2	FMC_HPC0_DP7_C2M_P	B32	DP7_C2M_P	
K3	MGTHTXN2	FMC_HPC0_DP7_C2M_N	B33	DP7_C2M_N	
J2	MGTHRXP2	FMC_HPC0_DP7_M2C_P	B12	DP7_M2C_P	
J1	MGTHRXN2	FMC_HPC0_DP7_M2C_N	B13	DP7_M2C_N	
H4	MGTHTXP3	FMC_HPC0_DP4_C2M_P	A34	DP4_C2M_P	
H3	MGTHTXN3	FMC_HPC0_DP4_C2M_N	A35	DP4_C2M_N	
G2	MGTHRXP3	FMC_HPC0_DP4_M2C_P	A14	DP4_M2C_P	
G1	MGTHRXN3	FMC_HPC0_DP4_M2C_N	A15	DP4_M2C_N	
T8	MGTREFCLK0P	FMC_HPC0_GBTCLK1_M2C_C_P[1]	B20	GBTCLK1_M2C_P	
T7	MGTREFCLK0N	FMC_HPC0_GBTCLK1_M2C_C_N[1]	B21	GBTCLK1_M2C_N	
R10	MGTREFCLK1P	USER_MGT_SI570_CLOCK2_C_P[1]	13	Q2_P	SI53340U51 1-to-2 buffer
R9	MGTREFCLK1N	USER_MGT_SI570_CLOCK2_C_N[1]	14	Q2_N	

Notes:

1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.

PCI Express Endpoint Connectivity

[Figure 2-1, callout 36]

The 4-lane PCI Express edge connector P3 performs data transfers at the rate of 2.5 GT/s for Gen1 applications, 5.0 GT/s for Gen2 applications, and 8.0 GT/s for Gen3 applications. The PCIe transmit and receive signal data paths have a characteristic impedance of 85Ω ±10%. The PCIe clock is routed as a 100Ω differential pair. The XCZU7EV (-2 speed grade) supports up to Gen3 x8.

The PCIe reference clock input is from the P3 edge connector. It is AC coupled to MPSoC U1 through the MGTREFCLK0 pins of Quad 224. PCIE_CLK_P is connected to U1 pin AB8, and the _N net is connected to pin AB7. The PCI Express clock connection is shown in Figure 3-39 and the PCI Express connector is shown in Figure 3-40.

PCIe lane size is selected by jumper J162 as shown in Figure 3-40. The default lane size selection is 4-lane (J162 pins 2 and 4 jumped).

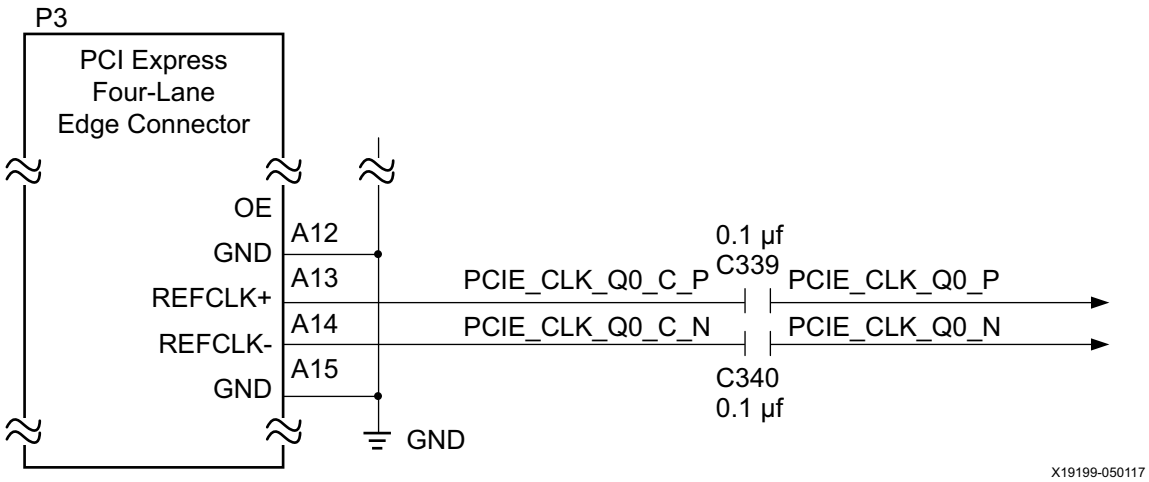


Figure 3-39: **PCIe Edge Connector Clock**

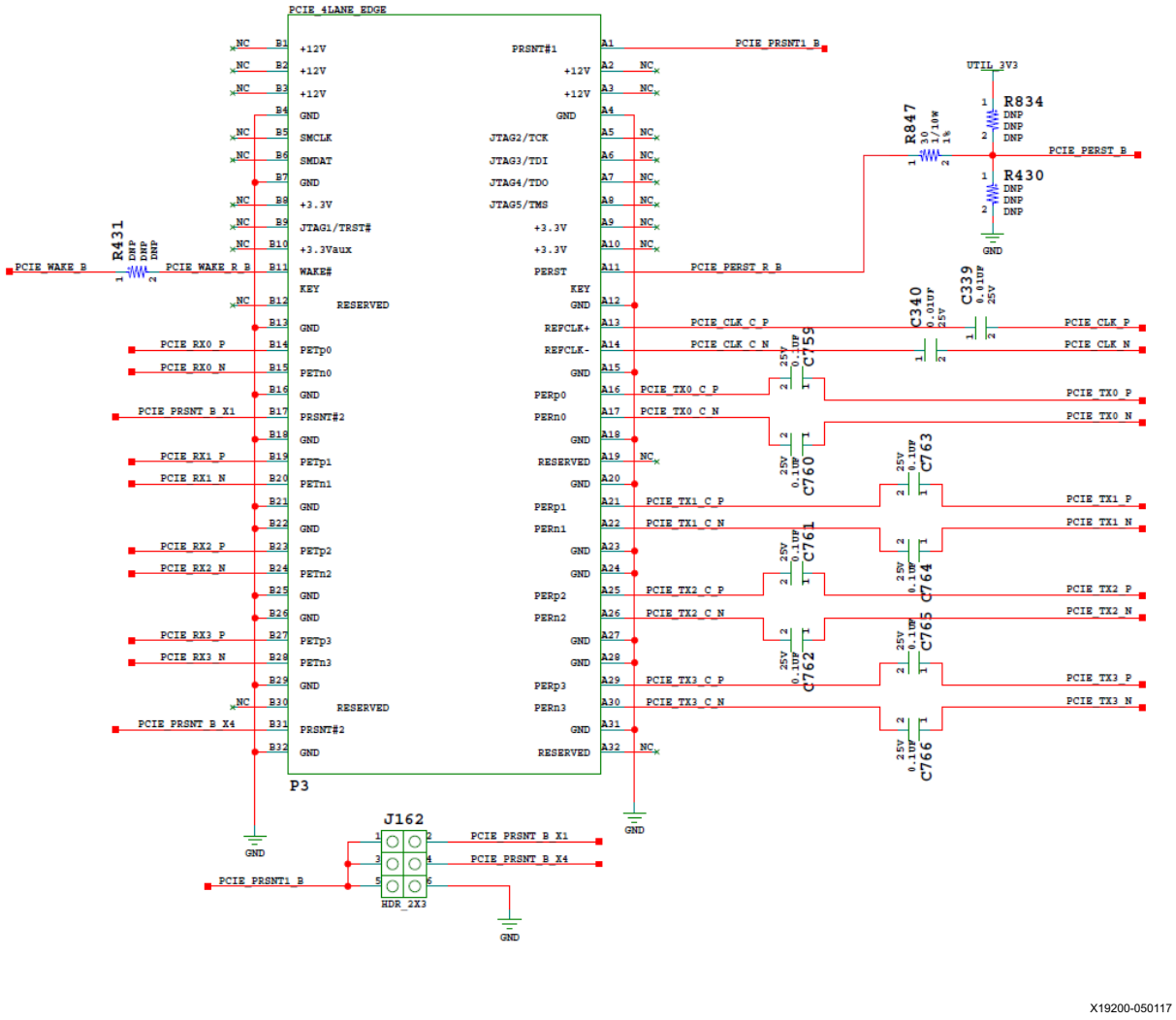


Figure 3-40: **PCI Express Connector P3 and Lane Size Select Jumper J162**

See Table 3-38 for the PCIe P3 edge connector wiring to MPSoC U1.

PS GTR Transceivers

[Figure 2-1, callout 1]

The PS GTR transceiver bank 505 supports two DisplayPort transmit channels, USB (3.0) and SATA, as shown in Figure 3-41.

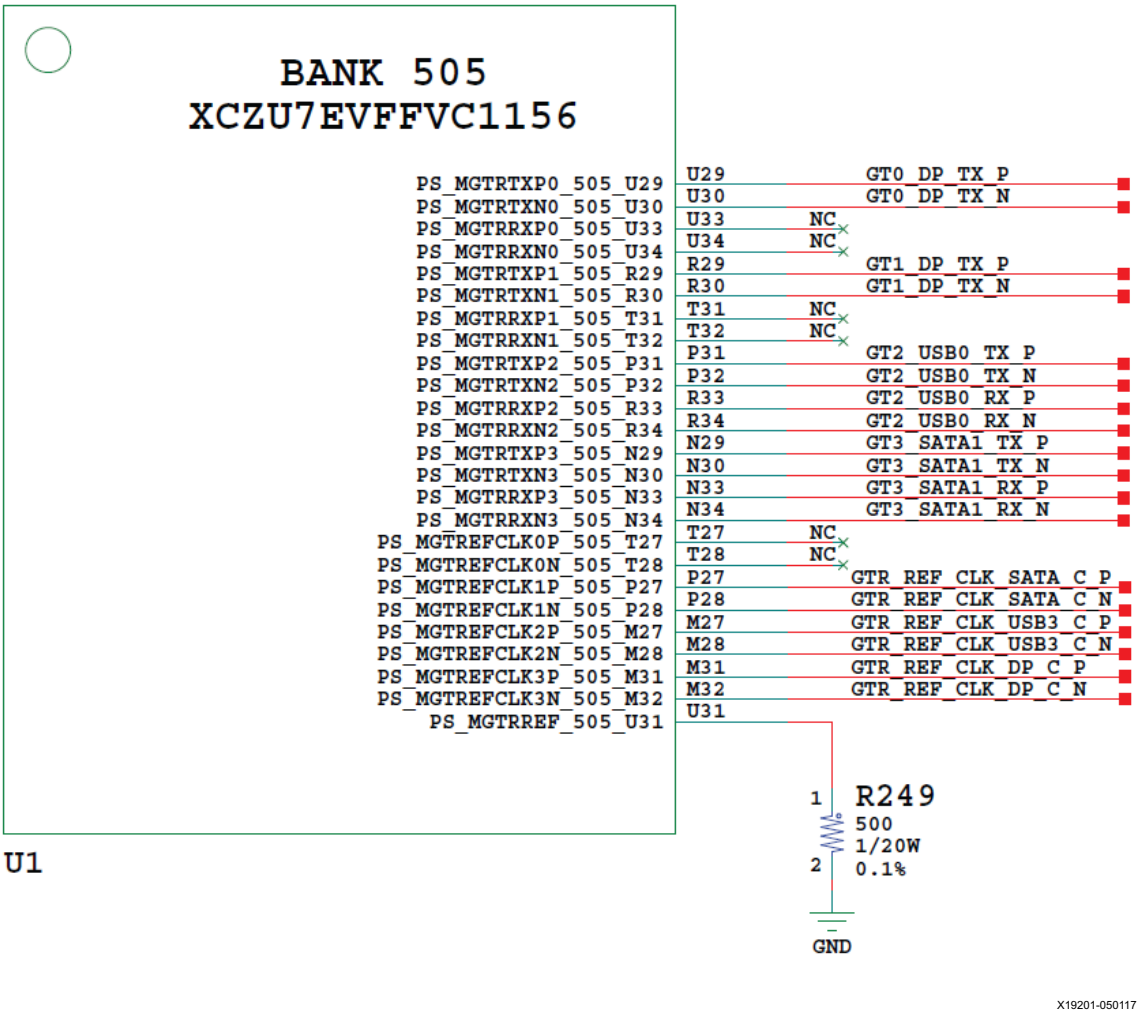


Figure 3-41: **PS-GTR Lane Assignments**

Bank 505 DP (DisplayPort) lanes 0 and 1 TX support the 2-channel source only PS-side DisplayPort circuitry described in DisplayPort DPAUX (MIO 27-30), page 69.

Bank 505 USB0 lane 2 supports the USB3.0 interface described in USB 3.0 Transceiver and USB 2.0 ULPI PHY, page 40.

Bank 505 SATA1 lane 3 supports SATA connector P9 as shown in Figure 3-42.

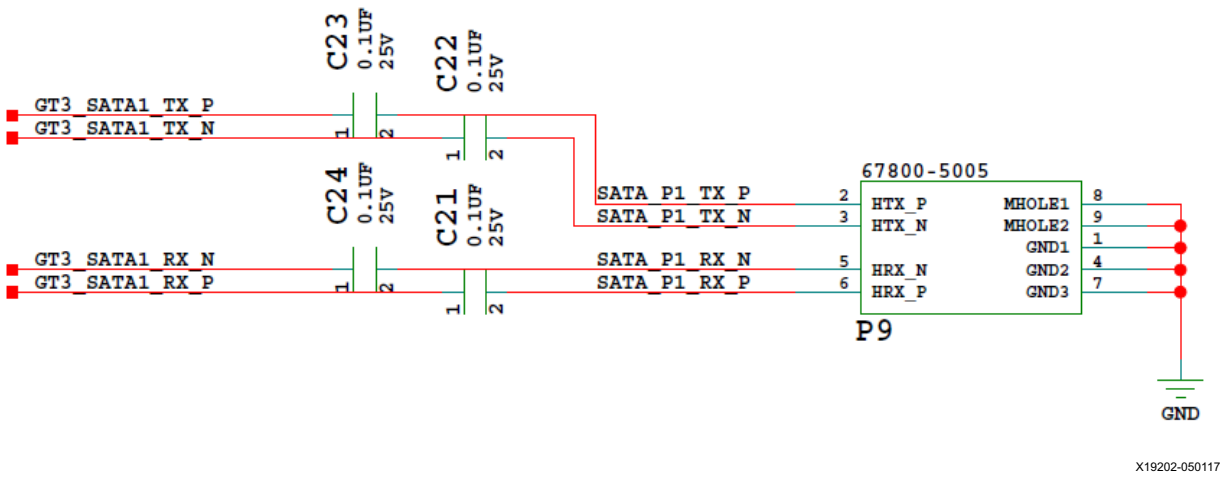


Figure 3-42: **PS-GTR SATA**

Bank 505 reference clocks are connected to the U69 SI5341B clock generator as described in SI5341B 10 Independent Output Any-Frequency Clock Generator, page 50. Bank 505 connections are shown in Table 3-42.

Table 3-42: **PS-GTR Bank 505 Interface Connections**

XCZU7EV (U1) Pin	XCZU7EV Pin Name	Schematic Net Name(2)	Connected To		
			Pin No.	Pin Name	Device
U29	PS_MGTRTXP0	GT0_DP_TX_P(1)	4	ML_LANE1_P	DisplayPort connector P11
U30	PS_MGTRTXN0	GT0_DP_TX_N(1)	6	ML_LANE1_N	
R29	PS_MGTRTXP1	GT1_DP_TX_P(1)	1	ML_LANE0_P	
R30	PS_MGTRTXN1	GT1_DP_TX_N(1)	3	ML_LANE0_N	
U33	PS_MGTRRXP0	NC	NA	NA	NA
U34	PS_MGTRRXN0	NC	NA	NA	
T31	PS_MGTRRXP1	NC	NA	NA	
T32	PS_MGTRRXN1	NC	NA	NA	
P31	PS_MGTRTXP2	GT2_USB0_TX_P(1)	9	SSTXP	USB J96
P32	PS_MGTRTXN2	GT2_USB0_TX_N(1)	8	SSTXN	
R33	PS_MGTRRXP2	GT2_USB0_RX_P	6	SSRXP	
R34	PS_MGTRRXN2	GT2_USB0_RX_N	5	SSRXN	

Table 3-42: **PS-GTR Bank 505 Interface Connections *(Cont'd)***

XCZU7EV (U1) Pin	XCZU7EV Pin Name	Schematic Net Name[2]	Connected To		
			Pin No.	Pin Name	Device
N29	PS_MGTRTXP3	GT3_SATA1_TX_P[1]	2	HTX_P	SATA P9
N30	PS_MGTRTXN3	GT3_SATA1_TX_N[1]	3	HTX_N	
N33	PS_MGTRRXP3	GT3_SATA1_RX_P[1]	6	HRX_P	
N34	PS_MGTRRXN3	GT3_SATA1_RX_N[1]	5	HRX_N	
T27	PS_MGTREFCLK0P	NC	NA	NA	NA
T28	PS_MGTREFCLK0N	NC	NA	NA	
P27	PS_MGTREFCLK1P	GTR_REF_CLK_SATA_C_P[1]	35	OUT3_P	SI5341B U69
P28	PS_MGTREFCLK1N	GTR_REF_CLK_SATA_C_N[1]	34	OUT3_N	
M27	PS_MGTREFCLK2P	GTR_REF_CLK_USB3_C_P[1]	31	OUT2_P	
M28	PS_MGTREFCLK2N	GTR_REF_CLK_USB3_C_N[1]	30	OUT2_N	
M31	PS_MGTREFCLK3P	GTR_REF_CLK_DP_C_P[1]	24	OUT0_P	
M32	PS_MGTREFCLK3N	GTR_REF_CLK_DP_C_N[1]	23	OUT0_N	

Notes:

1. Series capacitor coupled.
2. MGT connections I/O standard not applicable.

FPGA Mezzanine Card Interface

[Figure 2-1, callouts 32, 33]

The ZCU106 evaluation board supports the VITA 57.1 FPGA mezzanine card (FMC) specification [Ref 23] by providing subset implementations of high pin count connectors at J5 (HPC0) and J4 (HPC1). HPC connectors use a 10 x 40 form factor, populated with 400 pins. The connectors are keyed so that a mezzanine card, when installed in either of these FMC connectors on the ZCU106 evaluation board, faces away from the board.

FMC HPC0 Connector J5

[Figure 2-1, callout 32]

The FMC connector at J5 (HPC0) implements a subset of the full FMC HPC connectivity:

- 68 single-ended, or 34 differential user-defined pairs (34 LA pairs: LA[00:33])
- Eight GTH transceiver DP differential pairs
- Two GBTCLK differential clocks
- 159 ground and 15 power connections

The ZCU106 board FMC VADJ voltage VADJ_FMC_BUS for the J5 (HPC0) and J4 (HPC1) FMC connectors is determined by the MAX15301 U63 voltage regulator described in Board Power System, page 122. The valid values of the VADJ_FMC rail are 1.2V, 1.5V, and 1.8V. The HPC0 J5 connections to XCZU7EV U1 are shown in Table 3-43 through Table 3-46.

Table 3-43: **J5 HPC0 FMC Section A and B Connections to XCZU7EV U1**

J5 Pin	Schematic Net Name	I/O Standard	U1 Pin	J5 Pin	Schematic Net Name	I/O Standard	U1 Pin
A2	FMC_HPC0_DP1_M2C_P	(7)	U2	B1	NC		
A3	FMC_HPC0_DP1_M2C_N	(7)	U1	B4	NC		
A6	FMC_HPC0_DP2_M2C_P	(7)	P4	B5	NC		
A7	FMC_HPC0_DP2_M2C_N	(7)	P3	B8	NC		
A10	FMC_HPC0_DP3_M2C_P	(7)	V4	B9	NC		
A11	FMC_HPC0_DP3_M2C_N	(7)	V3	B12	FMC_HPC0_DP7_M2C_P	(7)	J2
A14	FMC_HPC0_DP4_M2C_P	(7)	G2	B13	FMC_HPC0_DP7_M2C_N	(7)	J1
A15	FMC_HPC0_DP4_M2C_N	(7)	G1	B16	FMC_HPC0_DP6_M2C_P	(7)	N2
A18	FMC_HPC0_DP5_M2C_P	(7)	L2	B17	FMC_HPC0_DP6_M2C_N	(7)	N1
A19	FMC_HPC0_DP5_M2C_N	(7)	L1	B20	FMC_HPC0_GBTCLK1_M2C_P	(1)(7)	T8
A22	FMC_HPC0_DP1_C2M_P	(7)	T4	B21	FMC_HPC0_GBTCLK1_M2C_N	(1)(7)	T7
A23	FMC_HPC0_DP1_C2M_N	(7)	T3	B24	NC		
A26	FMC_HPC0_DP2_C2M_P	(7)	N6	B25	NC		
A27	FMC_HPC0_DP2_C2M_N	(7)	N5	B28	NC		
A30	FMC_HPC0_DP3_C2M_P	(7)	U6	B29	NC		
A31	FMC_HPC0_DP3_C2M_N	(7)	U5	B32	FMC_HPC0_DP7_C2M_P	(7)	K4
A34	FMC_HPC0_DP4_C2M_P	(7)	H4	B33	FMC_HPC0_DP7_C2M_N	(7)	K3
A35	FMC_HPC0_DP4_C2M_N	(7)	H3	B36	FMC_HPC0_DP6_C2M_P	(7)	M4
A38	FMC_HPC0_DP5_C2M_P	(7)	L6	B37	FMC_HPC0_DP6_C2M_N	(7)	M3
A39	FMC_HPC0_DP5_C2M_N	(7)	L5	B40	NC		

Notes:

1. Series capacitor coupled to FPGA U1 pin.
2. Connected to I2C switch U135 pins 4 and 5.
3. FPGA U1 JTAG TCK, TMS, TDO pins are buffered by U48 SN74AVC8T245.
4. J5 HPC0 TDO-TDI connections to U27 HPC0 FMC JTAG bypass switch (N.C. normally-closed/bypassing J5 until an FMC card is plugged onto J5).
5. FMC_HPC0_PRSNT_M2C_B is the HPC FMC JTAG bypass switch U27.4 OE control signal, driven by I2C I/O expander U97.13.
6. Sourced from VADJ_FMC_BUS voltage regulator U63 MAX15301 pin 32 power good output signal.
7. U1 MGT (I/O standards do not apply).

Table 3-44: **J5 HPC0 FMC Section C and D Connections to XCZU7EV U1**

J5 Pin	Schematic Net Name	I/O Standard	U1 Pin	J5 Pin	Schematic Net Name	I/O Standard	U1 Pin
C2	FMC_HPC0_DP0_C2M_P	(7)	R6	D1	VADJ_FMC_PGOOD (6)		
C3	FMC_HPC0_DP0_C2M_N	(7)	R5	D4	FMC_HPC0_GBTCLK0_M2C_P (1)	(1)(7)	V8
C6	FMC_HPC0_DP0_M2C_P	(7)	R2	D5	FMC_HPC0_GBTCLK0_M2C_N (1)	(1)(7)	V7
C7	FMC_HPC0_DP0_M2C_N	(7)	R1	D8	FMC_HPC0_LA01_CC_P	LVCMOS18	H18
C10	FMC_HPC0_LA06_P	LVCMOS18	H19	D9	FMC_HPC0_LA01_CC_N	LVCMOS18	H17
C11	FMC_HPC0_LA06_N	LVCMOS18	G19	D11	FMC_HPC0_LA05_P	LVCMOS18	K17
C14	FMC_HPC0_LA10_P	LVCMOS18	L15	D12	FMC_HPC0_LA05_N	LVCMOS18	J17
C15	FMC_HPC0_LA10_N	LVCMOS18	K15	D14	FMC_HPC0_LA09_P	LVCMOS18	H16
C18	FMC_HPC0_LA14_P	LVCMOS18	C13	D15	FMC_HPC0_LA09_N	LVCMOS18	G16
C19	FMC_HPC0_LA14_N	LVCMOS18	C12	D17	FMC_HPC0_LA13_P	LVCMOS18	G15
C22	FMC_HPC0_LA18_CC_P	LVCMOS18	D11	D18	FMC_HPC0_LA13_N	LVCMOS18	F15
C23	FMC_HPC0_LA18_CC_N	LVCMOS18	D10	D20	FMC_HPC0_LA17_CC_P	LVCMOS18	F11
C26	FMC_HPC0_LA27_P	LVCMOS18	A8	D21	FMC_HPC0_LA17_CC_N	LVCMOS18	E10
C27	FMC_HPC0_LA27_N	LVCMOS18	A7	D23	FMC_HPC0_LA23_P	LVCMOS18	B11
C30	FMC_HPC0_IIC_SCL	(2)		D24	FMC_HPC0_LA23_N	LVCMOS18	A11
C31	FMC_HPC0_IIC_SDA	(2)		D26	FMC_HPC0_LA26_P	LVCMOS18	B9
C34	GND			D27	FMC_HPC0_LA26_N	LVCMOS18	B8
C35	VCC12_SW			D29	FMC_HPC0_TCK_BUF	(3)	
C37	VCC12_SW			D30	FPGA_TDO_FMC_TDI_BUF	(4)	
C39	UTIL_3V3			D31	FMC_HPC0_TDO_HPC1_TDI	(3)(4)	
				D32	UTIL_3V3_10A		
				D33	FMC_HPC0_TMS_BUF	(3)	
				D34	NC		
				D35	GND		
				D36	UTIL_3V3		
				D38	UTIL_3V3		
				D40	UTIL_3V3		

Notes:

1. Series capacitor coupled to FPGA U1 pin.
2. Connected to I2C switch U135 pins 4 and 5.
3. FPGA U1 JTAG TCK, TMS, TDO pins are buffered by U48 SN74AVC8T245.
4. J5 HPC0 TDO-TDI connections to U27 HPC0 FMC JTAG bypass switch (N.C. normally-closed/bypassing J5 until an FMC card is plugged onto J5).
5. FMC_HPC0_PRSNT_M2C_B is the HPC FMC JTAG bypass switch U27.4 OE control signal, driven by I2C I/O expander U97.13.
6. Sourced from VADJ_FMC_BUS voltage regulator U63 MAX15301 pin 32 power good output signal.
7. U1 MGT (I/O standards do not apply).

Table 3-45: **J5 HPC0 FMC Section E and F Connections to XCZU7EV U1**

J5 Pin	Schematic Net Name	I/O Standard	U1 Pin		J5 Pin	Schematic Net Name	I/O Standard	U1 Pin
E2	NC				F1	FMC_HPC0_PG_M2C	P/U to 3.3V via R277	
E3	NC				F4	NC		
E6	NC				F5	NC		
E7	NC				F7	NC		
E9	NC				F8	NC		
E10	NC				F10	NC		
E12	NC				F11	NC		
E13	NC				F13	NC		
E15	NC				F14	NC		
E16	NC				F16	NC		
E18	NC				F17	NC		
E19	NC				F19	NC		
E21	NC				F20	NC		
E22	NC				F22	NC		
E24	NC				F23	NC		
E25	NC				F25	NC		
E27	NC				F26	NC		
E28	NC				F28	NC		
E30	NC				F29	NC		
E31	NC				F31	NC		
E33	NC				F32	NC		
E34	NC				F34	NC		
E36	NC				F35	NC		
E37	NC				F37	NC		
E39	VADJ_FMC_BUS				F38	NC		
					F40	VADJ_FMC_BUS		

Table 3-46: **J5 HPC0 FMC Section G and H Connections to XCZU7EV U1**

J5 Pin	Schematic Net Name	I/O Standard	U1 Pin	J5 Pin	Schematic Net Name	I/O Standard	U1 Pin
G2	FMC_HPC0_CLK1_M2C_P	LVDS	G10	H1	NC		
G3	FMC_HPC0_CLK1_M2C_N	LVDS	F10	H2	FMC_HPC0_PRSNT_M2C_B	(5)	
G6	FMC_HPC0_LA00_CC_P	LVDS	F17	H4	FMC_HPC0_CLK0_M2C_P	LVDS	E15
G7	FMC_HPC0_LA00_CC_N	LVDS	F16	H5	FMC_HPC0_CLK0_M2C_N	LVDS	E14
G9	FMC_HPC0_LA03_P	LVCMOS18	K19	H7	FMC_HPC0_LA02_P	LVCMOS18	L20
G10	FMC_HPC0_LA03_N	LVCMOS18	K18	H8	FMC_HPC0_LA02_N	LVCMOS18	K20
G12	FMC_HPC0_LA08_P	LVCMOS18	E18	H10	FMC_HPC0_LA04_P	LVCMOS18	L17
G13	FMC_HPC0_LA08_N	LVCMOS18	E17	H11	FMC_HPC0_LA04_N	LVCMOS18	L16
G15	FMC_HPC0_LA12_P	LVCMOS18	G18	H13	FMC_HPC0_LA07_P	LVCMOS18	J16
G16	FMC_HPC0_LA12_N	LVCMOS18	F18	H14	FMC_HPC0_LA07_N	LVCMOS18	J15
G18	FMC_HPC0_LA16_P	LVCMOS18	D17	H16	FMC_HPC0_LA11_P	LVCMOS18	A13
G19	FMC_HPC0_LA16_N	LVCMOS18	C17	H17	FMC_HPC0_LA11_N	LVCMOS18	A12
G21	FMC_HPC0_LA20_P	LVCMOS18	F12	H19	FMC_HPC0_LA15_P	LVCMOS18	D16
G22	FMC_HPC0_LA20_N	LVCMOS18	E12	H20	FMC_HPC0_LA15_N	LVCMOS18	C16
G24	FMC_HPC0_LA22_P	LVCMOS18	H13	H22	FMC_HPC0_LA19_P	LVCMOS18	D12
G25	FMC_HPC0_LA22_N	LVCMOS18	H12	H23	FMC_HPC0_LA19_N	LVCMOS18	C11
G27	FMC_HPC0_LA25_P	LVCMOS18	C7	H25	FMC_HPC0_LA21_P	LVCMOS18	B10
G28	FMC_HPC0_LA25_N	LVCMOS18	C6	H26	FMC_HPC0_LA21_N	LVCMOS18	A10
G30	FMC_HPC0_LA29_P	LVCMOS18	K10	H28	FMC_HPC0_LA24_P	LVCMOS18	B6
G31	FMC_HPC0_LA29_N	LVCMOS18	J10	H29	FMC_HPC0_LA24_N	LVCMOS18	A6
G33	FMC_HPC0_LA31_P	LVCMOS18	F7	H31	FMC_HPC0_LA28_P	LVCMOS18	M13
G34	FMC_HPC0_LA31_N	LVCMOS18	E7	H32	FMC_HPC0_LA28_N	LVCMOS18	L13
G36	FMC_HPC0_LA33_P	LVCMOS18	C9	H34	FMC_HPC0_LA30_P	LVCMOS18	E9
G37	FMC_HPC0_LA33_N	LVCMOS18	C8	H35	FMC_HPC0_LA30_N	LVCMOS18	D9
G39	VADJ_FMC_BUS			H37	FMC_HPC0_LA32_P	LVCMOS18	F8
				H38	FMC_HPC0_LA32_N	LVCMOS18	E8
				H40	VADJ_FMC_BUS		

Notes:

1. Series capacitor coupled to FPGA U1 pin.
2. Connected to I2C switch U135 pins 4 and 5.
3. FPGA U1 JTAG TCK, TMS, TDO pins are buffered by U48 SN74AVC8T245.
4. J5 HPC0 TDO-TDI connections to U27 HPC0 FMC JTAG bypass switch (N.C. normally-closed/bypassing J5 until an FMC card is plugged onto J5).
5. FMC_HPC0_PRSNT_M2C_B is the HPC FMC JTAG bypass switch U27.4 OE control signal, driven by I2C I/O expander U97.13.
6. Sourced from VADJ_FMC_BUS voltage regulator U63 MAX15301 pin 32 power good output signal.
7. U1 MGT (I/O standards do not apply).

Table 3-47: **J5 HPC0 FMC Section J and K Connections to XCZU7EV U1**

J5 Pin	Schematic Net Name	I/O Standard	U1 Pin	J5 Pin	Schematic Net Name	I/O Standard	U1 Pin
J2	NC			K1	NC		
J3	NC			K4	NC		
J6	NC			K5	NC		
J7	NC			K7	NC		
J9	NC			K8	NC		
J10	NC			K10	NC		
J12	NC			K11	NC		
J13	NC			K13	NC		
J15	NC			K14	NC		
J16	NC			K16	NC		
J18	NC			K17	NC		
J19	NC			K19	NC		
J21	NC			K20	NC		
J22	NC			K22	NC		
J24	NC			K23	NC		
J25	NC			K25	NC		
J27	NC			K26	NC		
J28	NC			K28	NC		
J30	NC			K29	NC		
J31	NC			K31	NC		
J33	NC			K32	NC		
J34	NC			K34	NC		
J36	NC			K35	NC		
J37	NC			K37	NC		
J39	NC			K38	NC		
				K40	NC		

FMC HPC1 Connector J4

[Figure 2-1, callout 33]

The FMC connector at J4 (HPC1) implements a subset of the full FMC HPC connectivity:

- 34 single-ended, or 17 differential user-defined pairs (LA[00:16])
- One GTH transceiver DP differential pair
- One GBTCLK differential clocks
- 159 ground and 15 power connections

The ZCU106 board FMC VADJ voltage VADJ_FMC_BUS for the J5 (HPC0) and J4 (HPC1) FMC connectors is determined by the MAX15301 U63 voltage regulator described in Board Power System, page 122. The valid values of the VADJ_FMC rail are 1.2V, 1.5V, and 1.8V. The HPC1 J4 connections to XCZU7EV U1 are shown in Table 3-48 through Table 3-52.

Table 3-48: **J4 HPC1 FMC Section A and B Connections to XCZU7EV U1**

J4 Pin	Schematic Net Name	I/O Standard	U1 Pin		J4 Pin	Schematic Net Name	I/O Standard	U1 Pin
A2	NC				B1	NC		
A3	NC				B4	NC		
A6	NC				B5	NC		
A7	NC				B8	NC		
A10	NC				B9	NC		
A11	NC				B12	NC		
A14	NC				B13	NC		
A15	NC				B16	NC		
A18	NC				B17	NC		
A19	NC				B20	NC		
A22	NC				B21	NC		
A23	NC				B24	NC		
A26	NC				B25	NC		
A27	NC				B28	NC		
A30	NC				B29	NC		
A31	NC				B32	NC		
A34	NC				B33	NC		
A35	NC				B36	NC		
A38	NC				B37	NC		
A39	NC				B40	NC		

Table 3-49: **J4 HPC1 FMC Section C and D Connections to XCZU7EV U1**

J4 Pin	Schematic Net Name	I/O Standard	U1 Pin		J4 Pin	Schematic Net Name	I/O Standard	U1 Pin
C2	FMC_HPC1_DP0_C2M_P	(7)	AJ6		D1	VADJ_FMC_PGOOD (6)		
C3	FMC_HPC1_DP0_C2M_N	(7)	AJ5		D4	FMC_HPC1_GBTCLK0_M2C_P	(1)(7)	Y8
C6	FMC_HPC1_DP0_M2C_P	(6)	AK4		D5	FMC_HPC1_GBTCLK0_M2C_N	(1)(6)	Y7
C7	FMC_HPC1_DP0_M2C_N	(7)	AK3		D8	FMC_HPC1_LA01_CC_P	LVDS	E24
C10	FMC_HPC1_LA06_P	LVDS	H21		D9	FMC_HPC1_LA01_CC_N	LVDS	D24
C11	FMC_HPC1_LA06_N	LVDS	H22		D11	FMC_HPC1_LA05_P	LVDS	G25
C14	FMC_HPC1_LA10_P	LVDS	F22		D12	FMC_HPC1_LA05_N	LVDS	G26
C15	FMC_HPC1_LA10_N	LVDS	E22		D14	FMC_HPC1_LA09_P	LVDS	G20
C18	FMC_HPC1_LA14_P	LVDS	D20		D15	FMC_HPC1_LA09_N	LVDS	F20
C19	FMC_HPC1_LA14_N	LVDS	D21		D17	FMC_HPC1_LA13_P	LVDS	C21
C22	NC				D18	FMC_HPC1_LA13_N	LVDS	C22
C23	NC				D20	NC		
C26	NC				D21	NC		
C27	NC				D23	NC		
C30	FMC_HPC1_IIC_SCL	(2)			D24	NC		
C31	FMC_HPC1_IIC_SDA	(2)			D26	NC		
C34	GND				D27	NC		
C35	VCC12_SW				D29	FMC_HPC1_TCK_BUF	(3)	
C37	VCC12_SW				D30	FPGA_TDO_FMC_TDI_BUF	(4)	
C39	UTIL_3V3				D31	FMC_HPC1_TDO_HPC1_TDI	(3)(4)	
					D32	UTIL_3V3_10A		
					D33	FMC_HPC1_TMS_BUF	(3)	
					D34	NC		
					D35	GND		
					D36	UTIL_3V3		
					D38	UTIL_3V3		
					D40	UTIL_3V3		

Notes:

1. Series capacitor coupled to FPGA U1 pin.
2. Connected to I2C switch U135 pins 6 and 7.
3. FPGA U1 JTAG TCK, TMS, and TDO pins are buffered by U48 SN74AVC8T245.
4. J4 HPC1 TDO-TDI connections to U24 HPC1 FMC JTAG bypass switch (N.C. normally-closed/bypassing J4 until an FMC card is plugged onto J4).
5. Sourced from VADJ_FMC_BUS voltage regulator U63 MAX15301 pin 32 power good output signal.
6. U1 MGT (I/O standards do not apply).

Table 3-50: **J4 HPC1 FMC Section E and F Connections to XCZU7EV U1**

J4 Pin	Schematic Net Name	I/O Standard	U1 Pin	J4 Pin	Schematic Net Name	I/O Standard	U1 Pin
E2	NC			F1	FMC_HPC1_PG_M2C	P/U to 3.3V via R250	
E3	NC			F4	NC		
E6	NC			F5	NC		
E7	NC			F7	NC		
E9	NC			F8	NC		
E10	NC			F10	NC		
E12	NC			F11	NC		
E13	NC			F13	NC		
E15	NC			F14	NC		
E16	NC			F16	NC		
E18	NC			F17	NC		
E19	NC			F19	NC		
E21	NC			F20	NC		
E22	NC			F22	NC		
E24	NC			F23	NC		
E25	NC			F25	NC		
E27	NC			F26	NC		
E28	NC			F28	NC		
E30	NC			F29	NC		
E31	NC			F31	NC		
E33	NC			F32	NC		
E34	NC			F34	NC		
E36	NC			F35	NC		
E37	NC			F37	NC		
E39	VADJ_FMC_BUS			F38	NC		
				F40	VADJ_FMC_BUS		

Table 3-51: **J4 HPC1 FMC Section G and H Connections to XCZU7EV U1**

J4 Pin	Schematic Net Name	I/O Standard	U1 Pin		J4 Pin	Schematic Net Name	I/O Standard	U1 Pin
G2	FMC_HPC1_CLK1_M2C_P	LVDS			H1	NC		
G3	FMC_HPC1_CLK1_M2C_N	LVDS			H2	FMC_HPC1_PRSNT_M2C_B	(1)	
G6	FMC_HPC1_LA00_CC_P	LVDS	B18		H4	FMC_HPC1_CLK0_M2C_P	LVDS	F23
G7	FMC_HPC1_LA00_CC_N	LVDS	B19		H5	FMC_HPC1_CLK0_M2C_N	LVDS	E23
G9	FMC_HPC1_LA03_P	LVDS	J21		H7	FMC_HPC1_LA02_P	LVDS	K22
G10	FMC_HPC1_LA03_N	LVDS	J22		H8	FMC_HPC1_LA02_N	LVDS	K23
G12	FMC_HPC1_LA08_P	LVDS	J25		H10	FMC_HPC1_LA04_P	LVDS	J24
G13	FMC_HPC1_LA08_N	LVDS	H26		H11	FMC_HPC1_LA04_N	LVDS	H24
G15	FMC_HPC1_LA12_P	LVDS	E19		H13	FMC_HPC1_LA07_P	LVDS	D22
G16	FMC_HPC1_LA12_N	LVDS	D19		H14	FMC_HPC1_LA07_N	LVDS	C23
G18	FMC_HPC1_LA16_P	LVDS	C18		H16	FMC_HPC1_LA11_P	LVDS	A20
G19	FMC_HPC1_LA16_N	LVDS	C19		H17	FMC_HPC1_LA11_N	LVDS	A21
G21	NC				H19	FMC_HPC1_LA15_P	LVDS	A18
G22	NC				H20	FMC_HPC1_LA15_N	LVDS	A19
G24	NC				H22	NC		
G25	NC				H23	NC		
G27	NC				H25	NC		
G28	NC				H26	NC		
G30	NC				H28	NC		
G31	NC				H29	NC		
G33	NC				H31	NC		
G34	NC				H32	NC		
G36	NC				H34	NC		
G37	NC				H35	NC		
G39	VADJ_FMC_BUS				H37	NC		
					H38	NC		
					H40	VADJ_FMC_BUS		

Notes:

1. FMC_HPC1_PRSNT_M2C_B is the HPC FMC JTAG bypass switch U24.4 OE control signal is driven from I2C I/O expander U97.14.

Table 3-52: **J4 HPC1 FMC Section J and K Connections to XCZU7EV U1**

J4 Pin	Schematic Net Name	I/O Standard	U1 Pin		J4 Pin	Schematic Net Name	I/O Standard	U1 Pin
J2	NC				K1	NC		
J3	NC				K4	NC		
J6	NC				K5	NC		
J7	NC				K7	NC		
J9	NC				K8	NC		
J10	NC				K10	NC		
J12	NC				K11	NC		
J13	NC				K13	NC		
J15	NC				K14	NC		
J16	NC				K16	NC		
J18	NC				K17	NC		
J19	NC				K19	NC		
J21	NC				K20	NC		
J22	NC				K22	NC		
J24	NC				K23	NC		
J25	NC				K25	NC		
J27	NC				K26	NC		
J28	NC				K28	NC		
J30	NC				K29	NC		
J31	NC				K31	NC		
J33	NC				K32	NC		
J34	NC				K34	NC		
J36	NC				K35	NC		
J37	NC				K37	NC		
J39	NC				K38	NC		
					K40	NC		

Cooling Fan Connector

[Figure 2-1, near callout 10]

The ZCU106 cooling fan connector is shown in Figure 3-43.

The ZCU106 uses the Maxim MAX6643 fan controller, which autonomously controls the fan speed by controlling the pulse width modulation (PWM) signal to the fan based on the die temperature sensed via the FPGA's DXP and DXN pins. The fan rotates slowly (acoustically quiet) when the FPGA is cool and rotates faster as the FPGA heats up (acoustically noisy).

The fan speed (PWM) versus the FPGA die temperature algorithm along with the over temperature set point and fan failure alarm mechanisms are defined by the strapping resistors on the MAX6643 device. The over temperature and fan failures alarms can be monitored by the any available processor in the FPGA by polling the I2C expander, U97. See the MAX6643 [Ref 22] data sheet for more information on the device circuit implementation on this board.

Note: At initial power on, it is normal for the fan controller to energize at full speed for a few seconds.

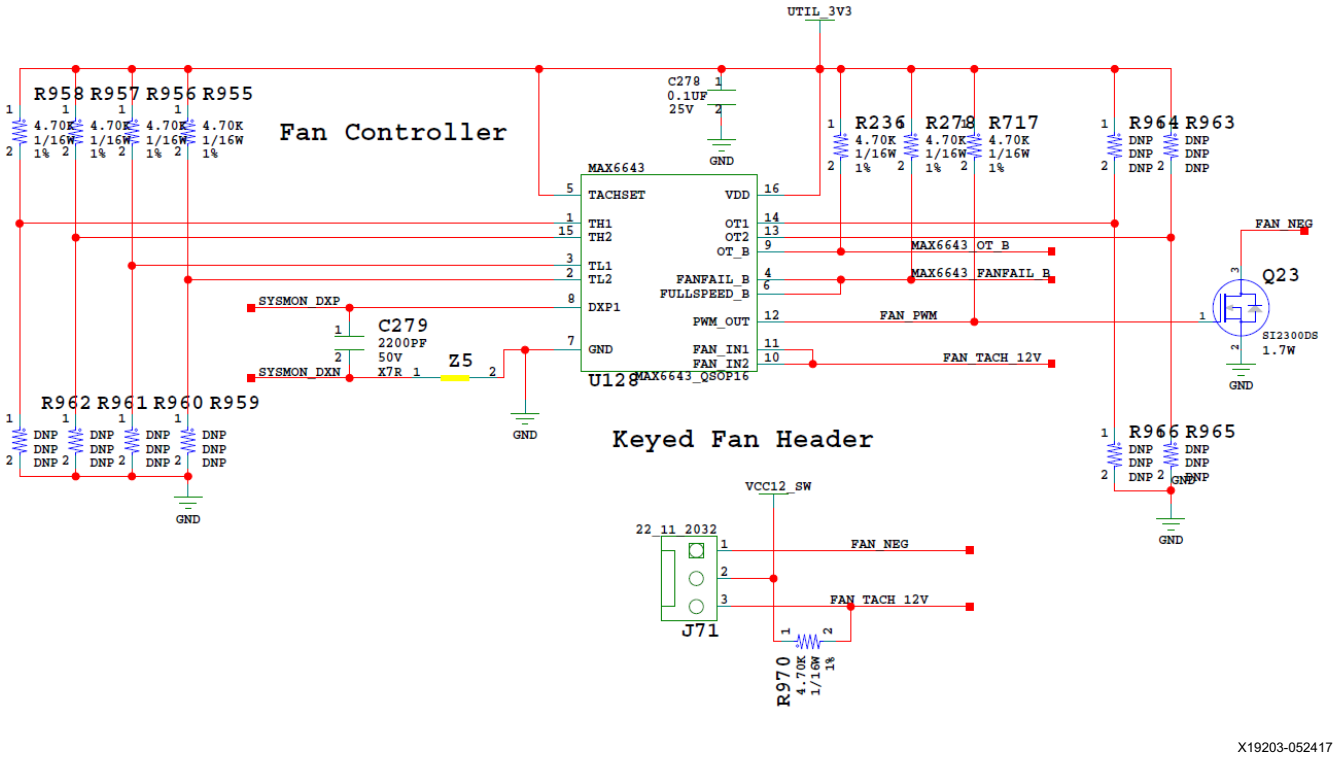


Figure 3-43: **ZCU106 12V Fan Controller**

VADJ_FMC Power Rail

The ZCU106 evaluation board implements the ANSI/VITA 57.1 section 5.5.1 IPMI support functionality. The power control of the V_{ADJ_FMC} power rail is managed by the U41 system controller. This rail powers both the FMC HPC0 (J5) and the FMC HPC1 (J4) V_{ADJ} pins, as well as the XCZU7EV HP banks 28, 67, and 68. The valid values of the V_{ADJ_FMC} rail are 1.2V, 1.5V, and 1.8V.

At power on, the system controller detects if an FMC module is connected to each interface:

- If no cards are attached to the FMC ports, the V_{ADJ} voltage is set to 1.8V.
- When one FMC card is attached, its IIC EEPROM is read to find a V_{ADJ} voltage supported by both the ZCU106 board and the FMC module, within the available choices of 1.8V, 1.5V, 1.2V, and 0.0V.
- When two FMC cards are attached with differing V_{ADJ} requirements, V_{ADJ_FMC} is set to the lowest value compatible with the ZCU106 board and the FMC modules, within the available choices of 1.8V, 1.5V, 1.2V, and 0.0V.
- If no valid information is found in an FMC card IIC EEPROM, the V_{ADJ_FMC} rail is set to 0.0V.

The system controller user interface allows the FMC IPMI routine to be overridden and an explicit value can be set for the V_{ADJ_FMC} rail. Override mode is useful for FMC mezzanine cards that do not contain valid IPMI EPROM data defined by the ANSI/VITA57.1 specification.

TI MSP430 System Controller

[Figure 2-1, callout 19]

The ZCU106 board includes an on-board MSP430 with integrated power advantage demonstration and system controller firmware. A host PC resident system controller user interface (SCUI) is provided on the ZCU106 web page. This GUI enables you to query and control select programmable features such as clocks, FMC functionality, and power system parameters. The ZCU106 web page also includes a tutorial on the SCUI (XTP433) [Ref 12] and board setup instructions (XTP435) [Ref 13].

The board setup instructions are summarized here:

1. Ensure that the Silicon Labs VCP USB-UART drivers are installed (see [Ref 7]).
2. Download the SCUI host PC application.
3. Connect the micro-USB to ZCU106 USB-UART connector (J83).
4. Power-cycle the ZCU106.
5. Observe that SYSCTLR LED0 (DS47) blinks and LED1 DS46 is illuminated.
6. Launch the SCUI.

The SCUI GUI is shown in Figure 3-44.

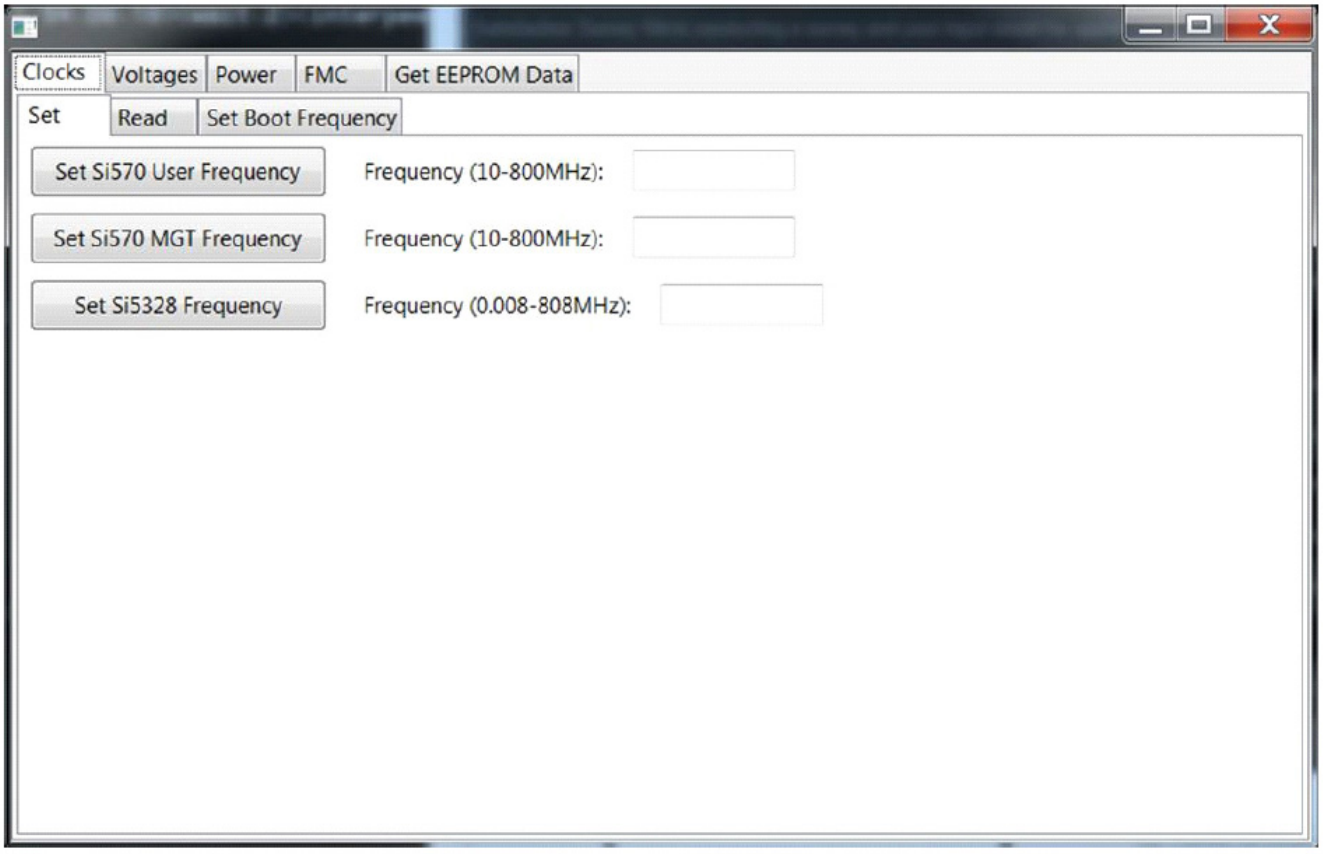


Figure 3-44: **System Controller User Interface**

On first use of the SCUI, select **FMC > Set VADJ > Boot-up** and click **USE FMC EEPROM Voltage**. The SCUI buttons are grayed out during command execution and return to their original appearance when ready to accept a new command.

See the *System Controller GUI Tutorial* (XTP433) [Ref 12] and the *ZCU106 Software Install and Board Setup Tutorial* (XTP435) [Ref 13] for more information on installing and using the system controller utility.

The MSP430 uses ID resistor encoding to allow the system controller utility to recognize which type of board is active. See Table 3-53 for the configuration of the ID encoding resistors R516 and R517.

Table 3-53: **MSP430 Board ID Encoding**

Zynq UltraScale Board	R516	R517
ZCU102	DNP	DNP
ZCU106	DNP	10K
Reserved	10K	DNP
Reserved	10K	10K

Switches

[Figure 2-1, callouts 27, 29, 31, and 46]

The ZCU106 board includes power, configuration, and reset switches:

- SW1 power on/off slide switch (callout 29)
- SW5 (PS_PROG_B), active-Low pushbutton (callout 31)
- SW3 (SRST_B), active-Low pushbutton (callout 27)
- SW4 (POR_B), active-Low pushbutton (callout 27)
- SW6 U1 MPSoC PS bank 503 4-pole mode DIP switch (callout 46)

Power On/Off Slide Switch

[Figure 2-1, callout 29]

The ZCU106 board power switch is SW1. Sliding the switch actuator from the off to the on position applies 12V power from J52, a 6-pin mini-fit connector. Green LED DS2 illuminates when the ZCU106 board power is on. See Board Power System, page 122 for details on the on-board power system.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into the ZCU106 board power connector J52. The ATX 6-pin connector has a different pin-out than J52. Connecting an ATX 6-pin connector into J52 damages the ZCU106 board and voids the board warranty.*

Figure 3-45 shows the power connector J52, power switch SW1, and LED indicator DS2.

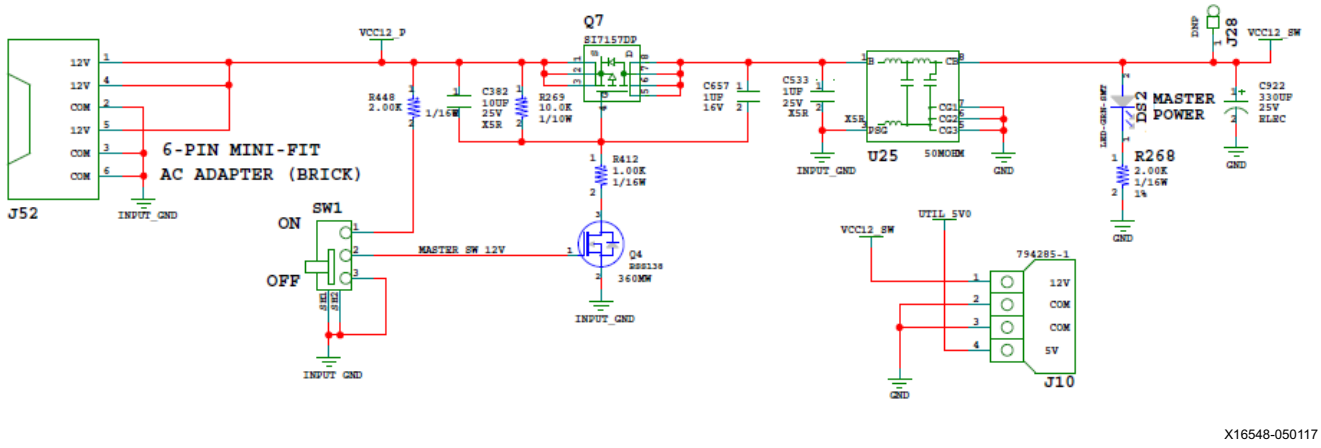


Figure 3-45: **Power Input**

Program_B Pushbutton

[Figure 2-1, callout 31]

PS_PROG_B pushbutton switch SW5 grounds the XCZU7EV MPSoC PS_PROG_B pin T24 when pressed (see Figure 3-46). This action clears the programmable logic configuration, which can then be acted on by the PS software. See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] for information about Zynq UltraScale+ MPSoC configuration.

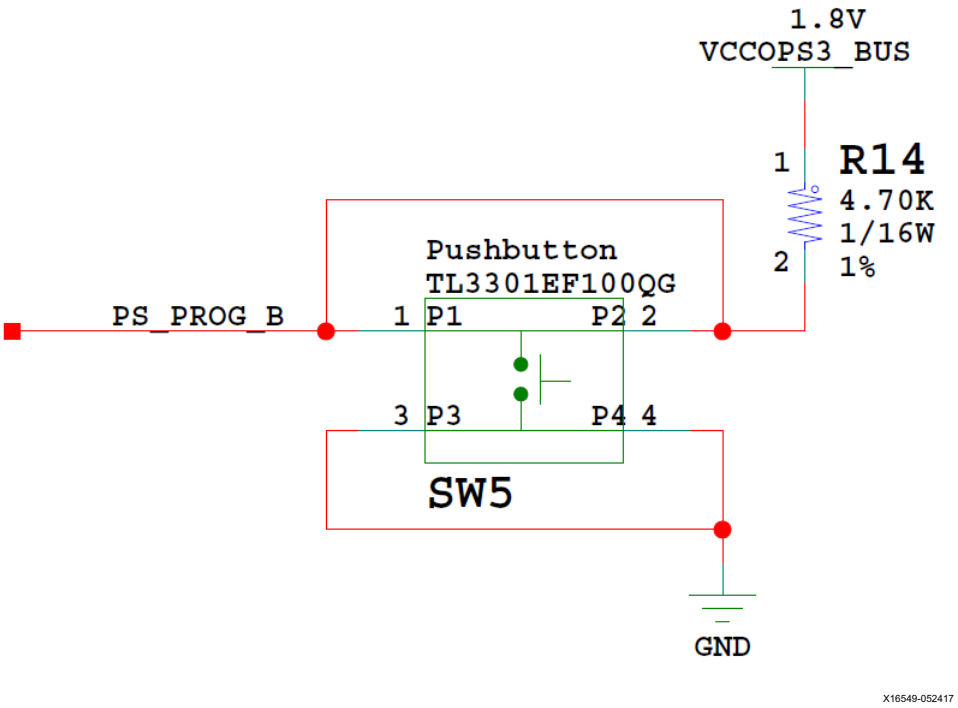


Figure 3-46: **PS_PROG_B Pushbutton Switch SW5**

System Reset Pushbuttons

[Figure 2-1, callout 27]

Figure 3-47 shows the reset circuitry for the PS.

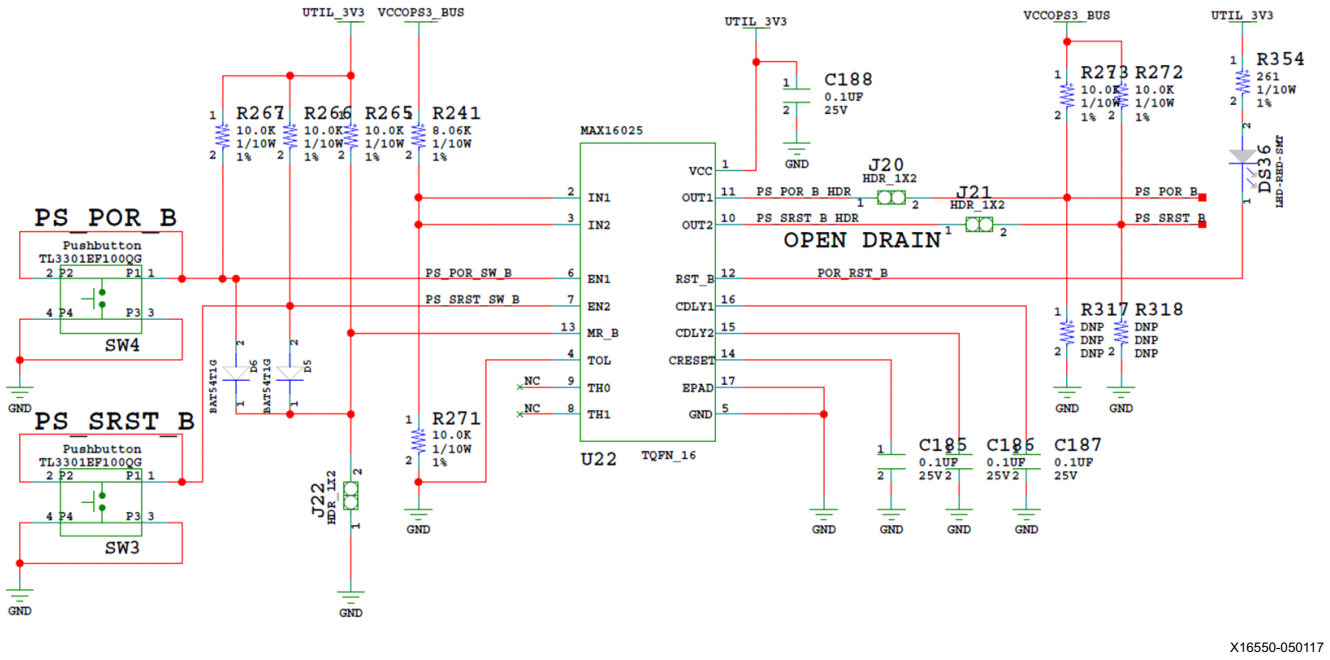


Figure 3-47: **PS SRST_B and POR_B Pushbutton Switches SW3 and SW4**

PS_POR_B Reset

Depressing and then releasing pushbutton SW4 causes net PS_POR_B to strobe Low. This reset is used to hold the PS in reset until all PS power supplies are at the required voltage levels. It must be held Low through PS power-up. PS_POR_B should be generated by the power supply power-good signal. When the voltage at IN1 is below its threshold or EN1 (P.B. switch SW4 is pressed) goes Low, OUT1 (PS_POR_B) goes Low.

PS_SRST_B Reset

Depressing and then releasing pushbutton SW3 causes net PS_SRST_B to strobe Low. This reset is used to force a system reset. It can be tied or pulled High, and can be High during the PS supply power ramps. When the voltage at IN2 is below its threshold or EN2 (P.B. switch SW3 is pressed) goes Low, OUT2 (PS_SRST_B) goes Low.

Active-Low reset output RST_B asserts when any of the monitored voltages (IN_) falls below the respective threshold, any EN_ goes Low, or MR is asserted. RST_B remains asserted for the reset time-out period after all of the monitored voltages exceed their respective threshold, all EN_ are High, all OUT_ are High, and MR is deasserted. See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] for information on the resets.

Board Power System

[Figure 2-1, callout 35]

The ZCU106 hosts a Maxim PMBus based power system. Each individual Maxim MAX20751EKX, MAX15301, or MAX15303 voltage regulator has a PMBus interface.

Figure 3-48 shows the ZCU106 power system block diagram.

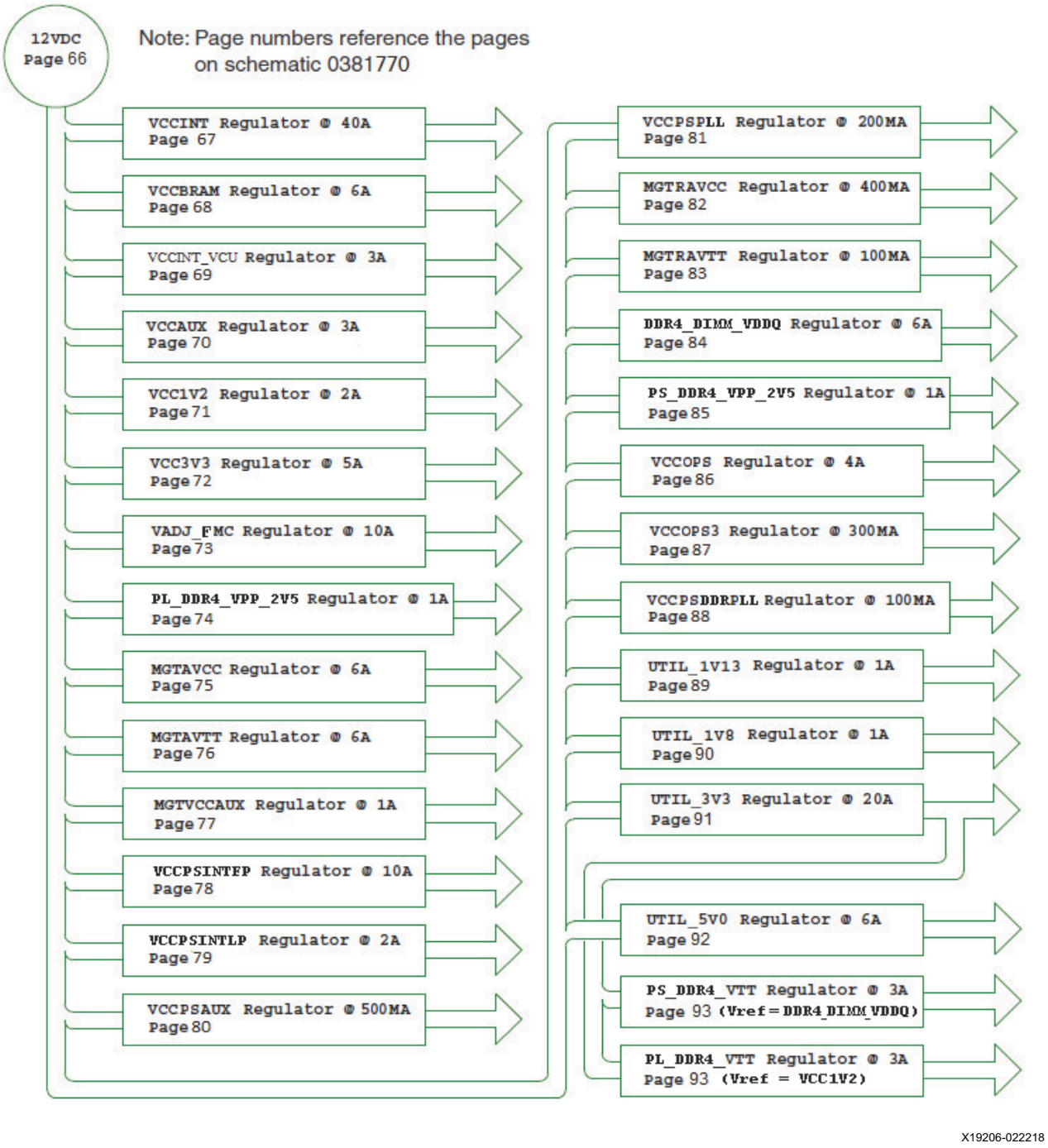


Figure 3-48: **Power System Block Diagram**

The ZCU106 evaluation board uses power regulators and PMBus compliant POL controllers from Maxim Integrated Circuits [Ref 22] to supply the core and auxiliary voltages listed in Table 3-54. The schematic page references are to 0381770.

Table 3-54: **Power System Devices**

Device Type	Ref. Des.	PMBus Addr.	Description	Power Rail Net Name	Power Rail Voltage	INA226 Address	Schem. Page
MAX15301	U47	0x13	Maxim InTune digital POL controller 20A	VCCINT	0.85V	PL:0x40	67
MAX15303	U7	0x14	Maxim InTune digital POL controller 6A	VCCBRAM	0.85V	PL:0x41	68
MAX8556	U153	NA	Maxim LDO regulator 3A	VCCINT_VCU	0.90V	PL:0x4A	69
MAX15303	U6	0x15	Maxim InTune digital POL controller 3A	VCCAUX	1.80V	PL:0x42	70
MAX15303	U10	0x16	Maxim InTune digital POL controller 2A	VCC1V2	1.20V	PL:0x43	71
MAX15303	U9	0x17	Maxim InTune digital POL controller 5A	VCC3V3	3.30V	PL:0x44	72
MAX15301	U63	0x18	Maxim InTune digital POL controller 5A	VADJ_FMC	1.80V	PL:0x45	73
MAX15027	U38	NA	Maxim LDO regulator 1A	PL_DDR4_VPP_2V5	2.5V	NA	74
MAX20751	U95	0x72	Maxim multiphase master with smart slave VT77518 6A	MGTAVCC	0.90V	PL:0x46	75
MAX20751	U96	0x73	Maxim multiphase master with smart slave VT77518 6A	MGTAVTT	1.20V	PL:0x47	76
MAX8869E	U14	NA	Maxim LDO regulator 1A	MGTVCCAUX	1.81V	NA	77
MAX15301	U46	0x0A	Maxim InTune digital POL controller 10A	VCCPSINTFP	0.85V	PS:0x40	78
MAX15303	U4	0x0B	Maxim InTune digital POL controller 2A	VCCPSINTLP	0.85V	PS:0x41	79
MAX8869E	U3	NA	Maxim LDO regulator 500MA	VCCPSAUX	1.81V	PS:0x42	80
MAX8869E	U17	NA	Maxim LDO regulator 200MA	VCCPSPLL	1.20V	PS:0x43	81
MAX8869E	U5	NA	Maxim LDO regulator 400MA	MGTRAVCC	0.85V	PS:0x44	82
MAX8869E	U12	NA	Maxim LDO regulator 100MA	MGTRAVTT	1.81V	PS:0x45	83
MAX15303	U18	0x1D	Maxim InTune digital POL controller 6A	DDR4_DIMM_VDDQ	1.20V	NA	84

Table 3-54: **Power System Devices *(Cont'd)***

Device Type	Ref. Des.	PMBus Addr.	Description	Power Rail Net Name	Power Rail Voltage	INA226 Address	Schem. Page
MAX15027	U39	NA	Maxim LDO regulator 1A	PS_DDR4_VPP_2V5	2.50V	NA	85
MAX15303	U13	0x10	Maxim InTune digital POL controller 4A	VCCOPS	1.80V	PS:0x47	86
MAX8869E	U31	NA	Maxim LDO regulator 300MA	VCCOPS3	1.81V	PS:0x4A	87
MAX8869E	U30	NA	Maxim LDO regulator 100MA	VCCPSDDRPLL	1.81V	PS:0x4B	88
MAX8869E	U143	NA	Maxim LDO regulator 1A	UTIL_1V13	1.13V	NA	89
MAX8869E	U37	NA	Maxim LDO regulator 1A	UTIL_1V8	1.80V	NA	90
MAX15301	U49	0x1A	Maxim InTune digital POL controller 20A	UTIL_3V3	3.30V	NA	91
MAX15303	U8	0x1B	Maxim InTune digital POL controller 6A	UTIL_5V0	5.00V	NA	92
TPS15200	U36	NA	Memory Vtt sink-source regulator 3A	PS_DDR4_VTT	0.6V	NA	93
TPS15200	U35	NA	Memory Vtt sink-source regulator 3A	PL_DDR4_VTT	0.6V	NA	93

The FMC HPC0 (J5) and FMC HPC1 (J4) VADJ pins are wired to the programmable rail VADJ_FMC_BUS. The VADJ_FMC_BUS rail is programmed to 1.80V by default. The valid values of the VADJ_FMC rail are 1.2V, 1.5V, and 1.8V. The VADJ_FMC derivative rail powers the XCZU7EV HP banks 28, 67, and 68 (see Table 3-2, page 28). Documentation describing PMBus programming for the Maxim InTune power controllers is available at the Maxim website [Ref 22]. The PCB layout and power system design meets the recommended criteria described in the *UltraScale Architecture PCB Design User Guide* (UG583) [Ref 3].

Monitoring Voltage and Current

Voltage and current monitoring and control are available for the Maxim power system controllers through the Maxim PowerTool graphical user interface. The on-board Maxim InTune power controllers listed in Table 3-54 are accessed through the 2x8 keyed shrouded PMBus connector J84, which is provided for use with the Maxim PowerTool USB cable (Maxim part number MAXPOWERTOOL001#). This cable can be ordered from the Maxim website [Ref 22]. The associated Maxim PowerTool GUI can be downloaded from the Maxim website. This is the simplest and most convenient way to monitor the voltage and current values for the Maxim PMBus programmed power rails listed in Table 3-54.

Each PMBus programmable Maxim controller can report the voltage and current of its controlled rail to the Maxim GUI. A subset of the programmable rails and two fixed rails have a TI INA226 PMBus power monitor circuit with connections to the rail series current sense resistor. This arrangement permits the INA226 to report the sensed parameters separately on the PMBus. The rails configured with the INA226 power monitors are shown in Table 3-54.

As described in I2C0 (MIO 14-15), page 60, the I2C0 bus provides access to the PMBus power controllers and the PS-side and PL-side INA226 power monitors via the U60 PCA9544A bus switch. All PMBus controlled Maxim regulators are tied to the MAXIM_PMBUS, while the INA226 power monitors are separated to PS_PMBUS and PL_PMBUS.

Figure 3-17, page 61 and Table 3-21, page 63 document the I2C0 bus access path to the Maxim PMBus controllers and INA226 power monitor op amps. Also, see schematic 0381770. The MPSoC core related power rail measurements (PL_PMBUS) and PS related power measurements (PS_PMBUS) are accessible to the system controller and MPSoC PL logic through their respective I2C0 bus connections.

These measurements are displayed in the system controller menu selections. The Maxim controller PMBus is accessible by the system controller, which can also display the rail voltage measurement made by its sourcing Maxim controller. User IP in the MPSoC PL can access the same set of PMBus resident devices through the logic I2C0 connections.

VITA 57.1 FMC Connector Pinouts

Overview

Figure A-1 shows the pinout of the FPGA mezzanine card (FMC) high pin count (HPC) J2 defined by the VITA 57.1 FMC specification. For a description of how the ZCU106 evaluation board implements the FMC specification, see FPGA Mezzanine Card Interface, page 104, FMC HPC0 Connector J5, page 104, and FMC HPC1 Connector J4, page 110.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
2	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C	GND	DP9_M2C_P	GND
5	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

X19207-050117

Figure A-1: **FMC HPC Connector Pinouts**

Master Constraints File Listing

Overview

The master Xilinx design constraints (XDC) file template for the ZCU106 board provides for designs targeting the ZCU106 evaluation board. Net names in the constraints listed correlate with net names on the latest ZCU106 evaluation board schematic. Identify the appropriate pins and replace the net names with net names in the user RTL. See the *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 9] for more information.

For detailed I/O standards information required for a particular interface, see the constraint files generated by tools such as the memory interface generator (MIG) and base system builder (BSB).

The FMC connectors J5 (HPC0) and J4 (HPC1) are connected to MPSoC banks powered by the variable voltage V_{AJ_FMC}. Because different FMC cards implement different circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

IMPORTANT: *The XDC file can be accessed on the Zynq UltraScale+ ZCU106 Development Kit website.*

ZCU106 Board Constraints File Listing

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#CLOCKS

#PS_REF_CLK 33.33 MHz U69 SI5341B
#Other net   PACKAGE_PIN R24 - PS_REF_CLK Bank 503 - PS_REF_CLK

#CLK_125 125 MHz U69 SI5341B
set_property PACKAGE_PIN G9       [get_ports "CLK_125_N"] ;
set_property IOSTANDARD  LVDS     [get_ports "CLK_125_N"] ;
set_property PACKAGE_PIN H9       [get_ports "CLK_125_P"] ;
set_property IOSTANDARD  LVDS     [get_ports "CLK_125_P"] ;

#CLK_74_25 74.25 MHz U69 SI5341B
set_property PACKAGE_PIN D14      [get_ports "CLK_74_25_N"] ;
set_property IOSTANDARD  LVDS     [get_ports "CLK_74_25_N"] ;
set_property PACKAGE_PIN D15      [get_ports "CLK_74_25_P"] ;
set_property IOSTANDARD  LVDS     [get_ports "CLK_74_25_P"] ;
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#USER_SI570 300 MHz
set_property PACKAGE_PIN AJ12        [get_ports "USER_SI570_N"] ;
set_property IOSTANDARD  DIFF_SSTL12 [get_ports "USER_SI570_N"] ;
set_property PACKAGE_PIN AH12        [get_ports "USER_SI570_P"] ;
set_property IOSTANDARD  DIFF_SSTL12 [get_ports "USER_SI570_P"] ;

#For completeness, the MGT clocks are documented here:

#MGTH 223 HDMI I/F
set_property PACKAGE_PIN AD7      [get_ports "HDMI_SI5324_OUT_C_N"]
set_property PACKAGE_PIN AD8      [get_ports "HDMI_SI5324_OUT_C_P"]
set_property PACKAGE_PIN AC9      [get_ports "HDMI_RX_CLK_C_N"] ;
set_property PACKAGE_PIN AC10     [get_ports "HDMI_RX_CLK_C_P"] ;

#MGTH 224 PCIE I/F
set_property PACKAGE_PIN AB7      [get_ports "PCIE_CLK_N"] ;
set_property PACKAGE_PIN AB8      [get_ports "PCIE_CLK_P"] ;

#MGTH 225 SDI, SMA_MGT, SFP0/1 I/F
set_property PACKAGE_PIN Y7       [get_ports "FMC_HPC1_GBTCLK0_M2C_C_N"] ;
set_property PACKAGE_PIN Y8       [get_ports "FMC_HPC1_GBTCLK0_M2C_C_P"] ;
set_property PACKAGE_PIN W9       [get_ports "SFP_SI5328_OUT_C_N"] ;
set_property PACKAGE_PIN W10      [get_ports "SFP_SI5328_OUT_C_P"] ;

#MGTH 226 HPC0 I/F
set_property PACKAGE_PIN V7       [get_ports "FMC_HPC0_GBTCLK0_M2C_C_N"] ;
set_property PACKAGE_PIN V8       [get_ports "FMC_HPC0_GBTCLK0_M2C_C_P"] ;
set_property PACKAGE_PIN U9       [get_ports "USER_MGT_SI570_CLOCK1_C_N"] ;
set_property PACKAGE_PIN U10      [get_ports "USER_MGT_SI570_CLOCK1_C_P"] ;

#MGTH 227 HPC0 I/F
set_property PACKAGE_PIN T7       [get_ports "FMC_HPC0_GBTCLK1_M2C_C_N"] ;
set_property PACKAGE_PIN T8       [get_ports "FMC_HPC0_GBTCLK1_M2C_C_P"] ;
set_property PACKAGE_PIN R9       [get_ports "USER_MGT_SI570_CLOCK2_C_N"] ;
set_property PACKAGE_PIN R10      [get_ports "USER_MGT_SI570_CLOCK2_C_P"] ;

#GTR 505 FIXED CLOCKS SOURCED FROM U69 SI5341B
#Other net   PACKAGE_PIN P28 - GTR_REF_CLK_SATA_C_N Bank 505 - PS_MGTREFCLK1N_505
#Other net   PACKAGE_PIN P27 - GTR_REF_CLK_SATA_C_P Bank 505 - PS_MGTREFCLK1P_505
#Other net   PACKAGE_PIN M28 - GTR_REF_CLK_USB3_C_N Bank 505 - PS_MGTREFCLK2N_505
#Other net   PACKAGE_PIN M27 - GTR_REF_CLK_USB3_C_P Bank 505 - PS_MGTREFCLK2P_505
#Other net   PACKAGE_PIN M32 - GTR_REF_CLK_DP_C_N   Bank 505 - PS_MGTREFCLK3N_505
#Other net   PACKAGE_PIN M31 - GTR_REF_CLK_DP_C_P   Bank 505 - PS_MGTREFCLK3P_505

#MEMORY
#DDR4 SODIMM J1 is a PS DDR Bank 504 Interface
#Other net PACKAGE_PIN AN34 - DR4_SODIMM_A0      Bank 504 - PS_DDR_A0
#Other net PACKAGE_PIN AM34 - DR4_SODIMM_A1      Bank 504 - PS_DDR_A1
#Other net PACKAGE_PIN AM33 - DR4_SODIMM_A2      Bank 504 - PS_DDR_A2
#Other net PACKAGE_PIN AL34 - DR4_SODIMM_A3      Bank 504 - PS_DDR_A3
#Other net PACKAGE_PIN AL33 - DR4_SODIMM_A4      Bank 504 - PS_DDR_A4
#Other net PACKAGE_PIN AK33 - DR4_SODIMM_A5      Bank 504 - PS_DDR_A5
#Other net PACKAGE_PIN AK30 - DR4_SODIMM_A6      Bank 504 - PS_DDR_A6
#Other net PACKAGE_PIN AJ30 - DR4_SODIMM_A7      Bank 504 - PS_DDR_A7
#Other net PACKAGE_PIN AJ31 - DR4_SODIMM_A8      Bank 504 - PS_DDR_A8
#Other net PACKAGE_PIN AH31 - DR4_SODIMM_A9      Bank 504 - PS_DDR_A9
#Other net PACKAGE_PIN AG31 - DR4_SODIMM_A10     Bank 504 - PS_DDR_A10
#Other net PACKAGE_PIN AF31 - DR4_SODIMM_A11     Bank 504 - PS_DDR_A11
#Other net PACKAGE_PIN AG30 - DR4_SODIMM_A12     Bank 504 - PS_DDR_A12
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#Other net PACKAGE_PIN AF30 - DR4_SODIMM_A13     Bank 504 - PS_DDR_A13
#Other net PACKAGE_PIN AG29 - DR4_SODIMM_WE_B    Bank 504 - PS_DDR_A14
#Other net PACKAGE_PIN AG28 - DR4_SODIMM_CAS_B   Bank 504 - PS_DDR_A15
#Other net PACKAGE_PIN AF28 - DR4_SODIMM_RAS_B   Bank 504 - PS_DDR_A16
#Other net PACKAGE_PIN AE27 - DR4_SODIMM_BA0     Bank 504 - PS_DDR_BA0
#Other net PACKAGE_PIN AE28 - DR4_SODIMM_BA1     Bank 504 - PS_DDR_BA1
#Other net PACKAGE_PIN AD27 - DR4_SODIMM_BG0     Bank 504 - PS_DDR_BG0
#Other net PACKAGE_PIN AF27 - DR4_SODIMM_BG1     Bank 504 - PS_DDR_BG1
#Other net PACKAGE_PIN AN24 - DR4_SODIMM_DM0_B   Bank 504 - PS_DDR_DM0
#Other net PACKAGE_PIN AM29 - DR4_SODIMM_DM1_B   Bank 504 - PS_DDR_DM1
#Other net PACKAGE_PIN AH24 - DR4_SODIMM_DM2_B   Bank 504 - PS_DDR_DM2
#Other net PACKAGE_PIN AJ29 - DR4_SODIMM_DM3_B   Bank 504 - PS_DDR_DM3
#Other net PACKAGE_PIN AD29 - DR4_SODIMM_DM4_B   Bank 504 - PS_DDR_DM4
#Other net PACKAGE_PIN Y29  - DR4_SODIMM_DM5_B   Bank 504 - PS_DDR_DM5
#Other net PACKAGE_PIN AC32 - DR4_SODIMM_DM6_B   Bank 504 - PS_DDR_DM6
#Other net PACKAGE_PIN Y32  - DR4_SODIMM_DM7_B   Bank 504 - PS_DDR_DM7
#Other net PACKAGE_PIN AF34 - DR4_SODIMM_DM8_B   Bank 504 - PS_DDR_DM8
#Other net PACKAGE_PIN AN33 - DR4_SODIMM_CKE0    Bank 504 - PS_DDR_CKE0
#Other net PACKAGE_PIN AL31 - DR4_SODIMM_CK0_T   Bank 504 - PS_DDR_CK0
#Other net PACKAGE_PIN AN32 - DR4_SODIMM_CK0_C   Bank 504 - PS_DDR_CK_N0
#Other net PACKAGE_PIN AH32 - DR4_SODIMM_CKE1    Bank 504 - PS_DDR_CKE1
#Other net PACKAGE_PIN AL30 - DR4_SODIMM_CK1_T   Bank 504 - PS_DDR_CK1
#Other net PACKAGE_PIN AL32 - DR4_SODIMM_CK1_C   Bank 504 - PS_DDR_CK_N1
#Other net PACKAGE_PIN AA26 - DR4_SODIMM_PARITY  Bank 504 - PS_DDR_PARITY
#Other net PACKAGE_PIN AE25 - DR4_SODIMM_ACT_B   Bank 504 - PS_DDR_ACT_N
#Other net PACKAGE_PIN AB26 - DR4_SODIMM_ALERT_B Bank 504 - PS_DDR_ALERT_N
#Other net PACKAGE_PIN AP32 - DR4_SODIMM_ODT0    Bank 504 - PS_DDR_ODT0
#Other net PACKAGE_PIN AJ32 - DR4_SODIMM_ODT1    Bank 504 - PS_DDR_ODT1
#Other net PACKAGE_PIN AP33 - DR4_SODIMM_CS0_B   Bank 504 - PS_DDR_CS_N0
#Other net PACKAGE_PIN AK32 - DR4_SODIMM_CS1_B   Bank 504 - PS_DDR_CS_N1
#Other net PACKAGE_PIN AD26 - DDR4_SODIMM_RESET_B Bank 504 - PS_DDR_RAM_RST_N
#Other net PACKAGE_PIN AP27 - DR4_SODIMM_DQ0     Bank 504 - PS_DDR_DQ0
#Other net PACKAGE_PIN AP25 - DR4_SODIMM_DQ1     Bank 504 - PS_DDR_DQ1
#Other net PACKAGE_PIN AP26 - DR4_SODIMM_DQ2     Bank 504 - PS_DDR_DQ2
#Other net PACKAGE_PIN AM26 - DR4_SODIMM_DQ3     Bank 504 - PS_DDR_DQ3
#Other net PACKAGE_PIN AP24 - DR4_SODIMM_DQ4     Bank 504 - PS_DDR_DQ4
#Other net PACKAGE_PIN AL25 - DR4_SODIMM_DQ5     Bank 504 - PS_DDR_DQ5
#Other net PACKAGE_PIN AM25 - DR4_SODIMM_DQ6     Bank 504 - PS_DDR_DQ6
#Other net PACKAGE_PIN AM24 - DR4_SODIMM_DQ7     Bank 504 - PS_DDR_DQ7
#Other net PACKAGE_PIN AM28 - DR4_SODIMM_DQ8     Bank 504 - PS_DDR_DQ8
#Other net PACKAGE_PIN AN28 - DR4_SODIMM_DQ9     Bank 504 - PS_DDR_DQ9
#Other net PACKAGE_PIN AP29 - DR4_SODIMM_DQ10    Bank 504 - PS_DDR_DQ10
#Other net PACKAGE_PIN AP28 - DR4_SODIMM_DQ11    Bank 504 - PS_DDR_DQ11
#Other net PACKAGE_PIN AM31 - DR4_SODIMM_DQ12    Bank 504 - PS_DDR_DQ12
#Other net PACKAGE_PIN AP31 - DR4_SODIMM_DQ13    Bank 504 - PS_DDR_DQ13
#Other net PACKAGE_PIN AN31 - DR4_SODIMM_DQ14    Bank 504 - PS_DDR_DQ14
#Other net PACKAGE_PIN AM30 - DR4_SODIMM_DQ15    Bank 504 - PS_DDR_DQ15
#Other net PACKAGE_PIN AF25 - DR4_SODIMM_DQ16    Bank 504 - PS_DDR_DQ16
#Other net PACKAGE_PIN AG25 - DR4_SODIMM_DQ17    Bank 504 - PS_DDR_DQ17
#Other net PACKAGE_PIN AG26 - DR4_SODIMM_DQ18    Bank 504 - PS_DDR_DQ18
#Other net PACKAGE_PIN AJ25 - DR4_SODIMM_DQ19    Bank 504 - PS_DDR_DQ19
#Other net PACKAGE_PIN AG24 - DR4_SODIMM_DQ20    Bank 504 - PS_DDR_DQ20
#Other net PACKAGE_PIN AK25 - DR4_SODIMM_DQ21    Bank 504 - PS_DDR_DQ21
#Other net PACKAGE_PIN AJ24 - DR4_SODIMM_DQ22    Bank 504 - PS_DDR_DQ22
#Other net PACKAGE_PIN AK24 - DR4_SODIMM_DQ23    Bank 504 - PS_DDR_DQ23
#Other net PACKAGE_PIN AH28 - DR4_SODIMM_DQ24    Bank 504 - PS_DDR_DQ24
#Other net PACKAGE_PIN AH27 - DR4_SODIMM_DQ25    Bank 504 - PS_DDR_DQ25
#Other net PACKAGE_PIN AJ27 - DR4_SODIMM_DQ26    Bank 504 - PS_DDR_DQ26
#Other net PACKAGE_PIN AK27 - DR4_SODIMM_DQ27    Bank 504 - PS_DDR_DQ27
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#Other net PACKAGE_PIN AL26 - DR4_SODIMM_DQ28    Bank 504 - PS_DDR_DQ28
#Other net PACKAGE_PIN AL27 - DR4_SODIMM_DQ29    Bank 504 - PS_DDR_DQ29
#Other net PACKAGE_PIN AH29 - DR4_SODIMM_DQ30    Bank 504 - PS_DDR_DQ30
#Other net PACKAGE_PIN AL28 - DR4_SODIMM_DQ31    Bank 504 - PS_DDR_DQ31
#Other net PACKAGE_PIN AB29 - DR4_SODIMM_DQ32    Bank 504 - PS_DDR_DQ32
#Other net PACKAGE_PIN AB30 - DR4_SODIMM_DQ33    Bank 504 - PS_DDR_DQ33
#Other net PACKAGE_PIN AC29 - DR4_SODIMM_DQ34    Bank 504 - PS_DDR_DQ34
#Other net PACKAGE_PIN AD32 - DR4_SODIMM_DQ35    Bank 504 - PS_DDR_DQ35
#Other net PACKAGE_PIN AC31 - DR4_SODIMM_DQ36    Bank 504 - PS_DDR_DQ36
#Other net PACKAGE_PIN AE30 - DR4_SODIMM_DQ37    Bank 504 - PS_DDR_DQ37
#Other net PACKAGE_PIN AC28 - DR4_SODIMM_DQ38    Bank 504 - PS_DDR_DQ38
#Other net PACKAGE_PIN AE29 - DR4_SODIMM_DQ39    Bank 504 - PS_DDR_DQ39
#Other net PACKAGE_PIN AC27 - DR4_SODIMM_DQ40    Bank 504 - PS_DDR_DQ40
#Other net PACKAGE_PIN AA27 - DR4_SODIMM_DQ41    Bank 504 - PS_DDR_DQ41
#Other net PACKAGE_PIN AA28 - DR4_SODIMM_DQ42    Bank 504 - PS_DDR_DQ42
#Other net PACKAGE_PIN AB28 - DR4_SODIMM_DQ43    Bank 504 - PS_DDR_DQ43
#Other net PACKAGE_PIN W27  - DR4_SODIMM_DQ44    Bank 504 - PS_DDR_DQ44
#Other net PACKAGE_PIN W29  - DR4_SODIMM_DQ45    Bank 504 - PS_DDR_DQ45
#Other net PACKAGE_PIN W28  - DR4_SODIMM_DQ46    Bank 504 - PS_DDR_DQ46
#Other net PACKAGE_PIN V27  - DR4_SODIMM_DQ47    Bank 504 - PS_DDR_DQ47
#Other net PACKAGE_PIN AA32 - DR4_SODIMM_DQ48    Bank 504 - PS_DDR_DQ48
#Other net PACKAGE_PIN AA33 - DR4_SODIMM_DQ49    Bank 504 - PS_DDR_DQ49
#Other net PACKAGE_PIN AA34 - DR4_SODIMM_DQ50    Bank 504 - PS_DDR_DQ50
#Other net PACKAGE_PIN AE34 - DR4_SODIMM_DQ51    Bank 504 - PS_DDR_DQ51
#Other net PACKAGE_PIN AD34 - DR4_SODIMM_DQ52    Bank 504 - PS_DDR_DQ52
#Other net PACKAGE_PIN AB31 - DR4_SODIMM_DQ53    Bank 504 - PS_DDR_DQ53
#Other net PACKAGE_PIN AC34 - DR4_SODIMM_DQ54    Bank 504 - PS_DDR_DQ54
#Other net PACKAGE_PIN AC33 - DR4_SODIMM_DQ55    Bank 504 - PS_DDR_DQ55
#Other net PACKAGE_PIN AA30 - DR4_SODIMM_DQ56    Bank 504 - PS_DDR_DQ56
#Other net PACKAGE_PIN Y30  - DR4_SODIMM_DQ57    Bank 504 - PS_DDR_DQ57
#Other net PACKAGE_PIN AA31 - DR4_SODIMM_DQ58    Bank 504 - PS_DDR_DQ58
#Other net PACKAGE_PIN W30  - DR4_SODIMM_DQ59    Bank 504 - PS_DDR_DQ59
#Other net PACKAGE_PIN Y33  - DR4_SODIMM_DQ60    Bank 504 - PS_DDR_DQ60
#Other net PACKAGE_PIN W33  - DR4_SODIMM_DQ61    Bank 504 - PS_DDR_DQ61
#Other net PACKAGE_PIN W34  - DR4_SODIMM_DQ62    Bank 504 - PS_DDR_DQ62
#Other net PACKAGE_PIN Y34  - DR4_SODIMM_DQ63    Bank 504 - PS_DDR_DQ63
#Other net PACKAGE_PIN AF32 - DR4_SODIMM_CB0     Bank 504 - PS_DDR_DQ64
#Other net PACKAGE_PIN AE32 - DR4_SODIMM_CB1     Bank 504 - PS_DDR_DQ65
#Other net PACKAGE_PIN AH33 - DR4_SODIMM_CB2     Bank 504 - PS_DDR_DQ66
#Other net PACKAGE_PIN AE33 - DR4_SODIMM_CB3     Bank 504 - PS_DDR_DQ67
#Other net PACKAGE_PIN AF33 - DR4_SODIMM_CB4     Bank 504 - PS_DDR_DQ68
#Other net PACKAGE_PIN AH34 - DR4_SODIMM_CB5     Bank 504 - PS_DDR_DQ69
#Other net PACKAGE_PIN AJ34 - DR4_SODIMM_CB6     Bank 504 - PS_DDR_DQ70
#Other net PACKAGE_PIN AK34 - DR4_SODIMM_CB7     Bank 504 - PS_DDR_DQ71
#Other net PACKAGE_PIN AN27 - DR4_SODIMM_DQS0_C  Bank 504 - PS_DDR_DQS_N0
#Other net PACKAGE_PIN AN26 - DR4_SODIMM_DQS0_T  Bank 504 - PS_DDR_DQS_P0
#Other net PACKAGE_PIN AP30 - DR4_SODIMM_DQS1_C  Bank 504 - PS_DDR_DQS_N1
#Other net PACKAGE_PIN AN29 - DR4_SODIMM_DQS1_T  Bank 504 - PS_DDR_DQS_P1
#Other net PACKAGE_PIN AJ26 - DR4_SODIMM_DQS2_C  Bank 504 - PS_DDR_DQS_N2
#Other net PACKAGE_PIN AH26 - DR4_SODIMM_DQS2_T  Bank 504 - PS_DDR_DQS_P2
#Other net PACKAGE_PIN AK29 - DR4_SODIMM_DQS3_C  Bank 504 - PS_DDR_DQS_N3
#Other net PACKAGE_PIN AK28 - DR4_SODIMM_DQS3_T  Bank 504 - PS_DDR_DQS_P3
#Other net PACKAGE_PIN AD31 - DR4_SODIMM_DQS4_C  Bank 504 - PS_DDR_DQS_N4
#Other net PACKAGE_PIN AD30 - DR4_SODIMM_DQS4_T  Bank 504 - PS_DDR_DQS_P4
#Other net PACKAGE_PIN Y28  - DR4_SODIMM_DQS5_C  Bank 504 - PS_DDR_DQS_N5
#Other net PACKAGE_PIN Y27  - DR4_SODIMM_DQS5_T  Bank 504 - PS_DDR_DQS_P5
#Other net PACKAGE_PIN AB34 - DR4_SODIMM_DQS6_C  Bank 504 - PS_DDR_DQS_N6
#Other net PACKAGE_PIN AB33 - DR4_SODIMM_DQS6_T  Bank 504 - PS_DDR_DQS_P6
#Other net PACKAGE_PIN W32  - DR4_SODIMM_DQS7_C  Bank 504 - PS_DDR_DQS_N7
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#Other net PACKAGE_PIN W31  - DR4_SODIMM_DQS7_T  Bank 504 - PS_DDR_DQS_P7
#Other net PACKAGE_PIN AG34 - DR4_SODIMM_DQS8_C  Bank 504 - PS_DDR_DQS_N8
#Other net PACKAGE_PIN AG33 - DR4_SODIMM_DQS8_T  Bank 504 - PS_DDR_DQS_P8

#DDR4 COMPONENT 64-BIT
set_propertyPACKAGE_PIN AK9       [get_ports "DDR4_A0"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_A0"] ;
set_propertyPACKAGE_PIN AG11      [get_ports "DDR4_A1"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_A1"] ;
set_propertyPACKAGE_PIN AJ10      [get_ports "DDR4_A2"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_A2"] ;
set_propertyPACKAGE_PIN AL8       [get_ports "DDR4_A3"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_A3"] ;
set_propertyPACKAGE_PIN AK10      [get_ports "DDR4_A4"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_A4"] ;
set_propertyPACKAGE_PIN AH8       [get_ports "DDR4_A5"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_A5"] ;
set_propertyPACKAGE_PIN AJ9       [get_ports "DDR4_A6"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_A6"] ;
set_propertyPACKAGE_PIN AG8       [get_ports "DDR4_A7"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_A7"] ;
set_propertyPACKAGE_PIN AH9       [get_ports "DDR4_A8"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_A8"] ;
set_propertyPACKAGE_PIN AG10      [get_ports "DDR4_A9"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_A9"] ;
set_propertyPACKAGE_PIN AH13      [get_ports "DDR4_A10"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_A10"] ;
set_propertyPACKAGE_PIN AG9       [get_ports "DDR4_A11"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_A11"] ;
set_propertyPACKAGE_PIN AM13      [get_ports "DDR4_A12"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_A12"] ;
set_propertyPACKAGE_PIN AF8       [get_ports "DDR4_A13"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_A13"] ;
set_propertyPACKAGE_PIN AC12      [get_ports "DDR4_A14_WE_B"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_A14_WE_B"] ;
set_propertyPACKAGE_PIN AE12      [get_ports "DDR4_A15_CAS_B"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_A15_CAS_B"] ;
set_propertyPACKAGE_PIN AF11      [get_ports "DDR4_A16_RAS_B"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_A16_RAS_B"] ;
set_propertyPACKAGE_PIN AK8       [get_ports "DDR4_BA0"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_BA0"] ;
set_propertyPACKAGE_PIN AL12      [get_ports "DDR4_BA1"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_BA1"] ;
set_propertyPACKAGE_PIN AE14      [get_ports "DDR4_BG0"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_BG0"] ;
set_propertyPACKAGE_PIN AB13      [get_ports "DDR4_CKE"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_CKE"] ;
set_propertyPACKAGE_PIN AJ11      [get_ports "DDR4_CK_C"] ;
set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_CK_C"] ;
set_propertyPACKAGE_PIN AH11      [get_ports "DDR4_CK_T"] ;
set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_CK_T"] ;
set_propertyPACKAGE_PIN AC13      [get_ports "DDR4_PAR"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_PAR"] ;
set_propertyPACKAGE_PIN AD14      [get_ports "DDR4_ACT_B"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_ACT_B"] ;
set_propertyPACKAGE_PIN AF10      [get_ports "DDR4_ODT"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_ODT"] ;
set_propertyPACKAGE_PIN AF12      [get_ports "DDR4_RESET_B"] ;
set_propertyIOSTANDARD LVCMOS12  [get_ports "DDR4_RESET_B"] ;
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set_propertyPACKAGE_PIN AD12      [get_ports "DDR4_CS_B"] ;
set_propertyIOSTANDARD SSTL12    [get_ports "DDR4_CS_B"] ;
set_propertyPACKAGE_PIN AH18      [get_ports "DDR4_DM0"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DM0"] ;
set_propertyPACKAGE_PIN AD15      [get_ports "DDR4_DM1"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DM1"] ;
set_propertyPACKAGE_PIN AM16      [get_ports "DDR4_DM2"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DM2"] ;
set_propertyPACKAGE_PIN AP18      [get_ports "DDR4_DM3"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DM3"] ;
set_propertyPACKAGE_PIN AE18      [get_ports "DDR4_DM4"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DM4"] ;
set_propertyPACKAGE_PIN AH22      [get_ports "DDR4_DM5"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DM5"] ;
set_propertyPACKAGE_PIN AL20      [get_ports "DDR4_DM6"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DM6"] ;
set_propertyPACKAGE_PIN AP19      [get_ports "DDR4_DM7"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DM7"] ;
set_propertyPACKAGE_PIN AF16      [get_ports "DDR4_DQ0"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ0"] ;
set_propertyPACKAGE_PIN AF18      [get_ports "DDR4_DQ1"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ1"] ;
set_propertyPACKAGE_PIN AG15      [get_ports "DDR4_DQ2"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ2"] ;
set_propertyPACKAGE_PIN AF17      [get_ports "DDR4_DQ3"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ3"] ;
set_propertyPACKAGE_PIN AF15      [get_ports "DDR4_DQ4"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ4"] ;
set_propertyPACKAGE_PIN AG18      [get_ports "DDR4_DQ5"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ5"] ;
set_propertyPACKAGE_PIN AG14      [get_ports "DDR4_DQ6"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ6"] ;
set_propertyPACKAGE_PIN AE17      [get_ports "DDR4_DQ7"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ7"] ;
set_propertyPACKAGE_PIN AA14      [get_ports "DDR4_DQ8"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ8"] ;
set_propertyPACKAGE_PIN AC16      [get_ports "DDR4_DQ9"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ9"] ;
set_propertyPACKAGE_PIN AB15      [get_ports "DDR4_DQ10"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ10"] ;
set_propertyPACKAGE_PIN AD16      [get_ports "DDR4_DQ11"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ11"] ;
set_propertyPACKAGE_PIN AB16      [get_ports "DDR4_DQ12"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ12"] ;
set_propertyPACKAGE_PIN AC17      [get_ports "DDR4_DQ13"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ13"] ;
set_propertyPACKAGE_PIN AB14      [get_ports "DDR4_DQ14"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ14"] ;
set_propertyPACKAGE_PIN AD17      [get_ports "DDR4_DQ15"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ15"] ;
set_propertyPACKAGE_PIN AJ16      [get_ports "DDR4_DQ16"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ16"] ;
set_propertyPACKAGE_PIN AJ17      [get_ports "DDR4_DQ17"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ17"] ;
set_propertyPACKAGE_PIN AL15      [get_ports "DDR4_DQ18"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ18"] ;
set_propertyPACKAGE_PIN AK17      [get_ports "DDR4_DQ19"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ19"] ;
set_propertyPACKAGE_PIN AJ15      [get_ports "DDR4_DQ20"] ;
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set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ20"] ;
set_propertyPACKAGE_PIN AK18      [get_ports "DDR4_DQ21"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ21"] ;
set_propertyPACKAGE_PIN AL16      [get_ports "DDR4_DQ22"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ22"] ;
set_propertyPACKAGE_PIN AL18      [get_ports "DDR4_DQ23"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ23"] ;
set_propertyPACKAGE_PIN AP13      [get_ports "DDR4_DQ24"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ24"] ;
set_propertyPACKAGE_PIN AP16      [get_ports "DDR4_DQ25"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ25"] ;
set_propertyPACKAGE_PIN AP15      [get_ports "DDR4_DQ26"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ26"] ;
set_propertyPACKAGE_PIN AN16      [get_ports "DDR4_DQ27"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ27"] ;
set_propertyPACKAGE_PIN AN13      [get_ports "DDR4_DQ28"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ28"] ;
set_propertyPACKAGE_PIN AM18      [get_ports "DDR4_DQ29"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ29"] ;
set_propertyPACKAGE_PIN AN17      [get_ports "DDR4_DQ30"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ30"] ;
set_propertyPACKAGE_PIN AN18      [get_ports "DDR4_DQ31"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ31"] ;
set_propertyPACKAGE_PIN AB19      [get_ports "DDR4_DQ32"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ32"] ;
set_propertyPACKAGE_PIN AD19      [get_ports "DDR4_DQ33"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ33"] ;
set_propertyPACKAGE_PIN AC18      [get_ports "DDR4_DQ34"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ34"] ;
set_propertyPACKAGE_PIN AC19      [get_ports "DDR4_DQ35"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ35"] ;
set_propertyPACKAGE_PIN AA20      [get_ports "DDR4_DQ36"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ36"] ;
set_propertyPACKAGE_PIN AE20      [get_ports "DDR4_DQ37"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ37"] ;
set_propertyPACKAGE_PIN AA19      [get_ports "DDR4_DQ38"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ38"] ;
set_propertyPACKAGE_PIN AD20      [get_ports "DDR4_DQ39"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ39"] ;
set_propertyPACKAGE_PIN AF22      [get_ports "DDR4_DQ40"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ40"] ;
set_propertyPACKAGE_PIN AH21      [get_ports "DDR4_DQ41"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ41"] ;
set_propertyPACKAGE_PIN AG19      [get_ports "DDR4_DQ42"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ42"] ;
set_propertyPACKAGE_PIN AG21      [get_ports "DDR4_DQ43"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ43"] ;
set_propertyPACKAGE_PIN AE24      [get_ports "DDR4_DQ44"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ44"] ;
set_propertyPACKAGE_PIN AG20      [get_ports "DDR4_DQ45"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ45"] ;
set_propertyPACKAGE_PIN AE23      [get_ports "DDR4_DQ46"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ46"] ;
set_propertyPACKAGE_PIN AF21      [get_ports "DDR4_DQ47"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ47"] ;
set_propertyPACKAGE_PIN AL22      [get_ports "DDR4_DQ48"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ48"] ;
set_propertyPACKAGE_PIN AJ22      [get_ports "DDR4_DQ49"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ49"] ;
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set_propertyPACKAGE_PIN AL23      [get_ports "DDR4_DQ50"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ50"] ;
set_propertyPACKAGE_PIN AJ21      [get_ports "DDR4_DQ51"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ51"] ;
set_propertyPACKAGE_PIN AK20      [get_ports "DDR4_DQ52"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ52"] ;
set_propertyPACKAGE_PIN AJ19      [get_ports "DDR4_DQ53"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ53"] ;
set_propertyPACKAGE_PIN AK19      [get_ports "DDR4_DQ54"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ54"] ;
set_propertyPACKAGE_PIN AJ20      [get_ports "DDR4_DQ55"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ55"] ;
set_propertyPACKAGE_PIN AP22      [get_ports "DDR4_DQ56"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ56"] ;
set_propertyPACKAGE_PIN AN22      [get_ports "DDR4_DQ57"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ57"] ;
set_propertyPACKAGE_PIN AP21      [get_ports "DDR4_DQ58"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ58"] ;
set_propertyPACKAGE_PIN AP23      [get_ports "DDR4_DQ59"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ59"] ;
set_propertyPACKAGE_PIN AM19      [get_ports "DDR4_DQ60"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ60"] ;
set_propertyPACKAGE_PIN AM23      [get_ports "DDR4_DQ61"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ61"] ;
set_propertyPACKAGE_PIN AN19      [get_ports "DDR4_DQ62"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ62"] ;
set_propertyPACKAGE_PIN AN23      [get_ports "DDR4_DQ63"] ;
set_propertyIOSTANDARD POD12_DCI [get_ports "DDR4_DQ63"] ;
set_propertyPACKAGE_PIN AJ14      [get_ports "DDR4_DQS0_C"] ;
set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_DQS0_C"] ;
set_propertyPACKAGE_PIN AH14      [get_ports "DDR4_DQS0_T"] ;
set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_DQS0_T"] ;
set_propertyPACKAGE_PIN AA15      [get_ports "DDR4_DQS1_C"] ;
set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_DQS1_C"] ;
set_propertyPACKAGE_PIN AA16      [get_ports "DDR4_DQS1_T"] ;
set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_DQS1_T"] ;
set_propertyPACKAGE_PIN AK14      [get_ports "DDR4_DQS2_C"] ;
set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_DQS2_C"] ;
set_propertyPACKAGE_PIN AK15      [get_ports "DDR4_DQS2_T"] ;
set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_DQS2_T"] ;
set_propertyPACKAGE_PIN AN14      [get_ports "DDR4_DQS3_C"] ;
set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_DQS3_C"] ;
set_propertyPACKAGE_PIN AM14      [get_ports "DDR4_DQS3_T"] ;
set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_DQS3_T"] ;
set_propertyPACKAGE_PIN AB18      [get_ports "DDR4_DQS4_C"] ;
set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_DQS4_C"] ;
set_propertyPACKAGE_PIN AA18      [get_ports "DDR4_DQS4_T"] ;
set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_DQS4_T"] ;
set_propertyPACKAGE_PIN AG23      [get_ports "DDR4_DQS5_C"] ;
set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_DQS5_C"] ;
set_propertyPACKAGE_PIN AF23      [get_ports "DDR4_DQS5_T"] ;
set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_DQS5_T"] ;
set_propertyPACKAGE_PIN AK23      [get_ports "DDR4_DQS6_C"] ;
set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_DQS6_C"] ;
set_propertyPACKAGE_PIN AK22      [get_ports "DDR4_DQS6_T"] ;
set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_DQS6_T"] ;
set_propertyPACKAGE_PIN AN21      [get_ports "DDR4_DQS7_C"] ;
set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_DQS7_C"] ;
set_propertyPACKAGE_PIN AM21      [get_ports "DDR4_DQS7_T"] ;
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set_propertyIOSTANDARD DIFF_POD12[get_ports "DDR4_DQS7_T"] ;

#QSPI
#QSPI_LWR U119 and UPR U120 are connected to PS MIO Bank 500
#Other net PACKAGE_PIN A24 - MIO0_QSPI_LWR_CLK  Bank 500 - PS_MIO0
#Other net PACKAGE_PIN C24 - MIO1_QSPI_LWR_DQ1  Bank 500 - PS_MIO1
#Other net PACKAGE_PIN B24 - MIO2_QSPI_LWR_DQ2  Bank 500 - PS_MIO2
#Other net PACKAGE_PIN E25 - MIO3_QSPI_LWR_DQ3  Bank 500 - PS_MIO3
#Other net PACKAGE_PIN A25 - MIO4_QSPI_LWR_DQ0  Bank 500 - PS_MIO4
#Other net PACKAGE_PIN D25 - MIO5_QSPI_LWR_CS_B Bank 500 - PS_MIO5
#Other net PACKAGE_PIN B25 - MIO7_QSPI_UPR_CS_B Bank 500 - PS_MIO7
#Other net PACKAGE_PIN D26 - MIO8_QSPI_UPR_DQ0  Bank 500 - PS_MIO8
#Other net PACKAGE_PIN C26 - MIO9_QSPI_UPR_DQ1  Bank 500 - PS_MIO9
#Other net PACKAGE_PIN F26 - MIO10_QSPI_UPR_DQ2 Bank 500 - PS_MIO10
#Other net PACKAGE_PIN B26 - MIO11_QSPI_UPR_DQ3 Bank 500 - PS_MIO11
#Other net PACKAGE_PIN C27 - MIO12_QSPI_UPR_CLK Bank 500 - PS_MIO12

#FMC
#HPC0 J5
set_propertyPACKAGE_PIN E14   [get_ports "FMC_HPC0_CLK0_M2C_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_CLK0_M2C_N"] ;
set_propertyPACKAGE_PIN E15   [get_ports "FMC_HPC0_CLK0_M2C_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_CLK0_M2C_P"] ;
set_propertyPACKAGE_PIN F10   [get_ports "FMC_HPC0_CLK1_M2C_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_CLK1_M2C_N"] ;
set_propertyPACKAGE_PIN G10   [get_ports "FMC_HPC0_CLK1_M2C_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_CLK1_M2C_P"] ;
set_propertyPACKAGE_PIN V7    [get_ports "FMC_HPC0_GBTCLK0_M2C_C_N"] ;
set_propertyPACKAGE_PIN V8    [get_ports "FMC_HPC0_GBTCLK0_M2C_C_P"] ;
set_propertyPACKAGE_PIN T7    [get_ports "FMC_HPC0_GBTCLK1_M2C_C_N"] ;
set_propertyPACKAGE_PIN T8    [get_ports "FMC_HPC0_GBTCLK1_M2C_C_P"] ;
set_propertyPACKAGE_PIN R5    [get_ports "FMC_HPC0_DP0_C2M_N"] ;
set_propertyPACKAGE_PIN R6    [get_ports "FMC_HPC0_DP0_C2M_P"] ;
set_propertyPACKAGE_PIN R1    [get_ports "FMC_HPC0_DP0_M2C_N"] ;
set_propertyPACKAGE_PIN R2    [get_ports "FMC_HPC0_DP0_M2C_P"] ;
set_propertyPACKAGE_PIN T3    [get_ports "FMC_HPC0_DP1_C2M_N"] ;
set_propertyPACKAGE_PIN T4    [get_ports "FMC_HPC0_DP1_C2M_P"] ;
set_propertyPACKAGE_PIN U1    [get_ports "FMC_HPC0_DP1_M2C_N"] ;
set_propertyPACKAGE_PIN U2    [get_ports "FMC_HPC0_DP1_M2C_P"] ;
set_propertyPACKAGE_PIN N5    [get_ports "FMC_HPC0_DP2_C2M_N"] ;
set_propertyPACKAGE_PIN N6    [get_ports "FMC_HPC0_DP2_C2M_P"] ;
set_propertyPACKAGE_PIN P3    [get_ports "FMC_HPC0_DP2_M2C_N"] ;
set_propertyPACKAGE_PIN P4    [get_ports "FMC_HPC0_DP2_M2C_P"] ;
set_propertyPACKAGE_PIN U5    [get_ports "FMC_HPC0_DP3_C2M_N"] ;
set_propertyPACKAGE_PIN U6    [get_ports "FMC_HPC0_DP3_C2M_P"] ;
set_propertyPACKAGE_PIN V3    [get_ports "FMC_HPC0_DP3_M2C_N"] ;
set_propertyPACKAGE_PIN V4    [get_ports "FMC_HPC0_DP3_M2C_P"] ;
set_propertyPACKAGE_PIN H3    [get_ports "FMC_HPC0_DP4_C2M_N"] ;
set_propertyPACKAGE_PIN H4    [get_ports "FMC_HPC0_DP4_C2M_P"] ;
set_propertyPACKAGE_PIN G1    [get_ports "FMC_HPC0_DP4_M2C_N"] ;
set_propertyPACKAGE_PIN G2    [get_ports "FMC_HPC0_DP4_M2C_P"] ;
set_propertyPACKAGE_PIN L5    [get_ports "FMC_HPC0_DP5_C2M_N"] ;
set_propertyPACKAGE_PIN L6    [get_ports "FMC_HPC0_DP5_C2M_P"] ;
set_propertyPACKAGE_PIN L1    [get_ports "FMC_HPC0_DP5_M2C_N"] ;
set_propertyPACKAGE_PIN L2    [get_ports "FMC_HPC0_DP5_M2C_P"] ;
set_propertyPACKAGE_PIN M3    [get_ports "FMC_HPC0_DP6_C2M_N"] ;
set_propertyPACKAGE_PIN M4    [get_ports "FMC_HPC0_DP6_C2M_P"] ;
set_propertyPACKAGE_PIN N1    [get_ports "FMC_HPC0_DP6_M2C_N"] ;
set_propertyPACKAGE_PIN N2    [get_ports "FMC_HPC0_DP6_M2C_P"] ;
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set_propertyPACKAGE_PIN K3    [get_ports "FMC_HPC0_DP7_C2M_N"] ;
set_propertyPACKAGE_PIN K4    [get_ports "FMC_HPC0_DP7_C2M_P"] ;
set_propertyPACKAGE_PIN J1    [get_ports "FMC_HPC0_DP7_M2C_N"] ;
set_propertyPACKAGE_PIN J2    [get_ports "FMC_HPC0_DP7_M2C_P"] ;
set_propertyPACKAGE_PIN F16   [get_ports "FMC_HPC0_LA00_CC_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA00_CC_N"] ;
set_propertyPACKAGE_PIN F17   [get_ports "FMC_HPC0_LA00_CC_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA00_CC_P"] ;
set_propertyPACKAGE_PIN H17   [get_ports "FMC_HPC0_LA01_CC_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA01_CC_N"] ;
set_propertyPACKAGE_PIN H18   [get_ports "FMC_HPC0_LA01_CC_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA01_CC_P"] ;
set_propertyPACKAGE_PIN K20   [get_ports "FMC_HPC0_LA02_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA02_N"] ;
set_propertyPACKAGE_PIN L20   [get_ports "FMC_HPC0_LA02_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA02_P"] ;
set_propertyPACKAGE_PIN K18   [get_ports "FMC_HPC0_LA03_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA03_N"] ;
set_propertyPACKAGE_PIN K19   [get_ports "FMC_HPC0_LA03_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA03_P"] ;
set_propertyPACKAGE_PIN L16   [get_ports "FMC_HPC0_LA04_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA04_N"] ;
set_propertyPACKAGE_PIN L17   [get_ports "FMC_HPC0_LA04_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA04_P"] ;
set_propertyPACKAGE_PIN J17   [get_ports "FMC_HPC0_LA05_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA05_N"] ;
set_propertyPACKAGE_PIN K17   [get_ports "FMC_HPC0_LA05_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA05_P"] ;
set_propertyPACKAGE_PIN G19   [get_ports "FMC_HPC0_LA06_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA06_N"] ;
set_propertyPACKAGE_PIN H19   [get_ports "FMC_HPC0_LA06_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA06_P"] ;
set_propertyPACKAGE_PIN J15   [get_ports "FMC_HPC0_LA07_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA07_N"] ;
set_propertyPACKAGE_PIN J16   [get_ports "FMC_HPC0_LA07_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA07_P"] ;
set_propertyPACKAGE_PIN E17   [get_ports "FMC_HPC0_LA08_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA08_N"] ;
set_propertyPACKAGE_PIN E18   [get_ports "FMC_HPC0_LA08_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA08_P"] ;
set_propertyPACKAGE_PIN G16   [get_ports "FMC_HPC0_LA09_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA09_N"] ;
set_propertyPACKAGE_PIN H16   [get_ports "FMC_HPC0_LA09_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA09_P"] ;
set_propertyPACKAGE_PIN K15   [get_ports "FMC_HPC0_LA10_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA10_N"] ;
set_propertyPACKAGE_PIN L15   [get_ports "FMC_HPC0_LA10_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA10_P"] ;
set_propertyPACKAGE_PIN A12   [get_ports "FMC_HPC0_LA11_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA11_N"] ;
set_propertyPACKAGE_PIN A13   [get_ports "FMC_HPC0_LA11_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA11_P"] ;
set_propertyPACKAGE_PIN F18   [get_ports "FMC_HPC0_LA12_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA12_N"] ;
set_propertyPACKAGE_PIN G18   [get_ports "FMC_HPC0_LA12_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA12_P"] ;
set_propertyPACKAGE_PIN F15   [get_ports "FMC_HPC0_LA13_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA13_N"] ;
set_propertyPACKAGE_PIN G15   [get_ports "FMC_HPC0_LA13_P"] ;
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set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA13_P"] ;
set_propertyPACKAGE_PIN C12   [get_ports "FMC_HPC0_LA14_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA14_N"] ;
set_propertyPACKAGE_PIN C13   [get_ports "FMC_HPC0_LA14_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA14_P"] ;
set_propertyPACKAGE_PIN C16   [get_ports "FMC_HPC0_LA15_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA15_N"] ;
set_propertyPACKAGE_PIN D16   [get_ports "FMC_HPC0_LA15_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA15_P"] ;
set_propertyPACKAGE_PIN C17   [get_ports "FMC_HPC0_LA16_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA16_N"] ;
set_propertyPACKAGE_PIN D17   [get_ports "FMC_HPC0_LA16_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA16_P"] ;
set_propertyPACKAGE_PIN E10   [get_ports "FMC_HPC0_LA17_CC_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA17_CC_N"] ;
set_propertyPACKAGE_PIN F11   [get_ports "FMC_HPC0_LA17_CC_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA17_CC_P"] ;
set_propertyPACKAGE_PIN D10   [get_ports "FMC_HPC0_LA18_CC_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA18_CC_N"] ;
set_propertyPACKAGE_PIN D11   [get_ports "FMC_HPC0_LA18_CC_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA18_CC_P"] ;
set_propertyPACKAGE_PIN C11   [get_ports "FMC_HPC0_LA19_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA19_N"] ;
set_propertyPACKAGE_PIN D12   [get_ports "FMC_HPC0_LA19_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA19_P"] ;
set_propertyPACKAGE_PIN E12   [get_ports "FMC_HPC0_LA20_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA20_N"] ;
set_propertyPACKAGE_PIN F12   [get_ports "FMC_HPC0_LA20_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA20_P"] ;
set_propertyPACKAGE_PIN A10   [get_ports "FMC_HPC0_LA21_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA21_N"] ;
set_propertyPACKAGE_PIN B10   [get_ports "FMC_HPC0_LA21_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA21_P"] ;
set_propertyPACKAGE_PIN H12   [get_ports "FMC_HPC0_LA22_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA22_N"] ;
set_propertyPACKAGE_PIN H13   [get_ports "FMC_HPC0_LA22_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA22_P"] ;
set_propertyPACKAGE_PIN A11   [get_ports "FMC_HPC0_LA23_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA23_N"] ;
set_propertyPACKAGE_PIN B11   [get_ports "FMC_HPC0_LA23_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA23_P"] ;
set_propertyPACKAGE_PIN A6    [get_ports "FMC_HPC0_LA24_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA24_N"] ;
set_propertyPACKAGE_PIN B6    [get_ports "FMC_HPC0_LA24_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA24_P"] ;
set_propertyPACKAGE_PIN C6    [get_ports "FMC_HPC0_LA25_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA25_N"] ;
set_propertyPACKAGE_PIN C7    [get_ports "FMC_HPC0_LA25_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA25_P"] ;
set_propertyPACKAGE_PIN B8    [get_ports "FMC_HPC0_LA26_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA26_N"] ;
set_propertyPACKAGE_PIN B9    [get_ports "FMC_HPC0_LA26_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA26_P"] ;
set_propertyPACKAGE_PIN A7    [get_ports "FMC_HPC0_LA27_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA27_N"] ;
set_propertyPACKAGE_PIN A8    [get_ports "FMC_HPC0_LA27_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA27_P"] ;
set_propertyPACKAGE_PIN L13   [get_ports "FMC_HPC0_LA28_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA28_N"] ;
```

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set_propertyPACKAGE_PIN M13   [get_ports "FMC_HPC0_LA28_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA28_P"] ;
set_propertyPACKAGE_PIN J10   [get_ports "FMC_HPC0_LA29_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA29_N"] ;
set_propertyPACKAGE_PIN K10   [get_ports "FMC_HPC0_LA29_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA29_P"] ;
set_propertyPACKAGE_PIN D9    [get_ports "FMC_HPC0_LA30_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA30_N"] ;
set_propertyPACKAGE_PIN E9    [get_ports "FMC_HPC0_LA30_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA30_P"] ;
set_propertyPACKAGE_PIN E7    [get_ports "FMC_HPC0_LA31_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA31_N"] ;
set_propertyPACKAGE_PIN F7    [get_ports "FMC_HPC0_LA31_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA31_P"] ;
set_propertyPACKAGE_PIN E8    [get_ports "FMC_HPC0_LA32_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA32_N"] ;
set_propertyPACKAGE_PIN F8    [get_ports "FMC_HPC0_LA32_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA32_P"] ;
set_propertyPACKAGE_PIN C8    [get_ports "FMC_HPC0_LA33_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA33_N"] ;
set_propertyPACKAGE_PIN C9    [get_ports "FMC_HPC0_LA33_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC0_LA33_P"] ;

#HPC1 J4
set_propertyPACKAGE_PIN E23   [get_ports "FMC_HPC1_CLK0_M2C_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_CLK0_M2C_N"] ;
set_propertyPACKAGE_PIN F23   [get_ports "FMC_HPC1_CLK0_M2C_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_CLK0_M2C_P"] ;
set_propertyPACKAGE_PIN AJ5   [get_ports "FMC_HPC1_DP0_C2M_N"] ;
set_propertyPACKAGE_PIN AJ6   [get_ports "FMC_HPC1_DP0_C2M_P"] ;
set_propertyPACKAGE_PIN AK3   [get_ports "FMC_HPC1_DP0_M2C_N"] ;
set_propertyPACKAGE_PIN AK4   [get_ports "FMC_HPC1_DP0_M2C_P"] ;
set_propertyPACKAGE_PIN Y7    [get_ports "FMC_HPC1_GBTCLK0_M2C_C_N"] ;
set_propertyPACKAGE_PIN Y8    [get_ports "FMC_HPC1_GBTCLK0_M2C_C_P"] ;
set_propertyPACKAGE_PIN B19   [get_ports "FMC_HPC1_LA00_CC_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA00_CC_N"] ;
set_propertyPACKAGE_PIN B18   [get_ports "FMC_HPC1_LA00_CC_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA00_CC_P"] ;
set_propertyPACKAGE_PIN D24   [get_ports "FMC_HPC1_LA01_CC_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA01_CC_N"] ;
set_propertyPACKAGE_PIN E24   [get_ports "FMC_HPC1_LA01_CC_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA01_CC_P"] ;
set_propertyPACKAGE_PIN K23   [get_ports "FMC_HPC1_LA02_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA02_N"] ;
set_propertyPACKAGE_PIN K22   [get_ports "FMC_HPC1_LA02_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA02_P"] ;
set_propertyPACKAGE_PIN J22   [get_ports "FMC_HPC1_LA03_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA03_N"] ;
set_propertyPACKAGE_PIN J21   [get_ports "FMC_HPC1_LA03_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA03_P"] ;
set_propertyPACKAGE_PIN H24   [get_ports "FMC_HPC1_LA04_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA04_N"] ;
set_propertyPACKAGE_PIN J24   [get_ports "FMC_HPC1_LA04_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA04_P"] ;
set_propertyPACKAGE_PIN G26   [get_ports "FMC_HPC1_LA05_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA05_N"] ;
set_propertyPACKAGE_PIN G25   [get_ports "FMC_HPC1_LA05_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA05_P"] ;
set_propertyPACKAGE_PIN H22   [get_ports "FMC_HPC1_LA06_N"] ;
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set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA06_N"] ;
set_propertyPACKAGE_PIN H21   [get_ports "FMC_HPC1_LA06_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA06_P"] ;
set_propertyPACKAGE_PIN C23   [get_ports "FMC_HPC1_LA07_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA07_N"] ;
set_propertyPACKAGE_PIN D22   [get_ports "FMC_HPC1_LA07_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA07_P"] ;
set_propertyPACKAGE_PIN H26   [get_ports "FMC_HPC1_LA08_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA08_N"] ;
set_propertyPACKAGE_PIN J25   [get_ports "FMC_HPC1_LA08_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA08_P"] ;
set_propertyPACKAGE_PIN F20   [get_ports "FMC_HPC1_LA09_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA09_N"] ;
set_propertyPACKAGE_PIN G20   [get_ports "FMC_HPC1_LA09_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA09_P"] ;
set_propertyPACKAGE_PIN E22   [get_ports "FMC_HPC1_LA10_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA10_N"] ;
set_propertyPACKAGE_PIN F22   [get_ports "FMC_HPC1_LA10_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA10_P"] ;
set_propertyPACKAGE_PIN A21   [get_ports "FMC_HPC1_LA11_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA11_N"] ;
set_propertyPACKAGE_PIN A20   [get_ports "FMC_HPC1_LA11_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA11_P"] ;
set_propertyPACKAGE_PIN D19   [get_ports "FMC_HPC1_LA12_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA12_N"] ;
set_propertyPACKAGE_PIN E19   [get_ports "FMC_HPC1_LA12_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA12_P"] ;
set_propertyPACKAGE_PIN C22   [get_ports "FMC_HPC1_LA13_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA13_N"] ;
set_propertyPACKAGE_PIN C21   [get_ports "FMC_HPC1_LA13_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA13_P"] ;
set_propertyPACKAGE_PIN D21   [get_ports "FMC_HPC1_LA14_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA14_N"] ;
set_propertyPACKAGE_PIN D20   [get_ports "FMC_HPC1_LA14_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA14_P"] ;
set_propertyPACKAGE_PIN A19   [get_ports "FMC_HPC1_LA15_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA15_N"] ;
set_propertyPACKAGE_PIN A18   [get_ports "FMC_HPC1_LA15_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA15_P"] ;
set_propertyPACKAGE_PIN C19   [get_ports "FMC_HPC1_LA16_N"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA16_N"] ;
set_propertyPACKAGE_PIN C18   [get_ports "FMC_HPC1_LA16_P"] ;
set_propertyIOSTANDARD  LVDS  [get_ports "FMC_HPC1_LA16_P"] ;

#HDMI
set_property PACKAGE_PIN AP3      [get_ports "HDMI_RX0_C_N"] ;
set_property PACKAGE_PIN AP4      [get_ports "HDMI_RX0_C_P"] ;
set_property PACKAGE_PIN AN1      [get_ports "HDMI_RX1_C_N"] ;
set_property PACKAGE_PIN AN2      [get_ports "HDMI_RX1_C_P"] ;
set_property PACKAGE_PIN AL1      [get_ports "HDMI_RX2_C_N"] ;
set_property PACKAGE_PIN AL2      [get_ports "HDMI_RX2_C_P"] ;
set_property PACKAGE_PIN AN5      [get_ports "HDMI_TX0_N"] ;
set_property PACKAGE_PIN AN6      [get_ports "HDMI_TX0_P"] ;
set_property PACKAGE_PIN AM3      [get_ports "HDMI_TX1_N"] ;
set_property PACKAGE_PIN AM4      [get_ports "HDMI_TX1_P"] ;
set_property PACKAGE_PIN AL5      [get_ports "HDMI_TX2_N"] ;
set_property PACKAGE_PIN AL6      [get_ports "HDMI_TX2_P"] ;
set_property PACKAGE_PIN AD7      [get_ports "HDMI_SI5324_OUT_C_N"] ;
set_property PACKAGE_PIN AD8      [get_ports "HDMI_SI5324_OUT_C_P"] ;
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set_property PACKAGE_PIN F13      [get_ports "HDMI_REC_CLOCK_C_N"] ;
set_property IOSTANDARD  LVDS     [get_ports "HDMI_REC_CLOCK_C_N"] ;
set_property PACKAGE_PIN G14      [get_ports "HDMI_REC_CLOCK_C_P"] ;
set_property IOSTANDARD  LVDS     [get_ports "HDMI_REC_CLOCK_C_P"] ;
set_property PACKAGE_PIN F21      [get_ports "HDMI_TX_LVDS_OUT_N"] ;
set_property IOSTANDARD  LVDS     [get_ports "HDMI_TX_LVDS_OUT_N"] ;
set_property PACKAGE_PIN G21      [get_ports "HDMI_TX_LVDS_OUT_P"] ;
set_property IOSTANDARD  LVDS     [get_ports "HDMI_TX_LVDS_OUT_P"] ;
set_property PACKAGE_PIN AC9      [get_ports "HDMI_RX_CLK_C_N"] ;
set_property PACKAGE_PIN AC10     [get_ports "HDMI_RX_CLK_C_P"] ;
set_property PACKAGE_PIN M8       [get_ports "HDMI_RX_PWR_DET"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "HDMI_RX_PWR_DET"] ;
set_property PACKAGE_PIN M10      [get_ports "HDMI_RX_HPD"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "HDMI_RX_HPD"] ;
set_property PACKAGE_PIN M9       [get_ports "HDMI_RX_SNK_SCL"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "HDMI_RX_SNK_SCL"] ;
set_property PACKAGE_PIN M11      [get_ports "HDMI_RX_SNK_SDA"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "HDMI_RX_SNK_SDA"] ;
set_property PACKAGE_PIN N11      [get_ports "HDMI_TX_EN"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "HDMI_TX_EN"] ;
set_property PACKAGE_PIN M12      [get_ports "HDMI_TX_CEC"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "HDMI_TX_CEC"] ;
set_property PACKAGE_PIN N13      [get_ports "HDMI_TX_HPD"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "HDMI_TX_HPD"] ;
set_property PACKAGE_PIN N8       [get_ports "HDMI_TX_SRC_SCL"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "HDMI_TX_SRC_SCL"] ;
set_property PACKAGE_PIN N9       [get_ports "HDMI_TX_SRC_SDA"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "HDMI_TX_SRC_SDA"] ;
set_property PACKAGE_PIN N12      [get_ports "HDMI_CTL_SCL"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "HDMI_CTL_SCL"] ;
set_property PACKAGE_PIN P12      [get_ports "HDMI_CTL_SDA"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "HDMI_CTL_SDA"] ;
set_property PACKAGE_PIN G8       [get_ports "HDMI_SI5324_LOL"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "HDMI_SI5324_LOL"] ;
set_property PACKAGE_PIN H8       [get_ports "HDMI_SI5324_RST"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "HDMI_SI5324_RST"] ;

#HDMI CLOCK RECOVERY
set_property PACKAGE_PIN F13      [get_ports "HDMI_REC_CLOCK_C_N"] ;
set_property IOSTANDARD  LVDS     [get_ports "HDMI_REC_CLOCK_C_N"] ;
set_property PACKAGE_PIN G14      [get_ports "HDMI_REC_CLOCK_C_P"] ;
set_property IOSTANDARD  LVDS     [get_ports "HDMI_REC_CLOCK_C_P"] ;

#ARM TRACE
set_property PACKAGE_PIN H6       [get_ports "TRACEDATA0"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDATA0"] ;
set_property PACKAGE_PIN G6       [get_ports "TRACEDATA1"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDATA1"] ;
set_property PACKAGE_PIN H7       [get_ports "TRACEDATA2"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDATA2"] ;
set_property PACKAGE_PIN E1       [get_ports "TRACEDATA3"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDATA3"] ;
set_property PACKAGE_PIN D1       [get_ports "TRACEDATA4"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDATA4"] ;
set_property PACKAGE_PIN C1       [get_ports "TRACEDATA5"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDATA5"] ;
set_property PACKAGE_PIN B1       [get_ports "TRACEDATA6"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDATA6"] ;
set_property PACKAGE_PIN A3       [get_ports "TRACEDATA7"] ;
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set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDATA7"] ;
set_property PACKAGE_PIN D2       [get_ports "TRACEDATA8"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDATA8"] ;
set_property PACKAGE_PIN C2       [get_ports "TRACEDATA9"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDATA9"] ;
set_property PACKAGE_PIN C3       [get_ports "TRACEDATA10"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDATA10"] ;
set_property PACKAGE_PIN B3       [get_ports "TRACEDATA11"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDATA11"] ;
set_property PACKAGE_PIN C4       [get_ports "TRACEDATA12"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDATA12"] ;
set_property PACKAGE_PIN B4       [get_ports "TRACEDATA13"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDATA13"] ;
set_property PACKAGE_PIN E4       [get_ports "TRACEDATA14"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDATA14"] ;
set_property PACKAGE_PIN D4       [get_ports "TRACEDATA15"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDATA15"] ;
set_property PACKAGE_PIN E5       [get_ports "TRACEDBGRQ"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDBGRQ"] ;
set_property PACKAGE_PIN F6       [get_ports "TRACESRST_B"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACESRST_B"] ;
set_property PACKAGE_PIN D5       [get_ports "TRACETDO"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACETDO"] ;
set_property PACKAGE_PIN D6       [get_ports "TRACERTCK"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACERTCK"] ;
set_property PACKAGE_PIN A5       [get_ports "TRACETCK"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACETCK"] ;
set_property PACKAGE_PIN B5       [get_ports "TRACETMS"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACETMS"] ;
set_property PACKAGE_PIN F4       [get_ports "TRACETDI"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACETDI"] ;
set_property PACKAGE_PIN F5       [get_ports "TRACETRST_B"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACETRST_B"] ;
set_property PACKAGE_PIN E2       [get_ports "TRACECLKA"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACECLKA"] ;
set_property PACKAGE_PIN E3       [get_ports "TRACEDBGACK"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEDBGACK"] ;
set_property PACKAGE_PIN A2       [get_ports "TRACEEXTTRIG"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACEEXTTRIG"] ;
set_property PACKAGE_PIN K8       [get_ports "TRACECTL"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "TRACECTL"] ;

#GPIO
#PUSHBUTTON SWITCHES
set_property PACKAGE_PIN AG13     [get_ports "GPIO_SW_N"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "GPIO_SW_N"] ;
set_property PACKAGE_PIN AP20     [get_ports "GPIO_SW_S"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "GPIO_SW_S"] ;
set_property PACKAGE_PIN AC14     [get_ports "GPIO_SW_E"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "GPIO_SW_E"] ;
set_property PACKAGE_PIN AK12     [get_ports "GPIO_SW_W"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "GPIO_SW_W"] ;
set_property PACKAGE_PIN AL10     [get_ports "GPIO_SW_C"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "GPIO_SW_C"] ;

#CPU_RESET PUSHBUTTON
set_property PACKAGE_PIN G13      [get_ports "CPU_RESET"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "CPU_RESET"] ;
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```
#GPIO 8-POLE DIP SW
set_property PACKAGE_PIN A17      [get_ports "GPIO_DIP_SW0"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "GPIO_DIP_SW0"] ;
set_property PACKAGE_PIN A16      [get_ports "GPIO_DIP_SW1"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "GPIO_DIP_SW1"] ;
set_property PACKAGE_PIN B16      [get_ports "GPIO_DIP_SW2"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "GPIO_DIP_SW2"] ;
set_property PACKAGE_PIN B15      [get_ports "GPIO_DIP_SW3"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "GPIO_DIP_SW3"] ;
set_property PACKAGE_PIN A15      [get_ports "GPIO_DIP_SW4"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "GPIO_DIP_SW4"] ;
set_property PACKAGE_PIN A14      [get_ports "GPIO_DIP_SW5"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "GPIO_DIP_SW5"] ;
set_property PACKAGE_PIN B14      [get_ports "GPIO_DIP_SW6"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "GPIO_DIP_SW6"] ;
set_property PACKAGE_PIN B13      [get_ports "GPIO_DIP_SW7"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "GPIO_DIP_SW7"] ;

#GPIO LEDs
set_property PACKAGE_PIN AL11     [get_ports "GPIO_LED_0_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "GPIO_LED_0_LS"] ;
set_property PACKAGE_PIN AL13     [get_ports "GPIO_LED_1_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "GPIO_LED_1_LS"] ;
set_property PACKAGE_PIN AK13     [get_ports "GPIO_LED_2_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "GPIO_LED_2_LS"] ;
set_property PACKAGE_PIN AE15     [get_ports "GPIO_LED_3_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "GPIO_LED_3_LS"] ;
set_property PACKAGE_PIN AM8      [get_ports "GPIO_LED_4_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "GPIO_LED_4_LS"] ;
set_property PACKAGE_PIN AM9      [get_ports "GPIO_LED_5_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "GPIO_LED_5_LS"] ;
set_property PACKAGE_PIN AM10     [get_ports "GPIO_LED_6_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "GPIO_LED_6_LS"] ;
set_property PACKAGE_PIN AM11     [get_ports "GPIO_LED_7_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "GPIO_LED_7_LS"] ;

#PMOD
#PMOD0 RT. ANGLE RECEPTACLE 2X6
set_property PACKAGE_PIN B23      [get_ports "PMOD0_0_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "PMOD0_0_LS"] ;
set_property PACKAGE_PIN A23      [get_ports "PMOD0_1_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "PMOD0_1_LS"] ;
set_property PACKAGE_PIN F25      [get_ports "PMOD0_2_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "PMOD0_2_LS"] ;
set_property PACKAGE_PIN E20      [get_ports "PMOD0_3_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "PMOD0_3_LS"] ;
set_property PACKAGE_PIN K24      [get_ports "PMOD0_4_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "PMOD0_4_LS"] ;
set_property PACKAGE_PIN L23      [get_ports "PMOD0_5_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "PMOD0_5_LS"] ;
set_property PACKAGE_PIN L22      [get_ports "PMOD0_6_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "PMOD0_6_LS"] ;
set_property PACKAGE_PIN D7       [get_ports "PMOD0_7_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "PMOD0_7_LS"] ;

#PMOD1 MALE PIN HEADER 2X6
set_property PACKAGE_PIN AN8      [get_ports "PMOD1_0_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "PMOD1_0_LS"] ;
set_property PACKAGE_PIN AN9      [get_ports "PMOD1_1_LS"] ;
```

```
set_property IOSTANDARD  LVCMOS12 [get_ports "PMOD1_1_LS"] ;
set_property PACKAGE_PIN AP11     [get_ports "PMOD1_2_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "PMOD1_2_LS"] ;
set_property PACKAGE_PIN AN11     [get_ports "PMOD1_3_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "PMOD1_3_LS"] ;
set_property PACKAGE_PIN AP9      [get_ports "PMOD1_4_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "PMOD1_4_LS"] ;
set_property PACKAGE_PIN AP10     [get_ports "PMOD1_5_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "PMOD1_5_LS"] ;
set_property PACKAGE_PIN AP12     [get_ports "PMOD1_6_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "PMOD1_6_LS"] ;
set_property PACKAGE_PIN AN12     [get_ports "PMOD1_7_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "PMOD1_7_LS"] ;

#PROTOTYPE MALE PIN HEADER 2X12
set_property PACKAGE_PIN K13      [get_ports "L6N_AD6N_64_N"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "L6N_AD6N_64_N"] ;
set_property PACKAGE_PIN L14      [get_ports "L6P_AD6P_64_P"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "L6P_AD6P_64_P"] ;
set_property PACKAGE_PIN J14      [get_ports "L5N_AD14N_64_N"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "L5N_AD14N_64_N"] ;
set_property PACKAGE_PIN K14      [get_ports "L5P_AD14P_64_P"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "L5P_AD14P_64_P"] ;
set_property PACKAGE_PIN J11      [get_ports "L4N_AD7N_64_N"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "L4N_AD7N_64_N"] ;
set_property PACKAGE_PIN K12      [get_ports "L4P_AD7P_64_P"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "L4P_AD7P_64_P"] ;
set_property PACKAGE_PIN L11      [get_ports "L3N_AD15N_64_N"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "L3N_AD15N_64_N"] ;
set_property PACKAGE_PIN L12      [get_ports "L3P_AD15P_64_P"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "L3P_AD15P_64_P"] ;
set_property PACKAGE_PIN G24      [get_ports "L14N_HDGC_65_N"] ;
set_property IOSTANDARD  LVDS     [get_ports "L14N_HDGC_65_N"] ;
set_property PACKAGE_PIN G23      [get_ports "L14P_HDGC_65_P"] ;
set_property IOSTANDARD  LVDS     [get_ports "L14P_HDGC_65_P"] ;

#MSP430 SYSTEM CONTROLLER
set_property PACKAGE_PIN J6       [get_ports "MSP430_GPIO_PL_0"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "MSP430_GPIO_PL_0"] ;
set_property PACKAGE_PIN J7       [get_ports "MSP430_GPIO_PL_1"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "MSP430_GPIO_PL_1"] ;
set_property PACKAGE_PIN J9       [get_ports "MSP430_GPIO_PL_2"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "MSP430_GPIO_PL_2"] ;
set_property PACKAGE_PIN K9       [get_ports "MSP430_GPIO_PL_3"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "MSP430_GPIO_PL_3"] ;
set_property PACKAGE_PIN AA17     [get_ports "MSP430_UCA1_TXD_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "MSP430_UCA1_TXD_LS"] ;
set_property PACKAGE_PIN AH16     [get_ports "MSP430_UCA1_RXD_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "MSP430_UCA1_RXD_LS"] ;

#SFP
#SFP0
set_property PACKAGE_PIN AE22     [get_ports "SFP0_TX_DISABLE"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "SFP0_TX_DISABLE"] ;
set_property PACKAGE_PIN AA1      [get_ports "SFP0_RX_N"] ;
set_property PACKAGE_PIN AA2      [get_ports "SFP0_RX_P"] ;
set_property PACKAGE_PIN Y3       [get_ports "SFP0_TX_N"] ;
set_property PACKAGE_PIN Y4       [get_ports "SFP0_TX_P"] ;
set_property PACKAGE_PIN AE22     [get_ports "SFP0_TX_DISABLE"] ;
```

```
set_property IOSTANDARD  LVCMOS12 [get_ports "SFP0_TX_DISABLE"] ;

#SFP1
set_property PACKAGE_PIN AF20     [get_ports "SFP1_TX_DISABLE"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "SFP1_TX_DISABLE"] ;
set_property PACKAGE_PIN W1       [get_ports "SFP1_RX_N"] ;
set_property PACKAGE_PIN W2       [get_ports "SFP1_RX_P"] ;
set_property PACKAGE_PIN W5       [get_ports "SFP1_TX_N"] ;
set_property PACKAGE_PIN W6       [get_ports "SFP1_TX_P"] ;
set_property PACKAGE_PIN AF20     [get_ports "SFP1_TX_DISABLE"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "SFP1_TX_DISABLE"] ;

#SFP COMMON
set_property PACKAGE_PIN W9       [get_ports "SFP_SI5328_OUT_C_N"] ;
set_property PACKAGE_PIN W10      [get_ports "SFP_SI5328_OUT_C_P"] ;

#SPF CLOCK RECOVERY
set_property PACKAGE_PIN G11      [get_ports "SFP_REC_CLOCK_C_N"] ;
set_property IOSTANDARD  LVDS     [get_ports "SFP_REC_CLOCK_C_N"] ;
set_property PACKAGE_PIN H11      [get_ports "SFP_REC_CLOCK_C_P"] ;
set_property IOSTANDARD  LVDS     [get_ports "SFP_REC_CLOCK_C_P"] ;

#I2C BUS
#I2C0
set_property PACKAGE_PIN AE19     [get_ports "PL_I2C0_SCL_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "PL_I2C0_SCL_LS"] ;
set_property PACKAGE_PIN AH23     [get_ports "PL_I2C0_SDA_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "PL_I2C0_SDA_LS"] ;

#I2C1
set_property PACKAGE_PIN AL21     [get_ports "PL_I2C1_SDA_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "PL_I2C1_SDA_LS"] ;
set_property PACKAGE_PIN AH19     [get_ports "PL_I2C1_SCL_LS"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "PL_I2C1_SCL_LS"] ;

#SYSMON I2C
set_property PACKAGE_PIN B20      [get_ports "SYSMON_SDA_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "SYSMON_SDA_LS"] ;
set_property PACKAGE_PIN A22      [get_ports "SYSMON_SCL_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "SYSMON_SCL_LS"] ;

#MIO DISPLAY PORT
#Other net   PACKAGE_PIN A30 - MIO27_DP_AUX_OUT Bank 501 - PS_MIO27
#Other net   PACKAGE_PIN A31 - MIO28_DP_HPD     Bank 501 - PS_MIO28
#Other net   PACKAGE_PIN A32 - MIO29_DP_OE      Bank 501 - PS_MIO29
#Other net   PACKAGE_PIN A33 - MIO30_DP_AUX_IN  Bank 501 - PS_MIO30

#USER MGT I/O
set_property PACKAGE_PIN AB3      [get_ports "SMA_MGT_RX_C_N"] ;
set_property PACKAGE_PIN AB4      [get_ports "SMA_MGT_RX_C_P"] ;
set_property PACKAGE_PIN AA5      [get_ports "SMA_MGT_TX_N"] ;
set_property PACKAGE_PIN AA6      [get_ports "SMA_MGT_TX_P"] ;
#USER MGT CLOCK
set_property PACKAGE_PIN AA9      [get_ports "USER_SMA_MGT_CLOCK_C_N"] ;
set_property PACKAGE_PIN AA10     [get_ports "USER_SMA_MGT_CLOCK_C_P"] ;
set_property PACKAGE_PIN U9       [get_ports "USER_MGT_SI570_CLOCK1_C_N"] ;
set_property PACKAGE_PIN U10      [get_ports "USER_MGT_SI570_CLOCK1_C_P"] ;
set_property PACKAGE_PIN R9       [get_ports "USER_MGT_SI570_CLOCK2_C_N"] ;
set_property PACKAGE_PIN R10      [get_ports "USER_MGT_SI570_CLOCK2_C_P"] ;
```

```
#UART
set_property PACKAGE_PIN AH17     [get_ports "UART2_TXD_O_FPGA_RXD"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "UART2_TXD_O_FPGA_RXD"] ;
set_property PACKAGE_PIN AM15     [get_ports "UART2_RTS_O_B"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "UART2_RTS_O_B"] ;
set_property PACKAGE_PIN AL17     [get_ports "UART2_RXD_I_FPGA_TXD"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "UART2_RXD_I_FPGA_TXD"] ;
set_property PACKAGE_PIN AP17     [get_ports "UART2_CTS_I_B"] ;
set_property IOSTANDARD  LVCMOS12 [get_ports "UART2_CTS_I_B"] ;

#SDI VIDEO
set_property PACKAGE_PIN B21      [get_ports "SDI_SCLK_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "SDI_SCLK_LS"] ;
set_property PACKAGE_PIN H23      [get_ports "SDI_MISO_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "SDI_MISO_LS"] ;
set_property PACKAGE_PIN L21      [get_ports "SDI_MOSI_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "SDI_MOSI_LS"] ;
set_property PACKAGE_PIN A9       [get_ports "SDI_CS_RCLKR_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "SDI_CS_RCLKR_LS"] ;
set_property PACKAGE_PIN J20      [get_ports "SDI_CS_RCVR_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "SDI_CS_RCVR_LS"] ;
set_property PACKAGE_PIN J19      [get_ports "SDI_CS_DRVR_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "SDI_CS_DRVR_LS"] ;
set_property PACKAGE_PIN E13      [get_ports "SDI_XALARM_RX_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "SDI_XALARM_RX_LS"] ;
set_property PACKAGE_PIN C14      [get_ports "SDI_XALARM_TX_LS"] ;
set_property IOSTANDARD  LVCMOS18 [get_ports "SDI_XALARM_TX_LS"] ;
set_property PACKAGE_PIN AC1      [get_ports "SDI_MGT_RX_N"] ;
set_property PACKAGE_PIN AC2      [get_ports "SDI_MGT_RX_P"] ;
set_property PACKAGE_PIN AC5      [get_ports "SDI_MGT_TX_N"] ;
set_property PACKAGE_PIN AC6      [get_ports "SDI_MGT_TX_P"] ;

#AES3 AUDIO
set_property PACKAGE_PIN G7          [get_ports "AES_IN"] ;
set_property IOSTANDARD  LVCMOS33    [get_ports "AES_IN"] ;
set_property PACKAGE_PIN AF13        [get_ports "AES_OUT_N"] ;
set_property IOSTANDARD  DIFF_SSTL12 [get_ports "AES_OUT_N"] ;
set_property PACKAGE_PIN AE13        [get_ports "AES_OUT_P"] ;
set_property IOSTANDARD  DIFF_SSTL12 [get_ports "AES_OUT_P"] ;

#PCIE
set_property PACKAGE_PIN L8       [get_ports "PCIE_PERST_B"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "PCIE_PERST_B"] ;
set_property PACKAGE_PIN L10      [get_ports "PCIE_WAKE_B"] ;
set_property IOSTANDARD  LVCMOS33 [get_ports "PCIE_WAKE_B"] ;

#PS GTR BANK 505
#Other net   PACKAGE_PIN U30 - GT0_DP_TX_N    Bank 505 - PS_MGTRTXN0_505
#Other net   PACKAGE_PIN R30 - GT1_DP_TX_N    Bank 505 - PS_MGTRTXN1_505
#Other net   PACKAGE_PIN U29 - GT0_DP_TX_P    Bank 505 - PS_MGTRTXP0_505
#Other net   PACKAGE_PIN R29 - GT1_DP_TX_P    Bank 505 - PS_MGTRTXP1_505
#Other net   PACKAGE_PIN R34 - GT2_USB0_RX_N  Bank 505 - PS_MGTRRXN2_505
#Other net   PACKAGE_PIN R33 - GT2_USB0_RX_P  Bank 505 - PS_MGTRRXP2_505
#Other net   PACKAGE_PIN P32 - GT2_USB0_TX_N  Bank 505 - PS_MGTRTXN2_505
#Other net   PACKAGE_PIN P31 - GT2_USB0_TX_P  Bank 505 - PS_MGTRTXP2_505
#Other net   PACKAGE_PIN N34 - GT3_SATA1_RX_N Bank 505 - PS_MGTRRXN3_505
#Other net   PACKAGE_PIN N33 - GT3_SATA1_RX_P Bank 505 - PS_MGTRRXP3_505
#Other net   PACKAGE_PIN N30 - GT3_SATA1_TX_N Bank 505 - PS_MGTRTXN3_505
```

```
#Other net   PACKAGE_PIN N29 - GT3_SATA1_TX_P Bank 505 - PS_MGTRTXP3_505
```

Appendix C

Regulatory and Compliance Information

Overview

This product is designed and tested to conform to the European Union directives and standards described in this section.

For Technical Support, open a Support Service Request.

Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Markings

This product complies with Directive 2002/96/EC on waste electrical and electronic equipment (WEEE). The affixed product label indicates that the user must not discard this electrical or electronic product in domestic household waste.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Appendix D

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

The most up to date information related to the ZCU106 board and its documentation is available on the ZCU106 Evaluation Kit website.

These Xilinx documents provide supplemental material useful with this guide:

1. *Zynq UltraScale+ MPSoC Data Sheet: Overview* (DS891)
2. *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085)
3. *UltraScale Architecture PCB Design User Guide* (UG583)
4. *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150)
5. *UltraScale Architecture GTH Transceivers User Guide* (UG576)
6. *UltraScale Architecture Gen3 Integrated Block for PCI Express LogiCORE IP Product Guide* (PG156)
7. *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033)
8. *Tera Term Terminal Emulator Installation Guide* (UG1036)
9. *Vivado Design Suite User Guide: Using Constraints* (UG903)
10. *UltraScale Architecture System Monitor User Guide* (UG580)
11. *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925)
12. *ZCU106 System Controller GUI Tutorial* (XTP433)
13. *ZCU106 Software Install and Board Setup Tutorial* (XTP435)
14. For additional documents associated with Xilinx devices, design tools, intellectual property, boards, and kits see the Xilinx documentation website.

The following websites provide supplemental material useful with this guide:

15. Micron Technology: www.micron.com

    (MT40A256M16GE-075E, MT25QU512ABB8ESF-0SIT data sheets)

16. Standard Microsystems Corporation (SMSC): www.microchip.com

    (USB3320 data sheet)

17. SanDisk Corporation: www.sandisk.com
18. SD Association: www.sdcard.org
19. Silicon Labs: www.silabs.com/Pages/default.aspx

    (SI5341B, Si570, Si5319C, Si53340, CP2108 data sheets)

20. Texas Instruments: www.ti.com/product/DP83867IR

(TI DP83867 data sheet)

21. PCI: https://pcisig.com/specifications
22. Maxim Integrated Circuits: https://www.maximintegrated.com
23. VITA FMC Marketing Alliance: www.vita.com/fmc
24. Digilent: www.digilentinc.com

(Pmod Peripheral Modules)

25. The Xilinx ATX cable part number 2600304 is manufactured by Sourcegate Technologies and is equivalent to the Sourcegate Technologies part number AZCBL-WH-11009.

Sourcegate only manufactures the latest revision, which is currently A4. To order, contact Aries Ang, aries.ang@sourcegate.net, +65 6483 2878 for price and availability. This is a custom cable and cannot be ordered from the Sourcegate website.

26. Future Technology Devices International Ltd.: http://www.ftdichip.com

(FT232HL)

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