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REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Nov. 06. 2012
Rev. 1.1	Typo error on page 9, revised as 8mmx10mm.	Dec.18. 2012
Rev. 1.2	1. Revise I _{SB1} on page 4 & I _{DR} on page 8 2. Revise V _{IH} (max) & V _L (min) note on page 4 V _{IH} (max) = VCC + 2.0V for pulse width less than 6ns. V _L (min) = VSS - 2.0V for pulse width less than 6ns.	June. 10. 2013
Rev 1.3	1. Amended Feature to read ROHS Compliant on page 1 2. Amended Power Dissipation table Standby(I _{SB1} ,TYP.) to read 6μA(SL & SLI) on page 1 3. Inserted missing temperature table for I _{SB1} on page 3 3. Inserted missing temperature table for I _{DR} on page 8 4. Typo error, revised word INTENTIONALLY on page 11	Jan 31, 2014

FEATURE

- Fast access time : 55ns
- Low power consumption:
Operating current : 45mA (TYP.)
Standby current : 6μA (TYP.) SL & SLI-version
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.2V (MIN.)
- **ROHS Compliant**
- Package : 48-ball 8mm x 10mm TFBGA

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I _{SB1} ,TYP.)	Operating(I _{cc} ,TYP.)
AS6C3216(I)	-40 ~ 85°C	2.7 ~ 3.6V	55ns	6μA(SL & SLI)	45/mA

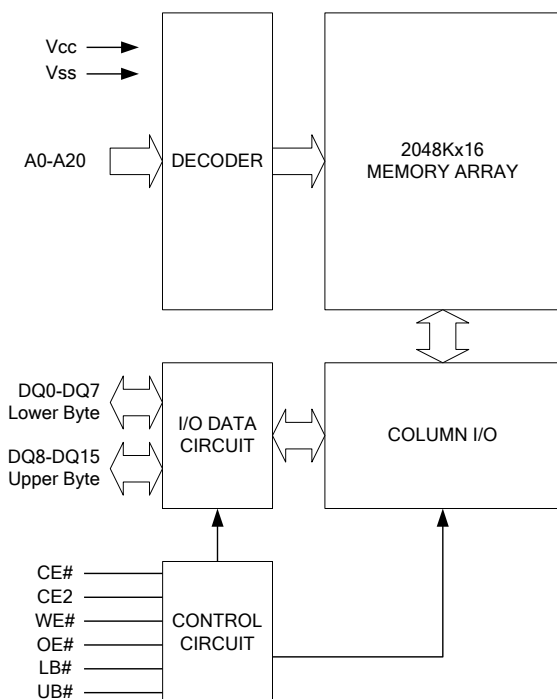
GENERAL DESCRIPTION

The AS6C3216 is a 33,554,432-bit low power CMOS static random access memory organized as 2,097,152 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C3216 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C3216 operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

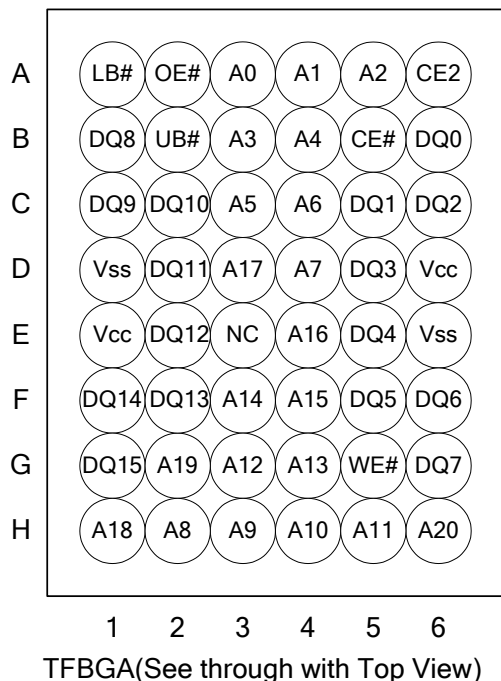
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 – A20	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
Vcc	Power Supply
Vss	Ground

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V _{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to Vss	V _{T2}	-0.5 to Vcc+0.5	V
Operating Temperature	T _A	-40 to 85(I grade)	°C
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
							DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	X	High – Z	High – Z	I_{SB}, I_{SB1}
	X	L	X	X	X	X	High – Z	High – Z	
	X	X	X	X	H	H	High – Z	High – Z	
Output Disable	L	H	H	H	L	X	High – Z	High – Z	I_{CC}, I_{CC1}
	L	H	H	H	X	L	High – Z	High – Z	
Read	L	H	L	H	L	H	D_{OUT}	High – Z	I_{CC}, I_{CC1}
	L	H	L	H	H	L	High – Z	D_{OUT}	
	L	H	L	H	L	L	D_{OUT}	D_{OUT}	
Write	L	H	X	L	L	H	D_{IN}	High – Z	I_{CC}, I_{CC1}
	L	H	X	L	H	L	High – Z	D_{IN}	
	L	H	X	L	L	L	D_{IN}	D_{IN}	

Note: H = V_{IH} , L = V_{IL} , X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP. ⁴	MAX.	UNIT
Supply Voltage	V _{CC}				2.7	3.0	3.6	V
Input High Voltage	V _{IH} ¹				2.2	-	V _{CC} +0.3	V
Input Low Voltage	V _{IL} ²				- 0.2	-	0.6	V
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}			- 1	-	1	μA
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} Output Disabled			- 1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = -1mA			2.2	2.7	-	V
Output Low Voltage	V _{OL}	I _{OL} = 2mA			-	-	0.4	V
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} and CE2 = V _{IH} I _{I/O} = 0mA Other pins at V _{IL} or V _{IH}		- 55	-	45	80	mA
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V and CE2 ≥ V _{CC} -0.2V I _{I/O} = 0mA Other pins at 0.2V or V _{CC} -0.2V			-	10	20	mA
Standby Power Supply Current	I _{SB}	CE# = V _{IH} or CE2 = V _{IL} Other pins at V _{IL} or V _{IH}			-	0.3	2	mA
	I _{SB1}	CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V	- SL	25℃	-	6	16	μA
			- SLI	40℃	-	6	16	μA
			- SL	25℃	-	6	60	μA
			- SLI	40℃	-	6	80	μA

Notes:

- $V_{IH}(\max) = V_{CC} + 2.0V$ for pulse width less than 6ns.
- $V_{IL}(\min) = V_{SS} - 2.0V$ for pulse width less than 6ns.
- Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
- Typical values are included for reference only and are not guaranteed or tested.

Typical values are measured at $V_{CC} = V_{CC}(TYP.)$ and $T_A = 25^\circ C$

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS6C3216-55		UNIT
		MIN.	MAX.	
Read Cycle Time	t _{RC}	55	-	ns
Address Access Time	t _{AA}	-	55	ns
Chip Enable Access Time	t _{ACE}	-	55	ns
Output Enable Access Time	t _{OE}	-	30	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	20	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	20	ns
Output Hold from Address Change	t _{OH}	10	-	ns
LB#, UB# Access Time	t _{BA}	-	55	ns
LB#, UB# to High-Z Output	t _{BHZ} *	-	25	ns
LB#, UB# to Low-Z Output	t _{BLZ} *	10	-	ns

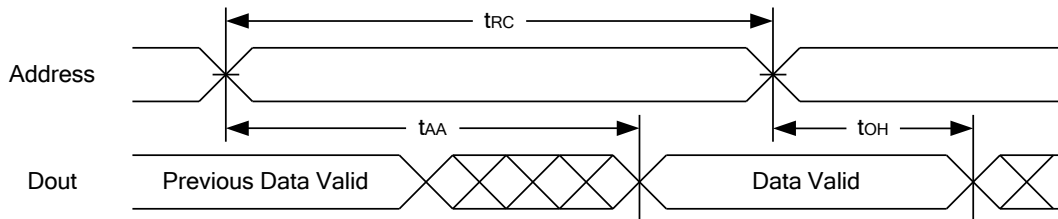
(2) WRITE CYCLE

PARAMETER	SYM.	AS6C3216-55		UNIT
		MIN.	MAX.	
Write Cycle Time	t _{WC}	55	-	ns
Address Valid to End of Write	t _{AW}	50	-	ns
Chip Enable to End of Write	t _{CW}	50	-	ns
Address Set-up Time	t _{AS}	0	-	ns
Write Pulse Width	t _{WP}	45	-	ns
Write Recovery Time	t _{WR}	0	-	ns
Data to Write Time Overlap	t _{DW}	25	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	20	ns
LB#, UB# Valid to End of Write	t _{BW}	45	-	ns

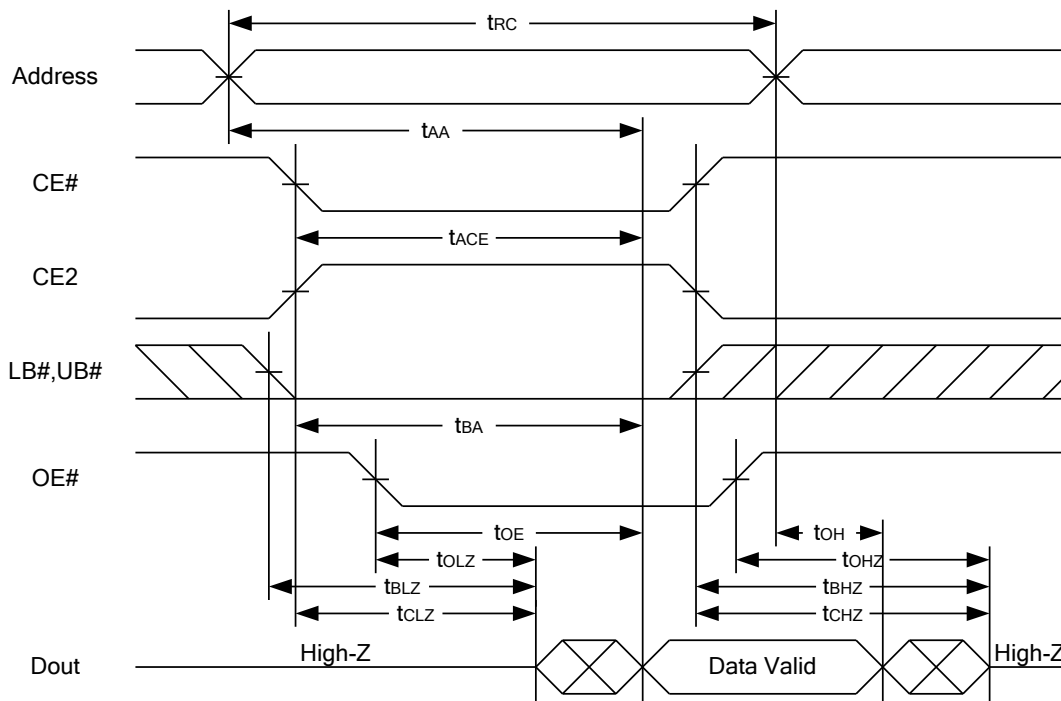
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



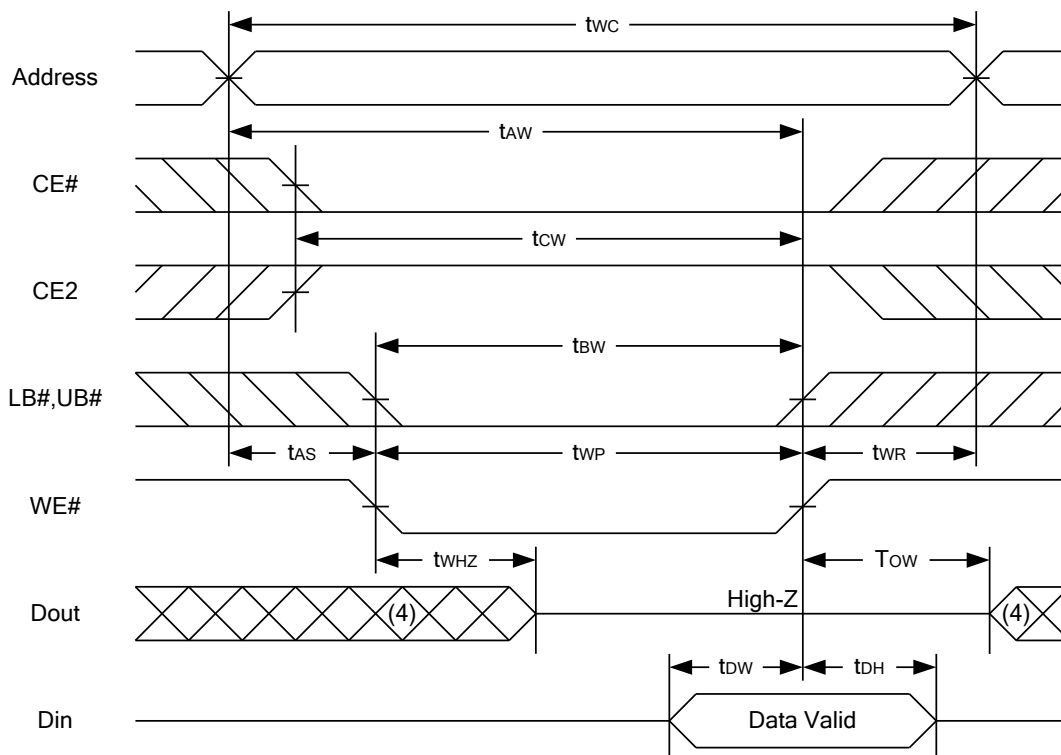
READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



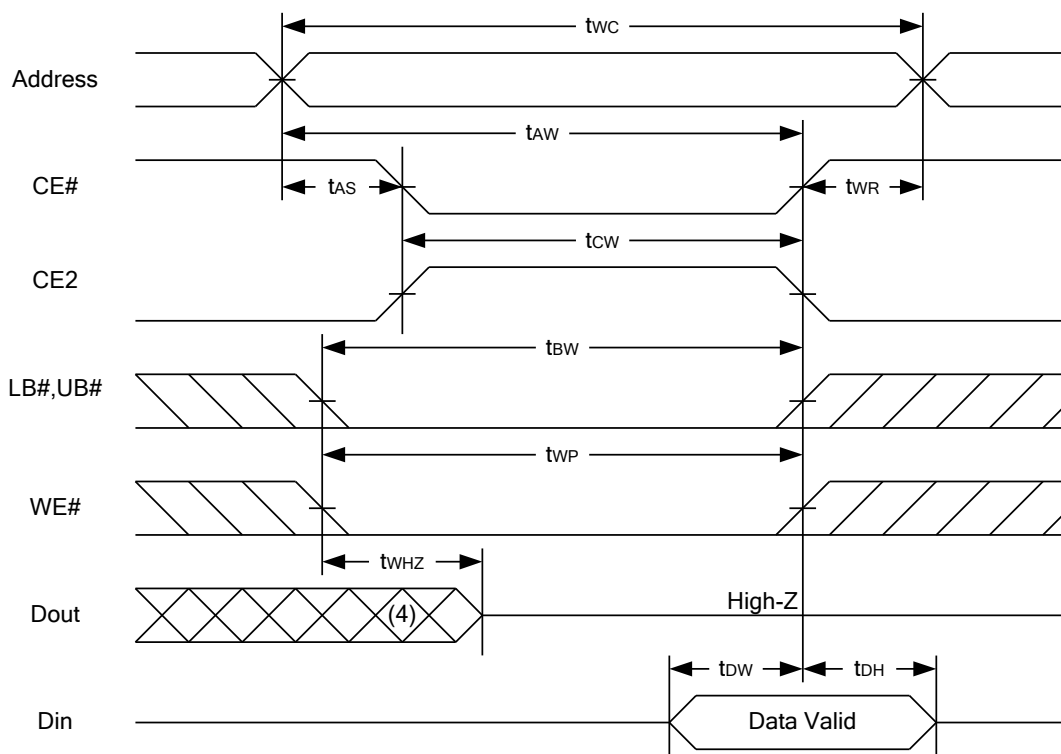
Notes :

- 1.WE# is high for read cycle.
- 2.Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.
- 3.Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise tAA is the limiting parameter.
- 4.tCLZ, tBLZ, tOLZ, tCHZ, tBHZ and tOHZ are specified with CL = 5pF. Transition is measured $\pm 500\text{mV}$ from steady state.
- 5.At any given temperature and voltage condition, tCHZ is less than tCLZ, tBHZ is less than tBLZ, tOHZ is less than tOLZ.

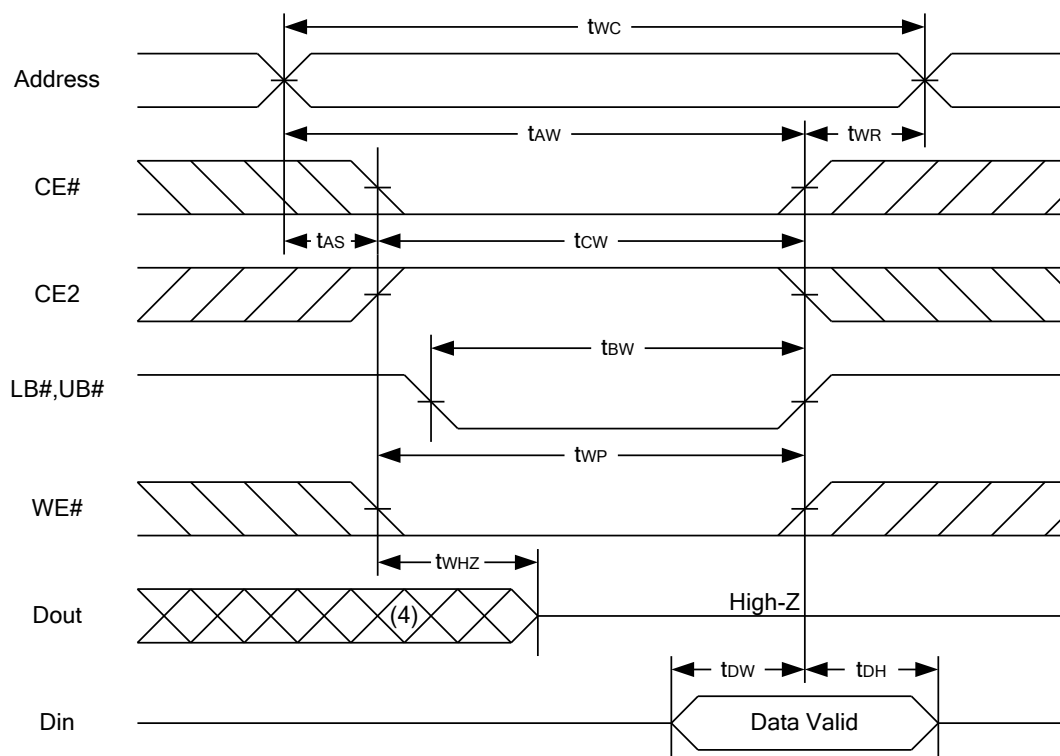
WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)



WRITE CYCLE 3 (LB#,UB# Controlled) (1,2,5,6)



Notes :

1. WE#, CE#, LB#, UB# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.
3. During a WE# controlled write cycle with OE# low, tWP must be greater than tWHZ + tDW to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tDW and tWHZ are specified with CL = 5pF. Transition is measured $\pm 500\text{mV}$ from steady state.

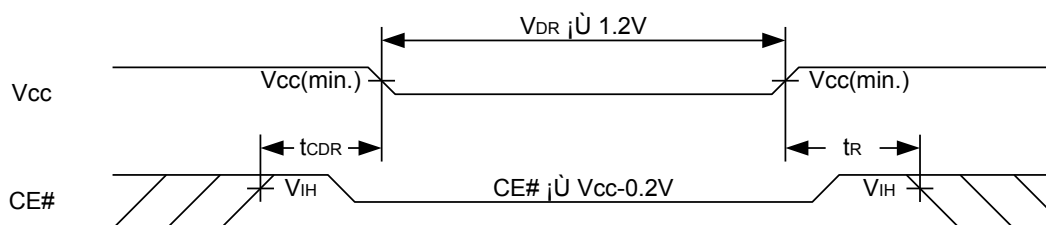
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION				MIN.	TYP.	MAX.	UNIT
VCC for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V				1.2	-	3.6	V
Data Retention Current	I _{DR}	V _{CC} = 1.2V CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V other pins at 0.2V or V _{CC} -0.2V	-SL	25°C	-	6	16	μA	
			-SLI	40°C	-	6	16	μA	
			-SL	25°C	-	6	60	μA	
			-SLI	40°C	-	6	80	μA	
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)				0	-	-	ns
Recovery Time	t _R					t _{RC} *	-	-	ns

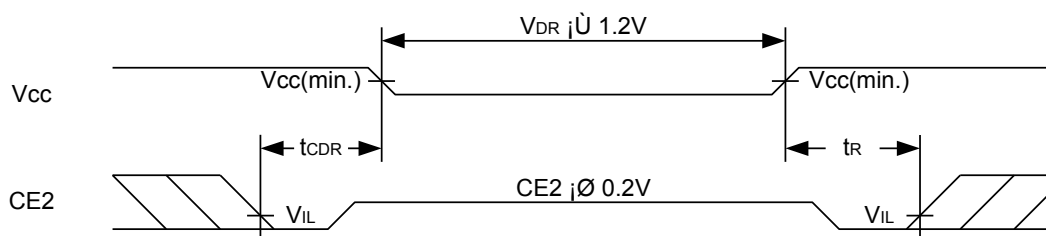
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

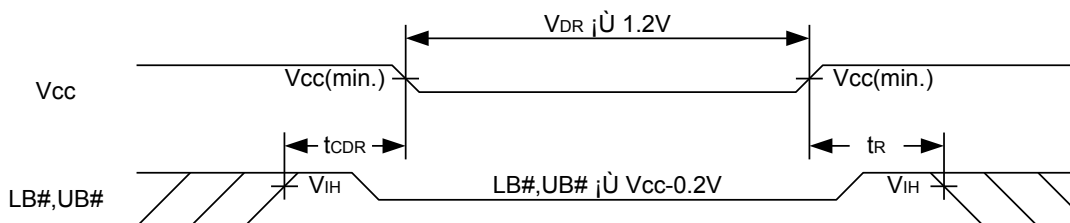
Low V_{CC} Data Retention Waveform (1) (CE# controlled)



Low V_{CC} Data Retention Waveform (2) (CE2 controlled)

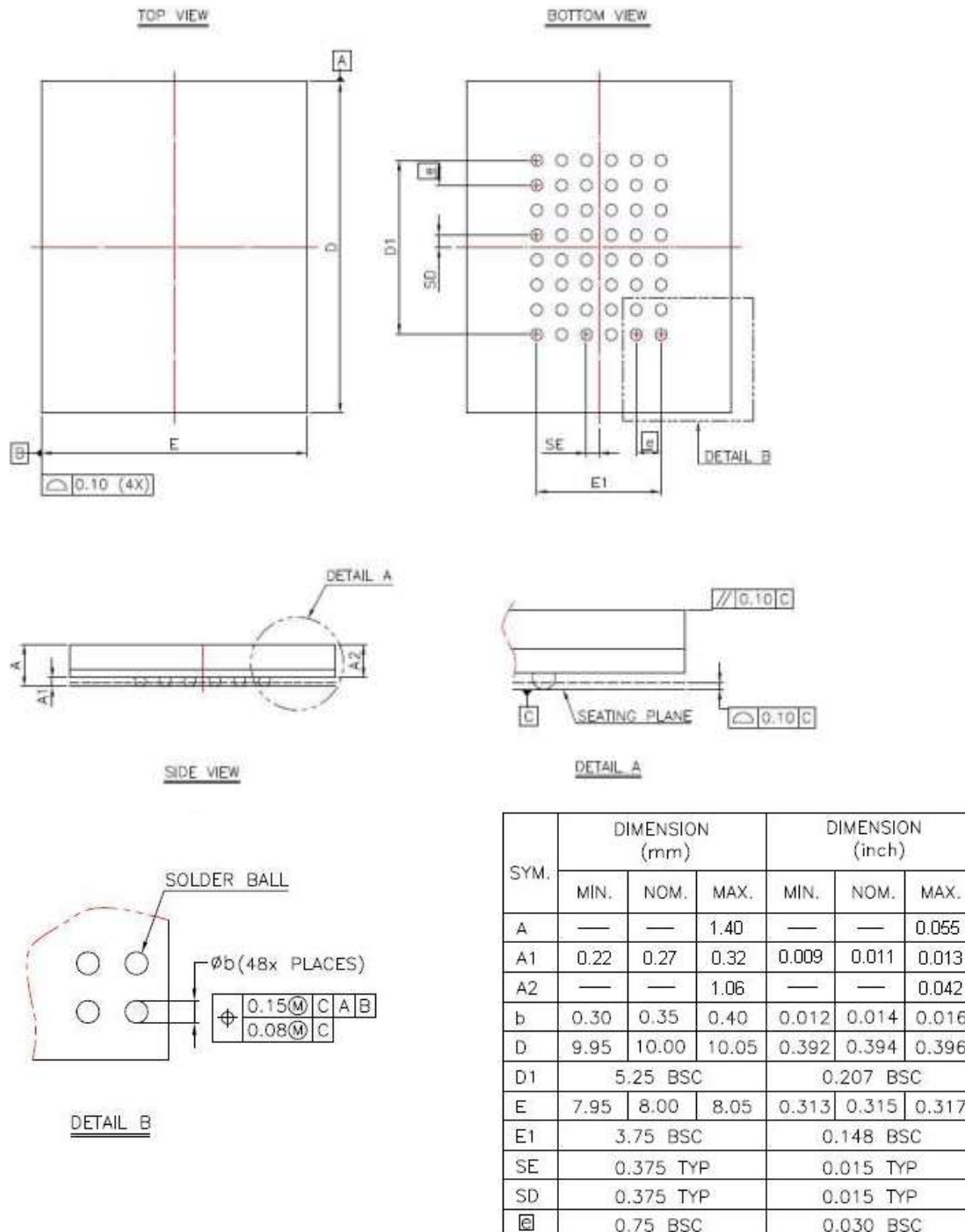


Low V_{CC} Data Retention Waveform (3) (LB#, UB# controlled)



PACKAGE OUTLINE DIMENSION

48-ball 8mm × 10mm TFBGA Package Outline Dimension



NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.

ORDERING INFORMATION

Alliance Part no	Organisation	Vcc Range	Package	Operating Temp	Speed ns
AS6C3216-55BIN - Tray	2048 x 16	2.7V – 3.6V	48-ball 8mm x 10mm TFBGA	-40°C~85°C	55
AS6C3216-55BINTR – Tape Reel	2048 x 16	2.7V – 3.6V	48-ball 8mm x 10mm TFBGA	-40°C~85°C	55

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