



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



FEATURES

- 8 analog input channels, integrated secondary monitor**
±3 mV maximum cell voltage accuracy, TUE, 14-bit ADC
- Very low measurement latency across 96 cells**
- Stack voltage measurement**
±16 mV typical battery stack voltage (TUE) accuracy
- Cell balancing interface, with individually programmable on time**
- 4 auxiliary analog input channels, 14-bit ADC**
Suitable for thermistor inputs and external diagnostics
- Buffered reference output for ratiometric measurements**
- Internal temperature sensor**
- V_{DD} operating range: 10 V to 40 V**
- On-chip 5 V regulator**
- Watchdog timer**
- I_{DD} matching current: 100 µA**
- Robust, proprietary daisy-chain interface**
- SPI to host controller**
- CRC protection on read and write commands**
- 2 general-purpose outputs**
- 64-lead low profile quad flat package, exposed pad (LQFP_EP)**
- Junction temperature range: –30°C to +120°C**
- Qualified for automotive applications**

APPLICATIONS

- Li-Ion battery monitoring**
- Electric and hybrid electric vehicles**
- Stationary power applications**

GENERAL DESCRIPTION

The **AD7284** contains all the functions required for the general-purpose monitoring of stacked Li-Ion batteries, as used in hybrid electric vehicles and battery backup applications.

The **AD7284** has multiplexed cell voltage and auxiliary, analog-to-digital converter (ADC) measurement channels supporting four to eight cells of battery management. The device provides a maximum total unadjusted error, TUE, (cell voltage accuracy) of ±3 mV that includes all the internal errors from input to output. The primary ADC resolution is 14 bits.

The **AD7284** also includes an integrated secondary measurement path that validates the data on the primary ADC. Other diagnostic features include the detection of open inputs, communication, and power supply related faults.

The **AD7284** cell balancing interface outputs control the external field effect transistors (FETs) to allow discharging of individual cells.

FUNCTIONAL BLOCK DIAGRAM

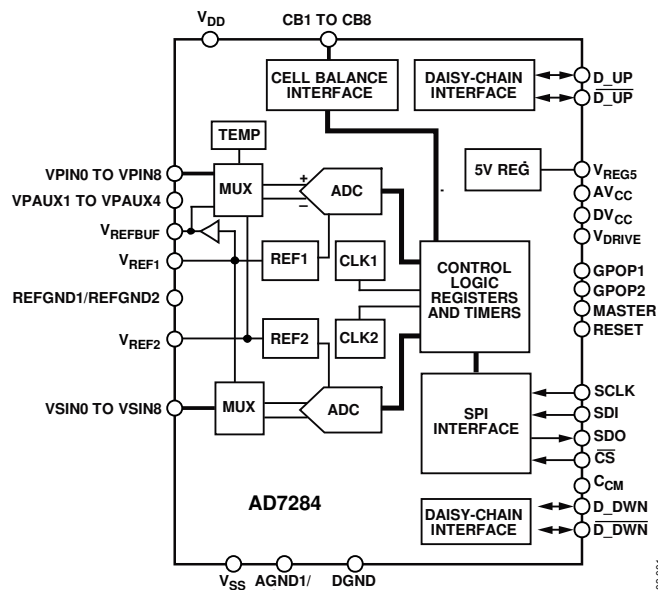


Figure 1.

There are two on-chip 2.5 V voltage references: one reference for the primary measurement path, and one for the secondary measurement path.

The **AD7284** operates from one V_{DD} supply, ranging from 10 V to 40 V. The device provides eight differential analog input channels to accommodate large common-mode signals across the full V_{DD} range. Each channel allows an input signal range, VPIN_x – VPIN(x – 1) and VSIN_x – VSIN(x – 1), of 0 V to 5 V, where x = 0 to 8. The input pins assume a series stack of eight cells. The **AD7284** includes four auxiliary ADC input channels that can be used for temperature measurement or system diagnostics.

The **AD7284** has a differential daisy-chain interface that allows multiple devices to be stacked without the need for individual device isolation. By design, this interface allows both device to device communication within the same module and communication between devices on different modules.

Rev. B

[Document Feedback](#)

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 ©2018 Analog Devices, Inc. All rights reserved.
[Technical Support](#) www.analog.com

TABLE OF CONTENTS

Features	1	Modes of Operation	25
Applications	1	Active Mode, Power-Up	25
General Description	1	Reset	26
Functional Block Diagram	1	Power-Down	26
Revision History	2	Watchdog Timer	28
Specifications	3	Serial Peripheral Interface (SPI)	29
ADC Timing Specifications	6	Register Write and Register Read Operations	29
Serial Peripheral Interface (SPI) Timing Specifications	7	Conversion Data Readback Operation	30
Absolute Maximum Ratings	8	CRC Pseudocode Examples	31
Thermal Data	8	Daisy-Chain Interface	32
Thermal Resistance	8	Daisy-Chain Physical Interface	32
ESD Caution	8	Daisy-Chain Protocol	32
Pin Configuration and Function Descriptions	9	Daisy-Chain Debug Mode	32
Typical Performance Characteristics	11	Register Map	33
Terminology	14	Page Addressing	33
Theory of Operation	15	Page 0 Addresses	35
Circuit Information	15	Page 1 Addresses	36
Converter Operation	16	Registers Common to Page 0 and Page 1	40
Internal Temperature Sensor	17	Examples of Interfacing with the AD7284	41
Auxiliary ADC Inputs	17	Register Write and Register Read Operations Examples	41
Voltage References	17	Conversion Data Readback Operation Examples	42
Cell Connections	18	Applications Information	44
ADC Conversions Sequence	19	Typical Connection Diagrams	44
Converting with a Single AD7284	20	Hot Plug	47
Converting with a Chain of AD7284 Devices	21	Service Disconnect (SD)	47
Conversion Data Readback	22	Transformer Configuration	48
Cell Balancing Outputs	23	Outline Dimensions	49
Open Input Detection	24	Ordering Guide	49
Power Management	25	Automotive Products	49
AD7284 Supplies	25		

REVISION HISTORY

4/2018—Rev. A to Rev. B

Changes to Table 1..... 3

5/2017—Revision A: Initial Version

SPECIFICATIONS

$V_{DD} = 10\text{ V to }40\text{ V}$, $V_{SS} = 0\text{ V}$, $DV_{CC} = AV_{CC} = V_{REG5}$, $V_{DRIVE} = 3.0\text{ V to }5.5\text{ V}$, unless otherwise noted. $T_J = -30^\circ\text{C to }+120^\circ\text{C}$, where T_J is the junction temperature, unless otherwise noted. See the Thermal Data section for more details.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PRIMARY ADC DC ACCURACY (VPIN0 to VPIN8)					
Resolution ¹	14			Bits	No missing codes, 305 $\mu\text{V}/\text{LSB}$
Integral Nonlinearity (INL)		± 1.4		LSB	
Differential Nonlinearity (DNL)		± 0.8		LSB	
ADC Unadjusted Error ¹		± 1		mV	
TUE ^{2, 3}					
VPINx – VPIN(x – 1) Range					
2 V to 3.6 V		± 1	± 3	mV	$10^\circ\text{C} \leq T_J \leq 75^\circ\text{C}$
2 V to 4.3 V		± 1	± 5	mV	$-10^\circ\text{C} \leq T_J \leq +105^\circ\text{C}$
0 V to 5 V ¹		± 1	± 10	mV	$7.5\text{ V} \leq V_{DD} \leq 40\text{ V}$
PRIMARY ADC CELL VOLTAGE INPUTS (VPIN0 to VPIN8)					
Pseudo Differential Input Voltage Range					
VPINx – VPIN(x – 1)	0		5	V	Convert start command issued every 100 ms
Static Leakage Current		± 30	± 100	nA	
Dynamic Leakage Current		± 3		nA	
Input Capacitance		15		pF	
PRIMARY ADC DC ACCURACY (VPAUX1 to VPAUX4)					
Resolution	14			Bits	No missing codes, 305 $\mu\text{V}/\text{LSB}$
INL ¹		± 1.5		LSB	
DNL ¹		± 0.8		LSB	
ADC Unadjusted Error ¹		± 2		mV	
TUE ²					
VPAUXx Range					
0 V to 2.5 V ¹		± 2	± 5	mV	$-10^\circ\text{C} \leq T_J \leq +105^\circ\text{C}$
0 V to 5 V ¹		± 2	± 10	mV	$7.5\text{ V} \leq V_{DD} \leq 40\text{ V}$
PRIMARY ADC AUXILIARY INPUTS (VPAUX1 to VPAUX4)					
Input Voltage Range ¹	0		5	V	Convert start command issued every 100 ms
Static Leakage Current		± 80	± 100	nA	
Dynamic Leakage Current		± 3		nA	
Input Capacitance		15		pF	
PRIMARY ADC DC ACCURACY (VSTK ⁴)					
Resolution ¹	14			Bits	No missing codes, 4.88 mV/LSB
TUE ²					
Battery Stack Voltage (VSTK) Range					
10 V to 28.8 V ¹		± 16	± 24	mV	$10^\circ\text{C} \leq T_J \leq 75^\circ\text{C}$
7.5 V to 40 V ¹		± 16	± 50	mV	Relative to the sum of the cells
VSTK Voltage Accuracy					
VSTK Range					
10 V to 28.8 V ¹		± 2	± 15	mV	$10^\circ\text{C} \leq T_J \leq 75^\circ\text{C}$
7.5 V to 40 V ¹		± 2	± 30	mV	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SECONDARY ADC DC ACCURACY (VSIN0 to VSIN8)					
Resolution	10			Bits	No missing codes, 4.88 mV/LSB
INL		±1		LSB	
DNL		±0.8		LSB	
TUE ^{2,3}		±15	±25	mV	7.5 V ≤ V _{DD} ≤ 40 V
SECONDARY ADC CELL VOLTAGE INPUTS (VSIN0 to VSIN8)					
Pseudo Differential Input Voltage VSINx – VSIN(x – 1)	0		5	V	
Static Leakage Current		±5	±100	nA	
Dynamic Leakage Current		±3		nA	Convert start command issued every 100 ms
Input Capacitance		15		pF	
REFERENCE (V _{REF1} , V _{REF2})					
Reference Voltage		2.5		V	
Reference Temperature Coefficient		±3		ppm/°C	Included in the TUE specification
Output Voltage Hysteresis		160		ppm	
Long-Term Drift ⁵		320		ppm/ 2000 hours	Primary reference
Turn On Settling Time		5		ms	C _{REF1} = 1 μF//100 nF, C _{REF2} = 1 μF//100 nF
REFERENCE BUFFER OUTPUT (V _{REFBUF})					
Output Voltage Accuracy	–4.5	±1	+4.5	mV	Relative to V _{REF1} output voltage
Output Current			1	mA	
Load Regulation		0.25		mV/mA	
Turn On Settling Time		5		ms	C _{REFBUF} = 1 μF
REGULATOR OUTPUT (V _{REG5})					
Output Voltage	4.8	5	5.2	V	
Output Current		2		mA	
Line Regulation		0.5		mV/V	
Load Regulation		0.5		mV/mA	
Internal Short-Circuit Protection Limit		30		mA	
CELL BALANCING OUTPUTS ⁶					CB1 to CB8 output
Output Voltage					
High, V _{OH}	3.7	5	5.3	V	I _{SOURCE} = 20 μA
Low, V _{OL}		0	0.09	V	
Ramp-Up and Ramp-Down Time		100		μs	For a 80 pF load
INTERNAL TEMPERATURE SENSOR					Measures junction temperature
Accuracy ¹		±3		°C	–30°C ≤ T _J ≤ +120°C
Resolution		0.03125		°C/LSB	
LOGIC INPUTS (EXCEPT RESET)					
Input Voltage					
High, V _{INH}	V _{DRIVE} × 0.7			V	
Low, V _{INL}			V _{DRIVE} × 0.3	V	
Input Current, I _{IN}		10		μA	
Input Capacitance, C _{IN}		5		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS					
Output Voltage					
High, V_{OH}	$V_{DRIVE} \times 0.9$			V	$I_{SOURCE} = 200 \mu A$
Low, V_{OL}			0.4	V	$I_{SINK} = 200 \mu A$
Floating State					
Leakage Current		1		μA	
Output Capacitance		5		pF	
RESET					
t_{RESET}	100			ns	Pulse width to reset or wake up the AD7284 (V_{DRIVE} high)
Leakage Current		60		μA	
POWER REQUIREMENTS					
V_{DD} Operating Range	10		40	V	
Current Consumption on the V_{DD} Pin (I_{DD})					Applies to master and slave configurations
I_{DD} During Conversion	14	15	17	mA	
I_{DD} During Conversion Data Readback	15	16.5	18	mA	Continuous readback
I_{DD} During Cell Balancing	13	14	16	mA	
I_{DD} Idle	12	13	14	mA	Device in partial power-down
I_{DD} Partial Power-Down Mode	11	12	14	mA	To support transformer-based communications
I_{DD} Full Power-Down Mode	22	30	40	μA	
I_{DD} Matching Current		100		μA	Similar supply and temperature conditions across devices
TXIBAL	−3.9	−4.5	−4.9	mA	Bit D6 in Control Register 2
IDIODE	−0.39	−0.35	−0.32	mA	Bit D5 in Control Register 2
RXIBAL		0.12	0.56	mA	Bit D4 in Control Register 2
IMASTER	−3.5	−4.0	−4.5	mA	Bit D3 in Control Register 2
Master Configuration Only					
V_{DRIVE}	3.0		5.5	V	Typically 3.3 V or 5 V
V_{DRIVE} Threshold		0.8		V	To wake up the master device
I_{DRIVE}		15		μA	

¹ Guaranteed by design and/or characterization.

² TUE includes the INL of the ADC, the gain and offset errors of the input channels, as well as the reference error; that is, the difference between the ideal and actual reference voltage and the temperature coefficient of the reference.

³ These specifications assume that all cells are in the same input voltage range, for example, $VPINx - VPIN(x - 1)$ range = 2 V to 3.6 V.

⁴ VSTK, the battery stack voltage, is scaled down internally by a factor of 16 before being applied to the ADC for measurement.

⁵ Data generated from high temperature operating life (HTOL) reliability testing.

⁶ For CB1 to CB5, the CBx output can be set to 0 V to 5 V with respect to the negative terminal of the cell being balanced. For CB6 to CB8, the CBx output can be set to 0 V to −5 V with respect to the positive terminal of the cell being balanced.

ADC TIMING SPECIFICATIONS

Table 2. ADC Timing for Three Devices in a Chain

Parameter ¹	Min	Typ	Max	Unit	Description
t_{CONV}		1040		ns	ADC conversion time
t_{ACQ}		400		ns	ADC acquisition time, Bits[D1:D0] of Control Register 2 set to 00
		800		ns	ADC acquisition time, Bits[D1:D0] of Control Register 2 set to 01
		1600		ns	ADC acquisition time, Bits[D1:D0] of Control Register 2 set to 10
		3200		ns	ADC acquisition time, Bits[D1:D0] of Control Register 2 set to 11
t_{START}	32	33.6	35	μ s	Delay from rising edge of $\overline{CS}$ (conversion command issued) to the first conversion
t_{DELAY}		100		ns	Propagation delay between two devices in the daisy chain

¹ All input signals are specified with $t_{RISE} = t_{FALL} = 5$ ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V. All timing specifications given are with a 25 pF load capacitance.

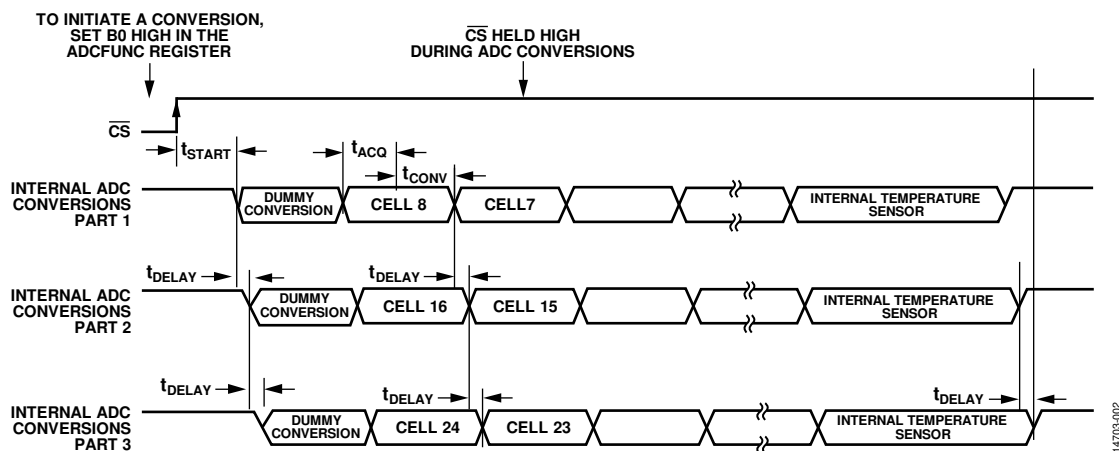


Figure 2. ADC Timing Diagram for Three Devices in a Chain

SERIAL PERIPHERAL INTERFACE (SPI) TIMING SPECIFICATIONS

Table 3.

Parameter ¹	Min	Typ	Max	Unit	Description
f_{SCLK}		500		kHz	Frequency of the serial read clock on the SCLK pin for write and read registers
		725 ²		kHz	Frequency of the serial read clock on the SCLK pin for write registers only
		725 ²		kHz	Frequency of the serial read clock on the SCLK pin for read conversion data on slave devices
t_1	200			ns	$\overline{\text{CS}}$ falling edge to SCLK rising edge
t_2^3			20	ns	Delay from $\overline{\text{CS}}$ falling edge to SDO active
t_3	10			ns	SDI setup time prior to SCLK falling edge
t_4	10			ns	SDI hold time after SCLK falling edge
t_5^4			40	ns	Data access time after SCLK rising edge
t_6	20			ns	SCLK to data valid hold time
t_7	$0.5 \times t_{\text{SCLK}}$			ns	SCLK high pulse width
t_8	$0.5 \times t_{\text{SCLK}}$			ns	SCLK low pulse width
t_9	100			ns	$\overline{\text{CS}}$ rising edge to SCLK rising edge
t_{10}^5			10	ns	$\overline{\text{CS}}$ rising edge to SDO high impedance
t_{11}	400			ns	$\overline{\text{CS}}$ high time
t_{12}		1.5		ns	Time from falling edge of last SCLK to rising edge of $\overline{\text{CS}}$

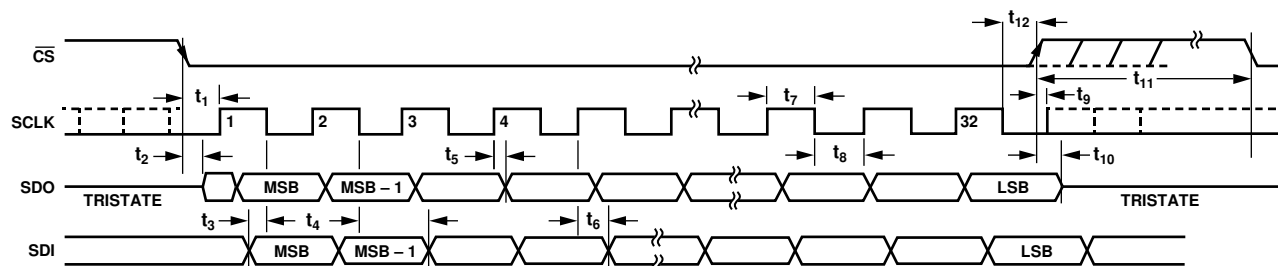
¹ All input signals are specified with $t_{\text{RISE}} = t_{\text{FALL}} = 5 \text{ ns}$ (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V. All timing specifications given are with a 25 pF load capacitance.

² Setting Bit D26 of the register address (see the Register Address section and Table 10) to 1 allows SCLK to increase to 725 kHz, as described in the Register Write and Register Read Operations section.

³ Guaranteed by design and/or characterization.

⁴ Time required for the output to cross 0.4 V or 2.4 V.

⁵ t_{10} applies when using a continuous SCLK signal. Guaranteed by design.

Figure 3. SPI Timing Diagram for a 32-Bit $\overline{\text{CS}}$ Frame

14703-003

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are defined with respect to the normal operating specifications and not to other maximum rating specifications. The mnemonics listed in the rating column refer to the values as defined in the Specifications section only.

Table 4.

Parameter	Rating
V _{DD}	V _{SS} ¹ – 0.3 V to V _{SS} + 48 V
MASTER	V _{SS} – 0.3 V to V _{DD} + 0.3 V
V _{DRIVE} , V _{REGS} ²	V _{SS} – 0.3 V to V _{SS} + 6 V
ADCGND1 to ADCGND2 to V _{SS}	–0.3 V to +0.3 V
VPIN0, VSIN0	V _{SS} – 0.3 V to V _{SS} + 0.3 V
VPIN1 to VPIN7, VSIN1 to VSIN7	V _{SS} –0.3 V to V _{DD} + 0.3 V
VPIN8, VSIN8	V _{DD} –0.3 V to V _{DD} +1 V
Pseudo Differential Input Voltage ³	
VPINx – VPIN(x – 1)	–0.3 V to +6 V
VPAUX1 to VPAUX4	V _{SS} – 0.3 V to V _{REGS} + 0.3 V
CB1	V _{SS} – 0.3 V to V _{REGS} + 0.3 V
CB2 to CB7	V _{SS} to V _{DD}
CB8	V _{DD} – 6 V to V _{DD}
Relative Input/Output Voltages	
CBx – VPINx – 1, x = 2 to 5	–0.3 V to +6 V
CBx – VPINx, x = 6 to 8	–6 V to +0.3 V
D_UP, D_UP	V _{SS} – 0.3 V to V _{DD} + 7 V
D_DWN, D_DWN	V _{SS} – 0.3 V to V _{REGS} + 0.3 V
Digital Input Voltage	V _{SS} – 0.3 V to V _{DRIVE} + 0.3 V
Digital Output Voltage	V _{SS} – 0.3 V to V _{DRIVE} + 0.3 V
Analog Outputs (V _{REF1} , V _{REFBUF} , C _{CM})	V _{SS} – 0.3 V to V _{REGS} +0.3 V
ESD Human Body Model (HBM) Rating	
ANSI/ESDA/JEDEC JS-001-2010 (Standard HBM), All Pins	2.5 kV
Operating Junction Temperature Range	–40°C to +120°C
Absolute Maximum Junction Temperature	150°C
Storage Temperature	150°C
Reflow Profile	J-STD 20 (JEDEC)

¹ V_{SS}, DGND, AGND1, AGND2, REFGND1, and REFGND2 are internally shorted on chip and must be connected together on the printed circuit board (PCB). See the pin descriptions of these pins in the Pin Configuration and Function Descriptions section for additional information.

² V_{REGS}, AV_{CC}, and DV_{CC} are internally shorted on chip and must be connected together on the PCB. See the pin descriptions of these pins in the Pin Configuration and Function Descriptions section for additional information.

³ Applies to primary and secondary analog voltage inputs; x = 1 to 8.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

The IPC 2221 industrial standard recommends the use of conformal coating on high voltage pins.

THERMAL DATA

The junction temperature (T_J) refers to the temperature of the silicon die within the package of the device when the device is powered. The AD7284 parameters are specified over a junction temperature range of –30°C to +120°C.

The absolute maximum junction temperature of the AD7284 is 150°C. The AD7284 may be damaged when the junction temperature limit is exceeded. Monitoring of the junction temperature, or the ambient temperature in conjunction with an accurate thermal model, guarantees that T_J is within the specified temperature limits.

Measure the junction temperature using the internal temperature sensor.

Use the junction temperature (T_J) and the power dissipation (P_D) to calculate the ambient temperature (T_A) by

$$T_A = T_J - (P_D \times \theta_{JA})$$

where θ_{JA} is the junction to ambient thermal resistance of the package.

THERMAL RESISTANCE

The AD7284 is in a 64-lead LQFP_EP package with an exposed pad. The exposed pad is added for thermal performance purposes.

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

Table 5. Thermal Resistance¹

Package Type	θ_{JA} ²	Unit
SW-64-2	32	°C/W

¹ Thermal impedance values take into account the localized heat distribution on the die.

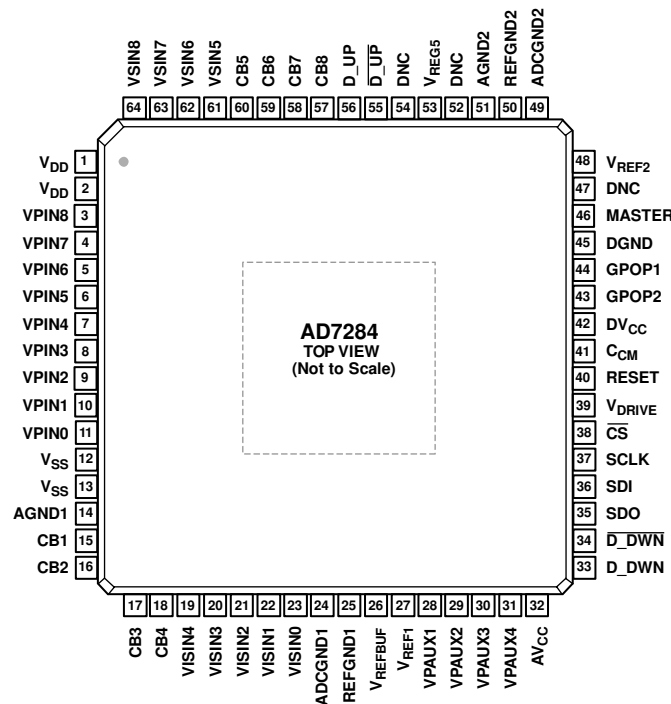
² Test Condition 1: thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with 25 thermal vias. See the JEDEC51 standard.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THESE PINS.
2. THE EXPOSED PAD IS PROVIDED FOR THERMAL PURPOSES AND MUST BE SOLDERED DOWN TO THE BOARD. THE EXPOSED PAD IS INTERNALLY CONNECTED TO V_{SS} ON THE DIE AND MUST BE CONNECTED TO THE V_{SS} PIN OF THE DEVICE ON THE PCB.

14703-004

Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2	V_{DD}	Positive Power Supply Voltage. These pins are connected to the top of the battery stack. Place 4.6 μ F to 4.8 μ F decoupling capacitors on the V_{DD} pins. It is also recommended that a current limiting resistor be connected between V_{DD} and the top of the stack.
3 to 11	VPIN8 to VPIN0	Primary Analog Voltage Inputs for Monitoring Up to Eight Cells. Connect VPIN0 to the base of the series of the connected battery cells and, therefore, to the bottom of Cell 1. Connect VPIN1 to the top of Cell 1, connect VPIN2 to the top of Cell 2, and so on.
12, 13	V_{SS}	Negative Power Supply Voltage. These pins are connected to the bottom of the battery stack. These inputs must be at the same potential as all the analog and digital grounds of the device.
14, 51	AGND1, AGND2	Analog Ground Pins. These pins are the ground reference point for most of the analog circuitry on the AD7284. These inputs must be at the same potential as V_{SS} .
15 to 18, 57 to 60	CB1 to CB8	Cell Balance Outputs for Balancing Up to Eight Cells. These pins provide a voltage output that can supply the gate drive of an external cell balancing transistor. The CB1 to CB5 outputs provide a 0 V to 5 V voltage output referenced to the absolute voltage of the negative terminal of the battery cell that is being balanced. The CB6 to CB8 outputs provide a 0 V to -5 V voltage output referenced to the absolute voltage of the positive terminal of the battery cell that is being balanced.
19 to 23, 61 to 64	VSIN0 to VSIN8	Secondary Analog Voltage Inputs for Monitoring Up to Eight Cells. These pins can connect directly to the corresponding primary analog voltage inputs, or they can connect separately to the battery cells. If connected separately to the battery cells, connect VSIN0 to the base of the series connected battery cells and, therefore, to the bottom of Cell 1. Connect VSIN1 to the top of Cell 1, connect VSIN2 to the top of Cell 2, and so on.
24, 49	ADCGND1, ADCGND2	Analog Grounds for the Primary and Secondary ADCs. These pins must be at the same potential as V_{SS} .
25, 50	REFGND1, REFGND2	Reference Grounds. These pins are the ground reference points for the primary and secondary internal band gap references. These pins must be at the same potential as V_{SS} .
26	V_{REFBUF}	2.5 V Reference Buffer Output Voltage. A 1 μ F decoupling capacitor connected to REFGND1 is recommended on this pin.

Pin No.	Mnemonic	Description
27	V _{REF1}	2.5 V Primary Reference Output Voltage. A 1 μ F capacitor in parallel with a 100 nF decoupling capacitor connected to REFGND1 is recommended on this pin. V _{REF1} can be driven from an external reference, but it must not be used to drive any other circuit.
28 to 31	VPAUX1 to VPAUX4	Primary Auxiliary ADC Inputs (0 V to 5 V, Single-Ended). If any of these inputs are not required in the application, it is recommended that these pins be connected to V _{REG5} or V _{SS} through a 10 k Ω resistor.
32	AV _{CC}	Analog Supply Voltage. Decouple this supply pin to AGND1 with a 100 nF decoupling capacitor and connect this pin to the V _{REG5} output pin.
33, 34	D_DWN, $\overline{\text{D_DWN}}$	Daisy-Chain Lower Interface Ports. On slave devices, terminate these pins with a 50 Ω resistor connected to the C _{CM} pin. These pins are connected to the D_UP and $\overline{\text{D_UP}}$ pins on the AD7284 device below it in the daisy chain. On a master device, these pins are not used; connect these pins to V _{SS} via a 1 k Ω resistor instead.
35	SDO	Serial Data Output When Master Device. On a slave AD7284 device, this pin is not used and can be left unconnected.
36	SDI	Serial Data Input When Master Device. On a slave AD7284 device, this pin is not used and can be pulled low to DGND via a 1 k Ω resistor.
37	SCLK	Serial Clock Input When Master Device. On a slave AD7284 device, this pin is not used and can be pulled low to DGND via a 1 k Ω resistor.
38	$\overline{\text{CS}}$	Chip Select Input When Master Device. On a slave AD7284 device, this input is not used and can be connected to V _{SS} via a 1 k Ω resistor.
39	V _{DRIVE}	Digital Input/Output Supply Input. On a master device, connect an external voltage supply to the V _{DRIVE} pin. The voltage supplied at this pin determines the voltage at which the SPI interface operates. Decouple this pin to DGND with a 100 nF decoupling capacitor. On a master device, pulling V _{DRIVE} low powers down the device unless an active power-down timer is running. After the expiration of the power-down timer, the device powers down. On a slave device, connect the V _{DRIVE} pin to V _{REG5} .
40	RESET	Digital Input. An active high signal causes the device to reset to the power-on state. This input is internally pulled down. When this input is not used, an external 1 k Ω pull-down resistor to DGND is recommended.
41	C _{CM}	Common-Mode Decoupling Capacitor Port. This pin supplies a 2 V level used for the daisy-chain common mode. A 1 μ F decoupling capacitor to V _{SS} is required on this pin.
42	DV _{CC}	Digital Supply Voltage. Connect the DV _{CC} supply pin to the V _{REG5} output pin. Decouple this digital supply to DGND with a 100 nF decoupling capacitor.
43, 44	GPOP2, GPOP1	General-Purpose Outputs. These pins provide a voltage output level of 0 V for a low signal and a voltage output level of V _{DRIVE} for a high signal.
45	DGND	Digital Ground. This pin is the ground reference point for all digital circuitry on the AD7284. This pin must be at the same potential as V _{SS} .
46	MASTER	Voltage Input. When the AD7284 acts as a master, connect this pin to the V _{DD} supply pin through a 10 k Ω resistor. When the AD7284 acts as a slave, connect this pin to the V _{SS} supply pin of the same AD7284 device through a 10 k Ω resistor.
47, 52, 54	DNC	Do Not Connect. Do not connect to these pins.
48	V _{REF2}	2.5 V Secondary Reference Output Voltage. A 1 μ F capacitor in parallel with a 100 nF decoupling capacitor to REFGND2 is recommended on this pin. V _{REF2} can not be driven externally and must not be used to drive any other circuit.
53	V _{REG5}	5 V Analog Voltage Output. The internally generated V _{REG5} voltage provides the supply voltage for the ADC core. A 100 nF decoupling capacitor to AGND2 is required on the V _{REG5} pin.
55, 56	$\overline{\text{D_UP}}$, D_UP	Daisy-Chain Upper Interface Ports. Terminate these pins with a 50 Ω resistor connected to the V _{DD} pin directly for configurations using transformer isolation or via a capacitor when using the direct coupled configuration. The $\overline{\text{D_UP}}$ pin is connected to the D_DWN pin of the AD7284 device above it in the daisy chain, and the D_UP pin is connected to the D_DWN pin of the AD7284 device above it in the daisy chain.
	Exposed Pad	Exposed Pad. The exposed pad is provided for thermal purposes and must be soldered down to the board. The exposed pad is internally connected to V _{SS} on the die and must be connected to the V _{SS} pin of the device on the PCB.

TYPICAL PERFORMANCE CHARACTERISTICS

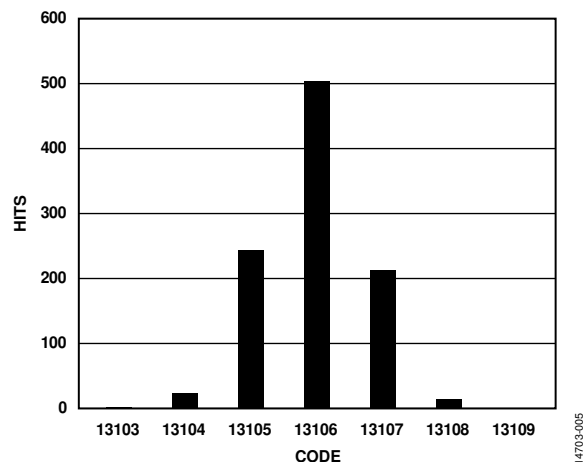
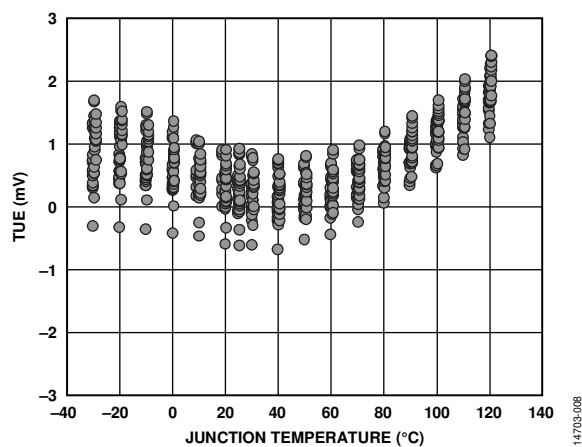
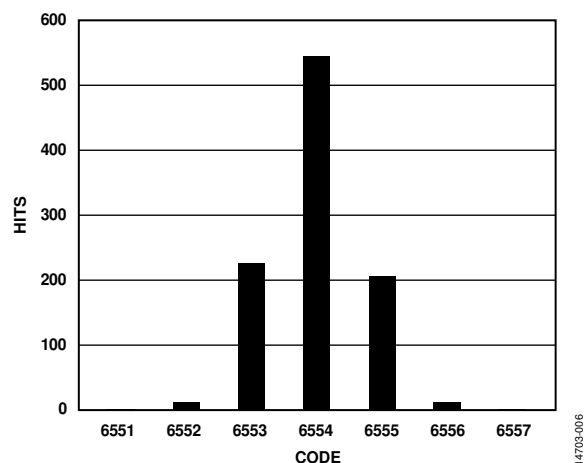
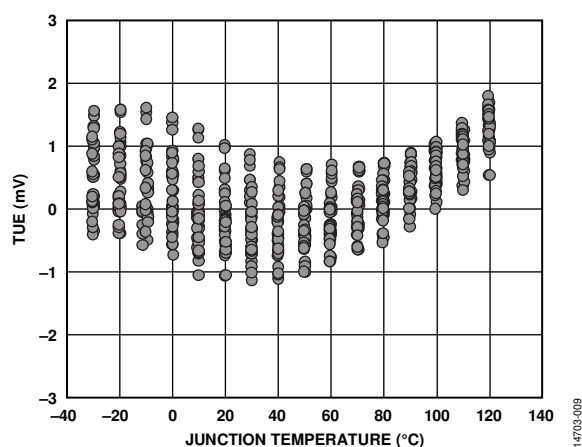
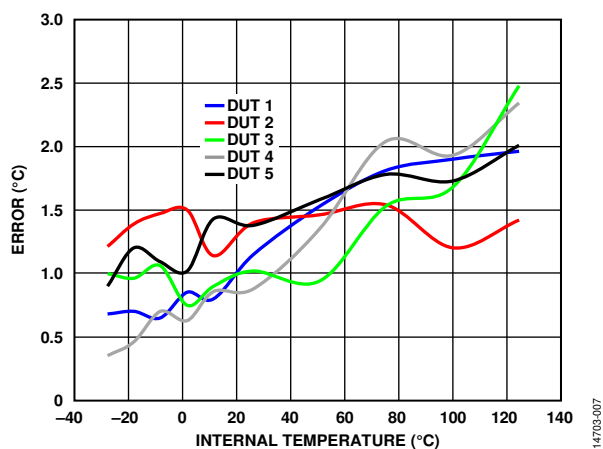
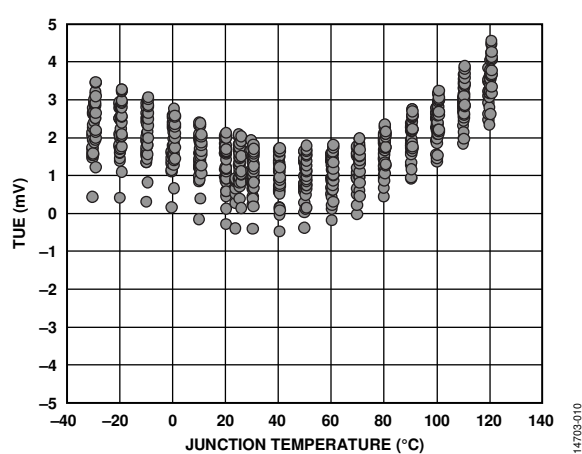
Figure 5. Typical Code Noise for VPIN1 Through VPIN8, $V_{DD} = 32\text{ V}$, $T_J = 60^\circ\text{C}$ Figure 8. TUE vs. Junction Temperature, Preassembly, $V_{DD} = 18\text{ V}$ Figure 6. Typical Code Noise for VSTK, $V_{DD} = 32\text{ V}$, $T_J = 60^\circ\text{C}$ Figure 9. TUE vs. Junction Temperature, Postassembly, $V_{DD} = 18\text{ V}$ 

Figure 7. Error vs. Internal Temperature for Various Devices Under Test (DUT)

Figure 10. TUE vs. Junction Temperature, Preassembly, $V_{DD} = 32\text{ V}$

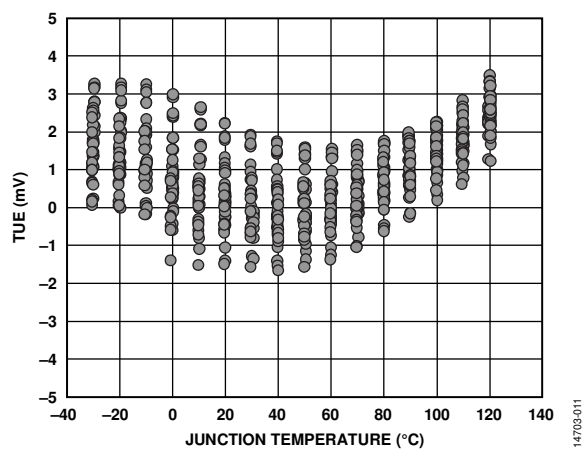


Figure 11. TUE vs. Junction Temperature, Postassembly, $V_{DD} = 32\text{ V}$

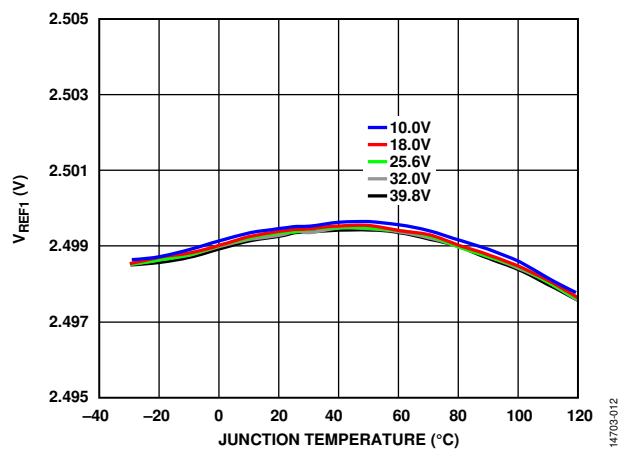


Figure 12. Preassembly Primary Voltage Reference, V_{REF1} vs. Junction Temperature

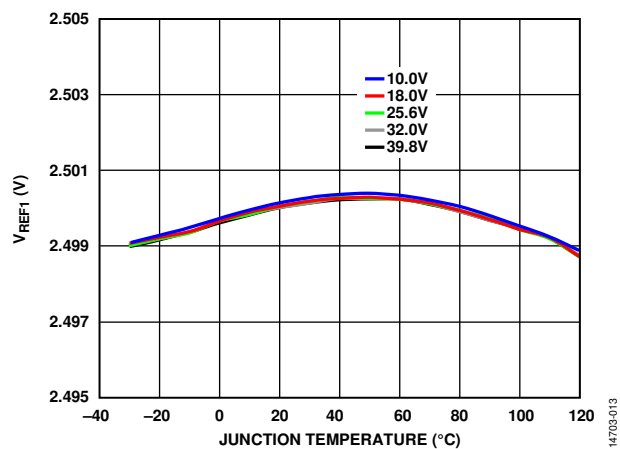


Figure 13. Postassembly Primary Voltage Reference, V_{REF1} vs. Junction Temperature

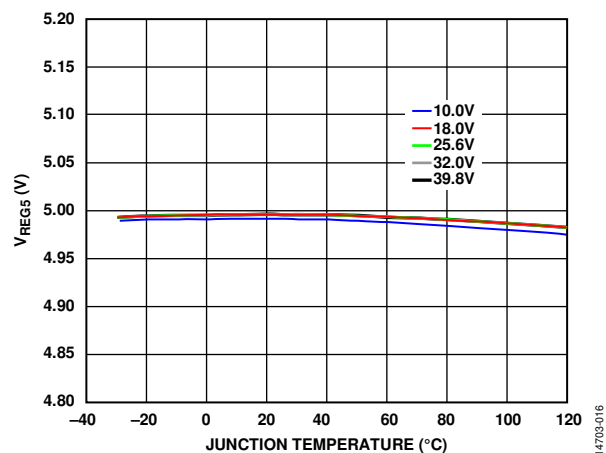


Figure 14. Preassembly 5 V Voltage Regulator Output (V_{REG5}) vs. Junction Temperature

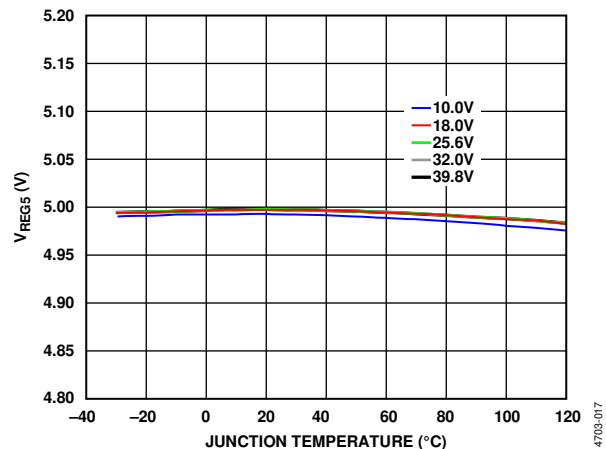


Figure 15. Postassembly 5 V Voltage Regulator Output (V_{REG5}) vs. Junction Temperature

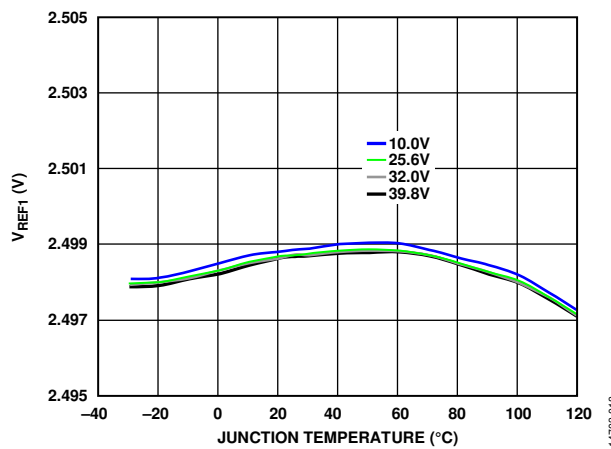


Figure 16. Preassembly Buffered Voltage Reference, V_{REF1} vs. Junction Temperature

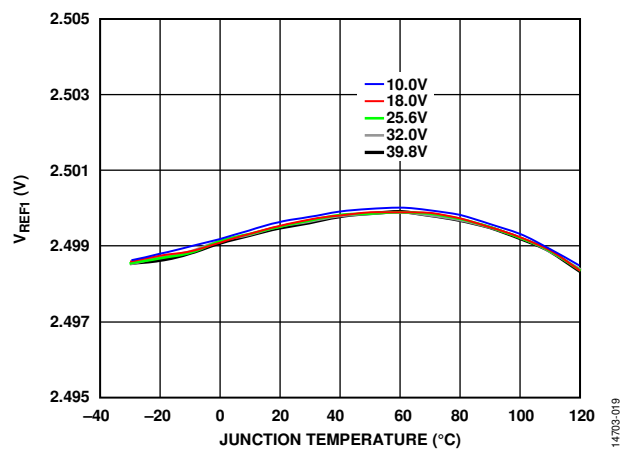


Figure 17. Postassembly Buffered Voltage Reference, V_{REF1} vs. Junction Temperature

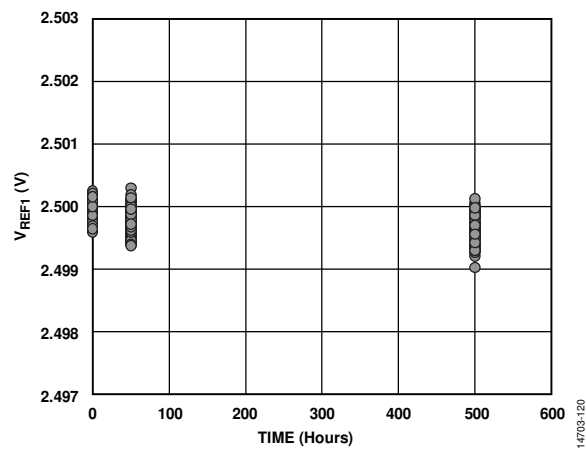


Figure 18. V_{REF1} vs. Time, 0 Hours to 500 Hours Accelerated Lifetime Drift (HTOL)

TERMINOLOGY

Differential Nonlinearity (DNL)

DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity (INL)

INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale (a point 1 LSB below the first code transition) and full scale (a point 1 LSB above the last code transition).

Offset Code Error

Offset code error applies to straight binary output coding. It is the deviation of the first code transition (00 ... 000) to (00 ... 001) from the ideal, that is, AGND + 1 LSB.

Gain Error

Gain error applies to straight binary output coding. It is the deviation of the last code transition (111 ... 110) to (111 ... 111) from the ideal (that is $2 \times V_{REF1} - 1$ LSB) after adjusting for the offset error.

ADC Unadjusted Error

ADC unadjusted error includes INL errors, as well as offset and gain errors of the ADC and measurement channel.

Total Unadjusted Error (TUE)

TUE is the maximum deviation of the output code from the ideal. TUE includes INL errors, offset and gain errors, and reference errors. Reference errors include the difference between the actual and ideal reference voltage (that is, 2.5 V) and the reference voltage temperature coefficient.

Reference Voltage Temperature Coefficient

The reference voltage temperature coefficient (tempco) is derived from the maximum and minimum reference output voltage (V_{REF}) measured between T_{MIN} and T_{MAX} . It is expressed in ppm/°C using the following equation:

$$Tempco\ V_{REF}\ (ppm/^{\circ}C) = \frac{V_{REF\ (MAX)} - V_{REF\ (MIN)}}{2.5\ V \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:

$V_{REF\ (MAX)}$ is the maximum V_{REF} between T_{MIN} and T_{MAX} .

$V_{REF\ (MIN)}$ is the minimum V_{REF} between T_{MIN} and T_{MAX} .

$T_{MAX} = 120^{\circ}C$.

$T_{MIN} = -30^{\circ}C$.

Output Voltage Hysteresis

Output voltage hysteresis, or thermal hysteresis, is defined as the absolute maximum change of the reference output voltage after the device is cycled through temperature from either T_{HYS+} or T_{HYS-} , where

$$T_{HYS+} = 25^{\circ}C \text{ to } T_{MAX} \text{ to } 25^{\circ}C$$

$$T_{HYS-} = 25^{\circ}C \text{ to } T_{MIN} \text{ to } 25^{\circ}C$$

It is expressed in ppm using the following equation:

$$V_{HYS}\ (ppm) = \left| \frac{V_{REF\ (25^{\circ}C)} - V_{REF\ (T_{HYS})}}{V_{REF\ (25^{\circ}C)}} \right| \times 10^6$$

where:

$V_{REF\ (25^{\circ}C)} = V_{REF}$ at $25^{\circ}C$.

$V_{REF\ (T_{HYS})}$ is the maximum change of V_{REF} at T_{HYS+} or T_{HYS-} .

Static Leakage Current

Static leakage current is the current that is measured on the cell voltage and/or the auxiliary ADC inputs when the device is static, that is, not converting.

Dynamic Leakage Current

Dynamic leakage current is the current measured on the cell voltage and/or the auxiliary ADC inputs, when converting, with the static leakage current subtracted. The dynamic leakage current is specified with a convert start command issued every 100 ms. Calculate the dynamic leakage current for a different conversion using the following equation:

$$I_{DYN\ (B)} = \left| \frac{I_{DYN\ (A)} \times f_{CNVST\ (B)}}{f_{CNVST\ (A)}} \right|$$

where:

$I_{DYN\ (B)}$ is the dynamic leakage at the desired convert start frequency, $f_{CNVST\ (B)}$.

$I_{DYN\ (A)}$ is the dynamic leakage at convert start frequency, $f_{CNVST\ (A)}$.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7284 is a Li-Ion battery monitoring device that can monitor eight series connected Li-Ion battery cells and four additional voltage inputs.

The AD7284 consists of a primary measurement path and a secondary measurement path, allowing the host microcontroller to perform a comparison of the two sets of acquired data.

Take the V_{DD} and V_{SS} supplies required by the AD7284 from the battery cells being monitored by the device. An internal V_{REG5} rail is generated to provide power for the internal AD7284 core.

The AD7284 includes two on-chip 2.5 V reference output voltages, V_{REF1} and V_{REF2} . Additionally, the V_{REFBUF} analog output voltage provides a buffered version of the V_{REF1} primary reference to allow the connection of external thermistors and to provide a ratiometric temperature measurement using the four primary auxiliary inputs, VPAUX1 to VPAUX4.

The primary measurement path consists of a voltage input multiplexer and a successive approximation register (SAR) ADC, providing 14 bits of resolution. The primary analog voltage inputs, VPIN0 to VPIN8, with a set of external filtering components, allow the individual voltage monitoring of eight cells, plus a stack voltage measurement. The primary auxiliary inputs, VPAUX1 to VPAUX4, can monitor temperatures or be used for external diagnostics. The primary measurement path also measures V_{REG5} , V_{REF2} , and the internal temperature sensor. The V_{REF2} measurement allows the host microcontroller to verify the operation of the primary measurement path.

The secondary measurement path consists of a voltage input multiplexer and a SAR ADC providing 10 bits of resolution. The secondary analog voltage inputs, VSIN0 to VSIN8, allow a second set of voltage measurements on the eight cells. The secondary analog voltage inputs can connect with a second set of external filtering components, or these inputs can connect directly to VPIN0 to VPIN8 on the primary measurement path to minimize the use of external components, if desired. The secondary measurement path also measures V_{REG5} and V_{REF1} . The V_{REF1} measurement allows the host microcontroller to verify the operation of the secondary measurement ADC.

The AD7284 provides eight outputs to control external transistors as part of a cell balancing circuit. The CB1 to CB5 outputs provide a 0 V to 5 V output voltage referenced to the absolute voltage of the negative terminal of the battery cell that is being balanced. The CB6 to CB8 outputs provide a 0 V to -5 V output voltage referenced to the absolute voltage of the positive terminal of the battery cell that is being balanced.

The AD7284 features a differential daisy-chain interface. A chain of AD7284 devices can monitor the cell voltages and temperatures of a larger number of cells, as shown in Figure 19. The conversion data from each AD7284 in the chain passes through the master device to the system controller via a single SPI interface. Control data can be similarly passed via the single SPI interface to the master AD7284 device and up the differential daisy-chain interface to each individual AD7284 device in the daisy chain.

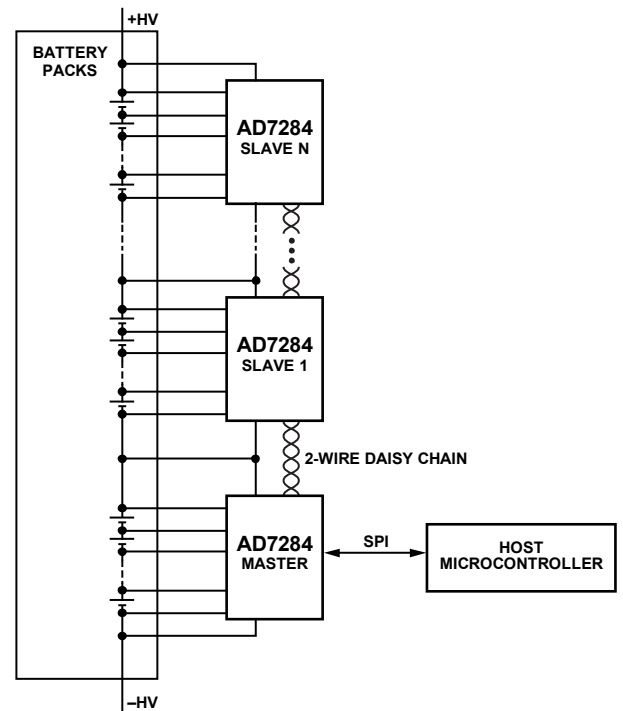


Figure 19. Simplified System Diagram with Multiple AD7284 Devices
(Additional Circuitry Omitted for Clarity)

The AD7284 also has a V_{DRIVE} feature to control the voltage at which the serial interface operates. V_{DRIVE} allows the AD7284 to interface to both the 3.3 V and the 5 V processors.

In the event of communication loss, a watchdog timer places the unresponsive devices in the chain into power-down mode.

CONVERTER OPERATION

The primary and secondary conversion paths of the AD7284 each consist of an input multiplexer and a SAR ADC.

Multiplexer Configuration

Each multiplexer selects a pair of analog inputs to convert: VPIN0 to VPIN8 for the primary path and VSIN0 to VSIN8 for the secondary path. The voltage of each individual cell is measured by converting the difference between the adjacent analog inputs, that is, VPIN1 – VPIN0, VPIN2 – VPIN1, and so on (see Figure 20 and Figure 21).

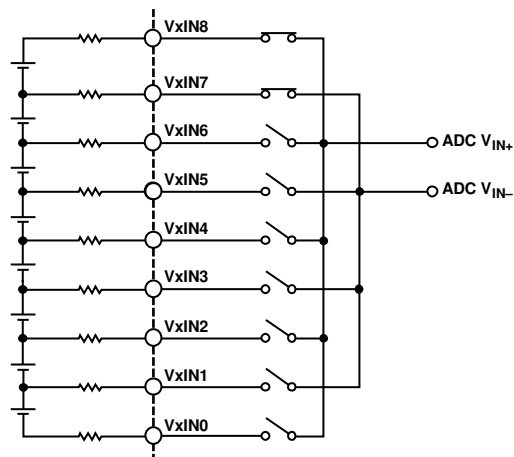


Figure 20. Multiplexer Configuration During VxIN8 to VxIN7 Sampling (Cell 8)

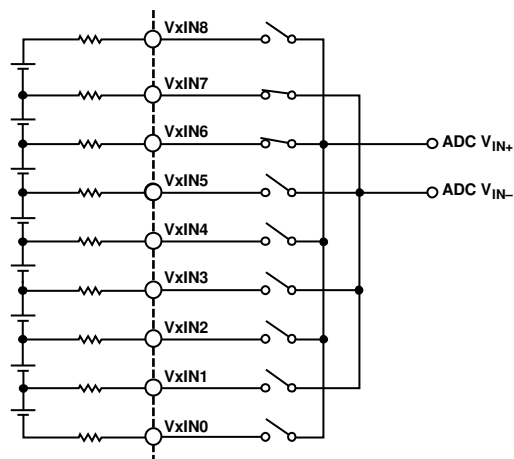
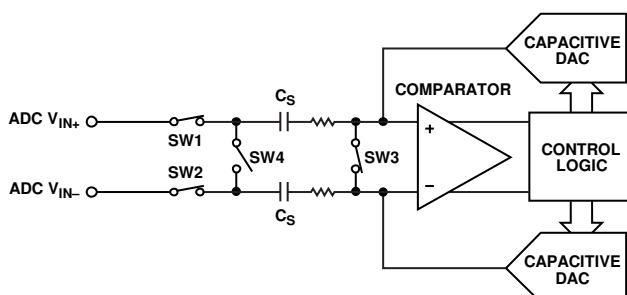


Figure 21. Multiplexer Configuration During VxIN7 to VxIN6 Sampling (Cell 7)

Converter Configurations

The two converters on the AD7284 are SAR ADCs. They are composed of a comparator, SAR control logic, and two capacitive digital-to-analog converters (DACs).

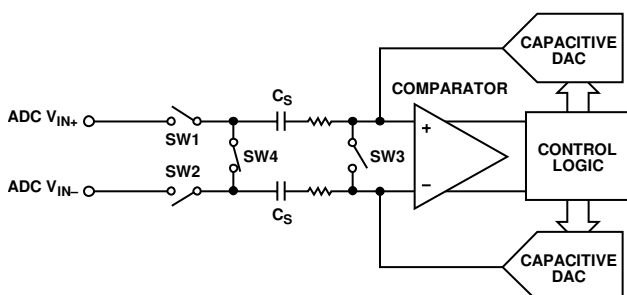
Figure 22 shows a simplified schematic of the SAR ADC. During the acquisition phase, the SW1, SW2, and SW3 switches are closed. The sampling capacitor array, C_S , acquires the signal on the input during this phase.



NOTES
1. THE CONVERTER INPUTS ARE ADC V_{IN+} AND ADC V_{IN-}.

Figure 22. SAR ADC Configuration During the Acquisition Phase

When the ADC starts a conversion, SW1, SW2, and SW3 open, and SW4 closes, causing the comparator to become unbalanced (see Figure 23). The control logic and capacitive DACs add and subtract fixed amounts of charge to return the comparator to a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. This output code is then stored in the appropriate register for the converted input.



NOTES
1. THE CONVERTER INPUTS ARE ADC V_{IN+} AND ADC V_{IN-}.

Figure 23. SAR ADC Configuration During the Conversion Phase

Transfer Function

The conversion data readback for each voltage measurement consists of 14 bits. The output coding of the AD7284 primary measurement path is in 14-bit, straight binary format. The output coding of the AD7284 secondary measurement path is in 10-bit, straight binary format. The result is inverted so that it is easily distinguished from the primary measurement and is preceded by four data bits set to 0000.

The LSB size is dependent on whether the primary measurement path or the secondary measurement is used. The analog input range of the voltage inputs is 0 V to 5 V. The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSBs, and so on). The ideal transfer characteristic is shown in Figure 24.

Table 7. LSB Size for the Analog Input Range

Measurement Path	Input Range	Full-Scale Range ¹	LSB Size
Primary	0 V to 5 V	5 V/16,384	305 μ V
Secondary	0 V to 5 V	5 V/1,024	4.88 mV

¹ The 16,384 and 1,024 values in this column represent the number of codes available for each ADC.

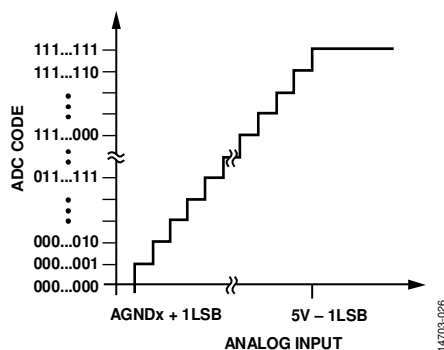


Figure 24. Ideal Transfer Characteristic

INTERNAL TEMPERATURE SENSOR

The AD7284 contains an on-chip temperature sensor. The temperature measurement updates with each conversion request and is provided as part of each conversion frame.

The temperature sensor measures the junction temperatures in the -30°C to $+120^{\circ}\text{C}$ range with a typical accuracy of $\pm 3^{\circ}\text{C}$.

The output coding of the temperature sensor is twos complement, with a resolution of 32 LSB/ $^{\circ}\text{C}$. Code 0 corresponds to 25°C (junction temperature).

AUXILIARY ADC INPUTS

The AD7284 provides four single-ended analog inputs to the primary ADC, VPAUX1 to VPAUX4. The input voltage range is 0 V to 5 V with respect to V_{SS} . These inputs can convert other voltages within the system, such as converting the voltage output of a thermistor temperature measurement circuit.

VOLTAGE REFERENCES

The AD7284 contains two identical 1.2 V band gap voltage references. These references are internally buffered and gained to provide 2.5 V reference voltages to the primary (V_{REF1}) and secondary (V_{REF2}) ADCs, as shown in Figure 25.

The provision of two reference voltages is a diagnostic feature and enables validation of the behavior of the measurement paths and the references. For example, the secondary ADC measures the primary reference, V_{REF1} . Similarly, the primary ADC measures the secondary reference, V_{REF2} .

An external 2.5 V reference can overdrive the reference for the primary path, V_{REF1} . When an external reference is used, set Bit D4 of Control Register 1 to disable the V_{REF1} buffer. The secondary measurement path measures the external reference in this case.

The primary reference is further buffered and provided as a reference output, V_{REFBUF} , to bias external thermistors. This buffer is capable of driving currents up to 1 mA, allowing the user to connect up to four 10 k Ω thermistor circuits in parallel. The primary conversion includes a measure of this voltage level.

Decouple the V_{REFBUF} pin to ADCGND1 using a 1 μ F capacitor. Decouple the V_{REF1} pin to ADCGND1 using a 1 μ F capacitor with a 100 nF capacitor in parallel. Decouple the V_{REF2} pin to ADCGND2 using a 1 μ F capacitor with 100 nF capacitor in parallel.

Larger decoupling capacitors can be used to decouple V_{REF1} and V_{REF2} ; however, this results in the reference taking longer to power up. The turn on settling time is typically 5 ms with the recommended decoupling capacitor values.

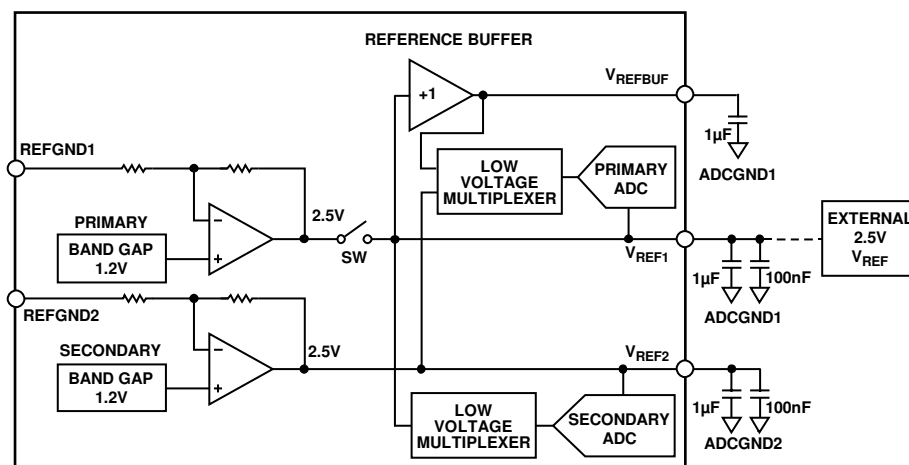


Figure 25. Internal References and Optional External Reference

CELL CONNECTIONS

The AD7284 can monitor four to eight battery cells connected in series.

Typical Eight Cell Configuration

Figure 26 shows the typical connections to the AD7284 supply and cell monitoring inputs in an eight cell configuration.

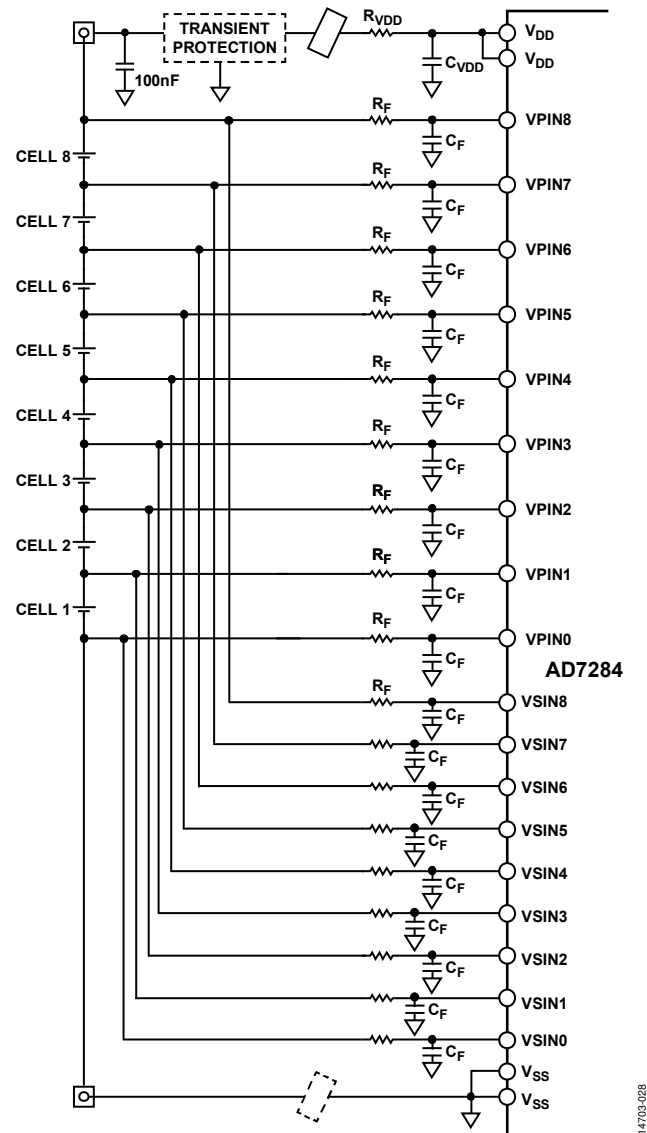


Figure 26. Typical Cells and Supply Connections (Additional Circuitry Omitted for Clarity)

A series resistor, R_{VDD} (10 Ω to 40 Ω), is recommended from the top of the battery into the V_{DD} supply pins. The total decoupling capacitors on the supply pins, C_{VDD} , must be 4.7 μF .

The analog voltage inputs must be filtered externally with a single-ended low-pass filter approach. The resistors, R_F , in series with the $VPIN0$ to $VPIN8$ and $VSIN0$ to $VSIN8$ inputs provide protection for the analog inputs in the event of an overvoltage or undervoltage condition on those inputs (for example, if any of the cell voltage inputs are incorrectly shorted to V_{DD} or V_{SS}). The resistors also provide protection during the initial connection of the daisy chain of AD7284 devices to the battery stack. The C_F capacitors, in conjunction with the R_F resistors, act as a low-pass filter. C_F capacitor values between 100 nF and 1 μF are recommended. The cutoff frequency of the low-pass filter when using an R_F of 1 k Ω and a C_F capacitor of 1 μF is 160 Hz. The cutoff frequency of the low-pass filter when using a C_F capacitor of 100 nF is 1600 Hz.

The time constant of the R_F and C_F filters on the primary and secondary paths must match the time constant on the V_{DD} pins fairly closely (for example, 100 nF (C_F) and 1 k Ω (R_F) on the inputs, and 4.7 μF (C_{VDD}) and 20 Ω (R_{VDD}) on V_{DD}).

Connection to Fewer Voltage Cells

While the AD7284 provides eight input channels for battery cell voltage measurement, it can also be used in applications that require fewer than eight cell voltage measurements. When used in this manner, ensure that the sum of the individual cell voltages still exceeds the minimum V_{DD} supply voltage (10 V).

The minimum number of cells connected to each AD7284 is four. Figure 27 shows the recommended connections to monitor four cells. The unused inputs are connected together and connected between Cell 2 and Cell 3 via a resistor. The resistor minimizes the leakage from the unused inputs.

Irrespective of how many cells are connected, the AD7284 acquires and converts all eight voltages. All conversion results are available for readback; results of the unused voltage channels are zero.

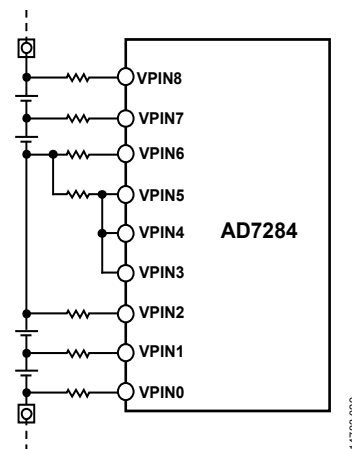


Figure 27. Typical Connection with Minimum Cells Connected (Additional Circuitry Omitted for Clarity)

Connection of Unused Secondary Channel Inputs

In applications where the secondary path is not used, connect the VSINx pins directly to the corresponding VPINx pins.

By default, the two ADCs convert simultaneously. To minimize the discharge of the C_F capacitor during the acquisition phase, enable the delay mode between conversions. The ADC delay mode is controlled by Control Register 3, Bit 6.

Acquisition Time

The time required to acquire an input signal depends on how quickly the sampling capacitor is charged. This, in turn, depends on the input impedance and any external components placed on the analog inputs. The default acquisition time of the AD7284 on initial power-up is 400 ns. To accommodate the use of alternative input filter configurations, the acquisition time can be set to 400 ns, 800 ns, 1600 ns, or 3200 ns using Bits[D1:D0] in Control Register 2 (see Table 22).

Calculate the minimum acquisition time required, t_{ACQ} , by

$$t_{ACQ} = 10 \times ((R_{SOURCE} + R) \times C)$$

where:

R_{SOURCE} includes any extra source impedance on the analog input between the external capacitors and the input pins. It does not include any extra source impedance, for example, the 1 k Ω series resistors, which are between the battery cells and the external capacitors.

R is the internal switch and path resistance, typically 620 Ω .

C is the sampling capacitance, typically 15 pF.

ADC CONVERSIONS SEQUENCE

Upon completion of a conversion sequence, the primary and secondary path measurements are available for read back. The primary path measurements must be read first. Reading the secondary path measurements is optional.

The primary path consists of 18 measurements available in the following order:

1. Cell Voltage 1 to Cell Voltage 8.
2. Stack voltage scaled down by 16.
3. Secondary path reference voltage.
4. V_{REG5} voltage scaled by 2/3.
5. Primary Auxiliary Input 1 to Primary Auxiliary Input 4.
6. Reference buffer output voltage.
7. Repeated V_{REG5} voltage scaled by 2/3.
8. Internal temperature sensor.

All 18 measurements must be read back on each device as described in the Conversion Data Readback section.

The secondary path consists of 10 measurements available in the following order:

1. Cell Voltage 1 to Cell Voltage 8.
2. Primary path reference voltage.
3. V_{REG5} voltage scaled by 4/5.

To read back one measurement from the secondary path, all 10 measurements must be read back for each device (see the Conversion Data Readback section).

The results are read back via the 4-wire SPI.

Internal Voltage Measurements

Table 8 and Table 9 show the range of the expected measured reference values that are returned on each measurement cycle. Detecting one of these values outside of the indicated range indicates a fault condition.

Table 8. Primary Internal Voltage Measurement

Parameter	Min	Max	Unit	Register
V_{REF2}	2.485	2.515	V	0x12
$V_{REG5} \times 2/3$	3.200	3.421	V	0x13
V_{REFBUF}	2.486	2.514	V	0x1C
$V_{REG5} \times 2/3$	3.200	3.421	V	0x1D

Table 9. Secondary Internal Voltage Measurement

Parameter	Min	Max	Unit	Register
V_{REF1}	2.475	2.525	V	0x31
$V_{REG5} \times 4/5$	3.865	4.135	V	0x34

CONVERTING WITH A SINGLE AD7284

Conversions are initiated on the AD7284 by setting Bit D0 high in the ADC functional control register. A single conversion command initiates conversions on all channels of the AD7284. The conversions on the primary measurement path and the secondary measurement path occur in parallel, as shown in Figure 28. As described in the Converter Operation section, the voltage of each individual battery cell is measured by converting the difference between the adjacent analog inputs. The first conversion starts t_{START} after the conversion start command. This conversion is a dummy conversion that has the same timing as a normal conversion and provides additional acquisition time for the first cell conversion. The first cell converted is Cell 8 (VPIN8 – VPIN7), then Cell 7 (VPIN7 – VPIN6), and so on, as shown in Figure 28.

Calculate the conversion time per channel by

$$\text{Conversion Time per Channel} = t_{ACQ} + t_{CONV}$$

Similarly, calculate the conversion time for eight cell voltages by

$$\text{Conversion Time per Eight Primary Cells} = (t_{ACQ} + t_{CONV}) \times 9$$

where the 9th conversion is the dummy conversion.

The device conversion time includes the internal temperature sensor channel, which requires a longer acquisition and conversion time (typically 276 μ s). Therefore, calculate the conversion time per device by

$$\text{Conversion Time per Device} = t_{START} + ((t_{ACQ} + t_{CONV}) \times 18) + 276 \mu\text{s}$$

where:

t_{START} is the time between the rising edge of $\overline{CS}$ to the dummy conversion. See Table 2.

t_{ACQ} is the analog input acquisition time. See Table 2.

t_{CONV} is the conversion time. See Table 2.

Factor 18 is the one dummy conversion plus seventeen measurements.

With an acquisition time set to 400 ns, the conversion time per device is typically 336 μ s.

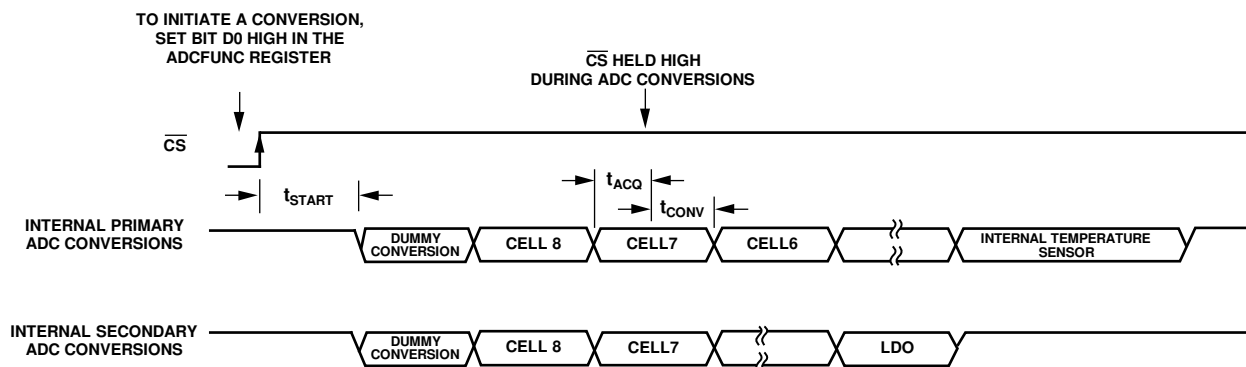


Figure 28. ADC Conversions with a Single Device

147703-030

CONVERTING WITH A CHAIN OF AD7284 DEVICES

The AD7284 provides a daisy-chain interface that allows up to 30 AD7284 devices to stack. One feature of the daisy-chain interface is the ability to initiate conversions on all devices in the daisy-chain stack with a single convert start command. The convert start command transfers up the daisy chain from the master device to each AD7284 in turn. The delay time between each AD7284 is t_{DELAY} , as shown in Figure 29. Note that this diagram is simplified to show the primary measurement path only.

Calculate the total conversion time for all channels by

$$\text{Total Conversion Time} = (\text{Conversion Time per Device}) + ((N - 1) \times t_{\text{DELAY}})$$

where:

N is the number of AD7284 devices in the daisy chain.

t_{DELAY} is the delay time when transferring the convert start command between adjacent AD7284 devices, as specified in Table 2.

The latency across all cells is the delay between the start of converting the first cell and the start of converting on the last cell of a battery stack, as shown in Figure 30. Calculate this latency by

$$\text{Latency Across All Cells} = (\text{Conversion Time of Seven Cells}) + ((N - 1) \times t_{\text{DELAY}})$$

With an acquisition time set to 400 ns, the latency across 96 cells is typically 13 μs .

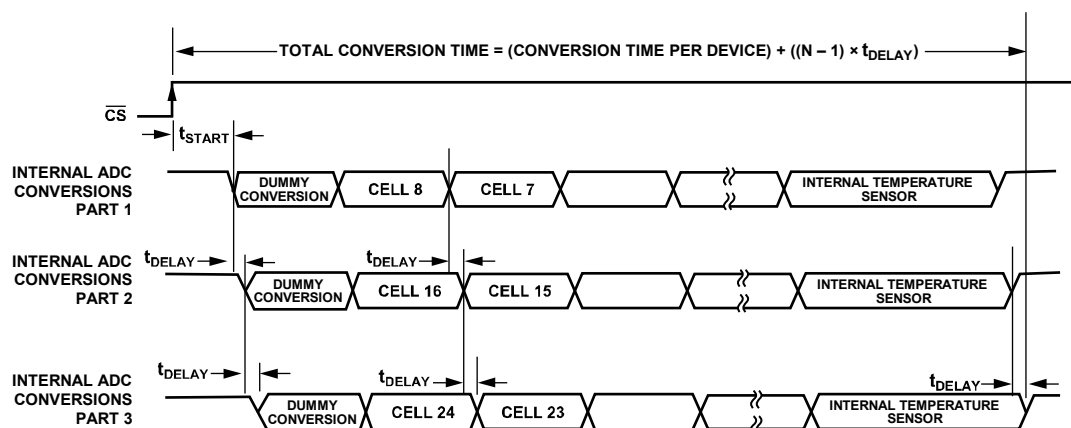


Figure 29. ADC Conversions with a Chain of Three Devices

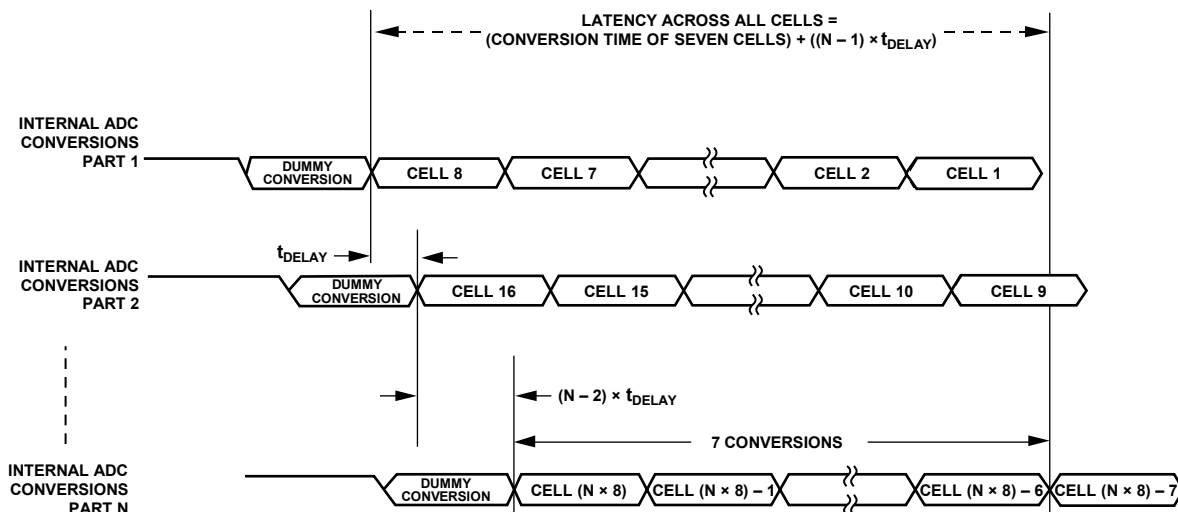


Figure 30. Latency Across All Cells

CONVERSION DATA READBACK

A sequence with ADC conversions and a readback operation is shown in Figure 31. The user issues a command to the device to start the conversion. The conversion data is available for read back when the channel acquisition and conversion times complete. The data returned from a conversion results readback operation is contained within multiple 64-bit packs, as described in the Conversion Data Readback Operation section.

Following a conversion, the primary conversion data for all devices in the daisy chain is available for readback. To enable secondary conversion data readback, a command is issued as shown in Figure 32. This is the only 32-bit command that can be issued while in 64-bit mode.

The sequence to read back primary and secondary data is described in the Example 5: Convert and Read All Conversion Data section.

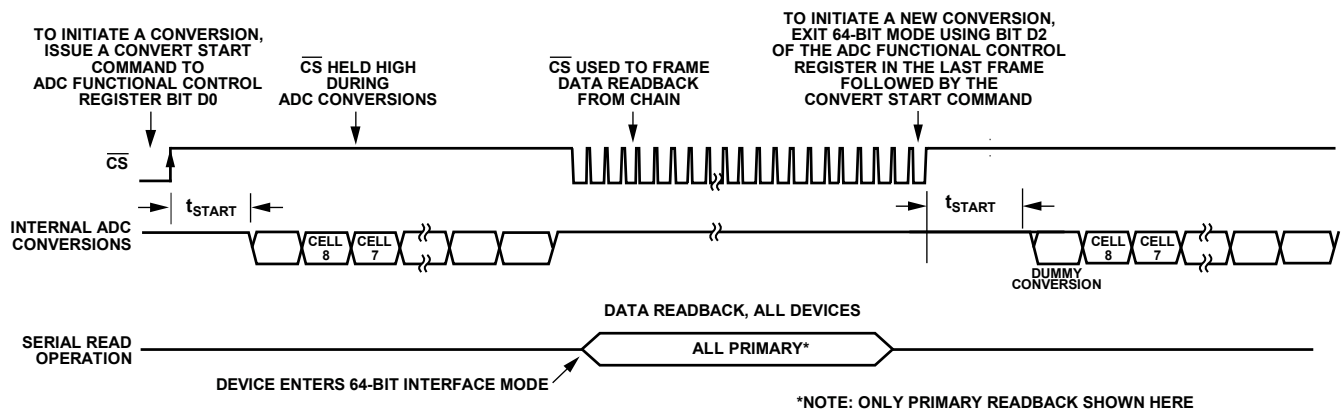


Figure 31. ADC Conversions and Readback of Primary Data and Initiation of a Second Conversion

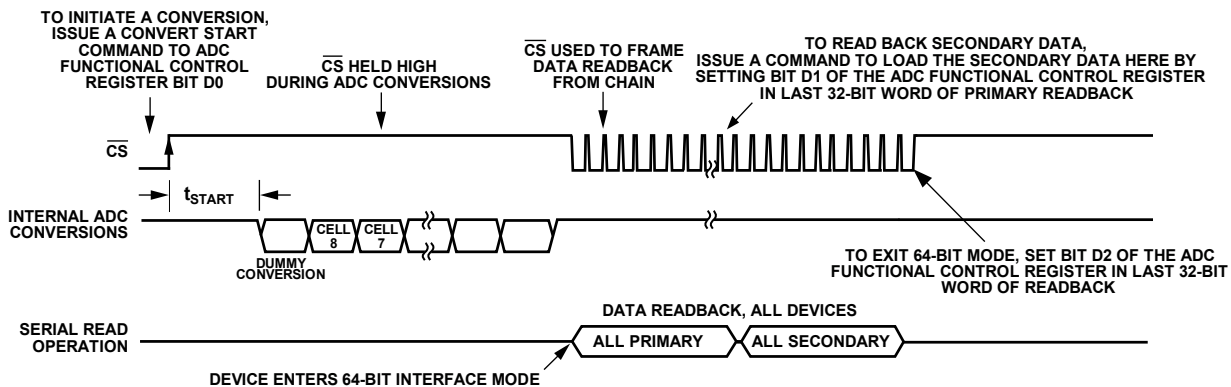


Figure 32. ADC Conversions and Readback of Primary and Secondary Data and Exit of 64-Bit Readback Mode

CELL BALANCING OUTPUTS

The AD7284 provides eight cell balance outputs that can drive the gates of the external transistors as part of a cell balancing circuit. The cell balance feature can be used while converting cell voltage measurements; however, the accuracy of the conversions degrades. Cell balancing is also available while the AD7284 is in partial power-down mode.

Cell Balance Connections

As shown in Figure 33, five of the cell balance outputs (CB1 to CB5) are capable of driving an N channel, metal oxide semiconductor field effect transistor (MOSFET), while the other three (CB6 to CB8) drive a P channel MOSFET. These outputs are designed to drive 20 μA (typical) into the external FET, enabling turn on within 100 μs .

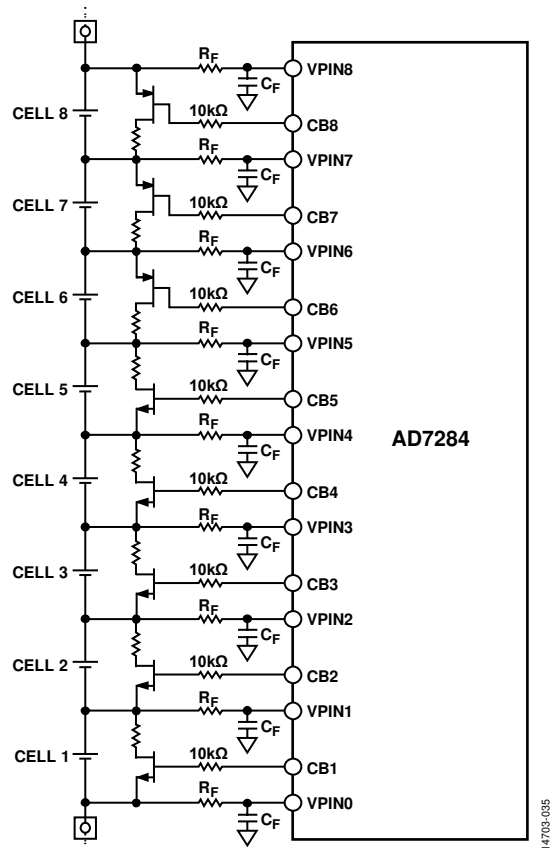


Figure 33. Cell Balancing Configuration

In an application with two or more AD7284 devices in a directly connected daisy chain, it is recommended to place 10 k Ω series resistors between the CBx outputs of the AD7284 and the gates of the external cell balancing transistors. These resistors, in conjunction with the internal 5 V clamps, help protect the CBx outputs and gates of the external cell balancing transistors during the initial connection of the monitoring circuitry to the battery stack.

The simplified internal configuration of the cell balance circuit (CB1 to CB5) is shown in Figure 34.

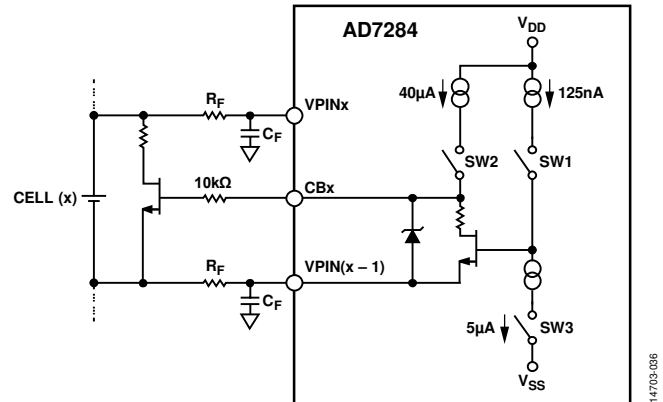


Figure 34. Simplified Internal Configuration of the Cell Balancing Circuit (CB1 to CB5)

When cell balancing is disabled, SW1 is closed, SW2 and SW3 are open, the negative channel metal oxide semiconductor (NMOS) switch is on, and the CBx pin is pulled to VPIN(x - 1). When enabled, SW1 is open, SW2 and SW3 are closed, the NMOS switch is off, and the CBx voltage increases as current charges the gate of an external FET. The internal clamp ensures that CBx stays within approximately 5 V of VPIN(x - 1) and provides a path for some of the 40 μA out of VPIN(x - 1), which causes a voltage drop on VPIN(x - 1). The voltage drop depends on the value of the input resistor. CB6 to CB8 use an equivalent positive channel metal oxide semiconductor (PMOS) circuit.

Cell Balance Outputs Interface

Three bits are used to control the cell balancing feature:

- The cell balance power-down bit, CBPDB, in Control Register 1 (see Table 21) controls the cell balance output drivers. The default value of this bit at power-up is 0, and the drivers are disabled. Turn off the drivers when cell balancing is not used to reduce power consumption and maintain accuracy on cell monitoring.
- The general output enable bit, GOE_CB, in Control Register 3 (see Table 24) allows the host microcontroller/DSP to control the state of all cell balance outputs with one write command while still maintaining the current state of the cell balance control register. The default value of this bit at power-up is 0, which corresponds to the cell balance outputs off state.
- The cell balance bits, CBx, in the cell balance control register (see Table 26) allow the user to individually configure the state of the cell balance output. The default value of this register at power-up is 0x00, and each of the cell balance outputs are disabled.

To enable cell balancing on one or multiple cells, the CBPDB bit, the GOE_CB bit, and the corresponding CBx bit(s) must be set to 1.

Programmable On Time

To enable individual programmable on times, activate the corresponding CBx output(s) as described in the Cell Balance Outputs Interface section. Programming an on time for a disabled CBx output has no effect.

The AD7284 offers eight cell balance timer (CBTx) registers to individually program the on time of the CBx output pins. On times of 0 minutes (the output stays turned on) to 8.5 hours can be programmed with a two minute resolution. All CBTx registers are 0x00 by default. The values programmed in the CBTx registers are compared with a single timer. The default value of the timer is 0x00. The current value of the timer is available in the current cell balance count state (CBCNT) register.

The timer starts from 0x00 when a CBTx register is written to. When the value in the timer reaches the value of any of the CBTx registers, the corresponding CBx output is switched off. The timer stops when the largest value programmed in the enabled CBTx registers is equal to the timer. CBTx registers settings are maintained following a timeout event.

The timer restarts from 0x00 on a write to any of the active CBTx registers. Writing zero causes the corresponding cell balance output to switch off and the timer to restart. A write to the CBCTRL register while the timer is active causes the timer to restart from 0x00. The CBCNT register can adjust the values of previously enabled cell balance timers. Individual or all CBx output(s) can be switched off before the timer reaches its or their programmed value(s) by disabling the CBx output(s) as described in the Cell Balance Outputs Interface section.

The cell balance timer is independent of the power-down timer. Use the power-down timer to allow cell balancing to occur for a set time before powering down the AD7284.

Note that the power-down timer can be used instead of the watchdog timer when using the cell balancing timer to prevent the need to service the watchdog timer.

OPEN INPUT DETECTION

Two methods are available to detect an open wire condition between the cell and an ADC's input pin: open input sense and cell balance sense. These methods require the use of the secondary path and independent filters on the ADC inputs.

The host controller initiates the diagnostic request. It then reads back conversion results from primary and secondary inputs from which it is possible to determine an open input condition.

Open Input Sense

The open input sense (OIS) technique allows the detection of an open wire at the board edge or at the device input.

When enabled, the OIS diagnostics cause a small current to sink (or source, in the case of VPIN0 and VSIN0) from the selected primary or secondary voltage sense pin. A delay is also introduced between the primary and secondary conversions. If an input wire disconnects, the OIS current sources from or sinks into the input filter capacitor, causing the input voltage to shift. This shift is seen as a difference between the primary and secondary measurements.

The size of the voltage shift depends on the size of the input filter capacitor, the delay between primary and secondary measurements (1000 μ s), and the OIS current (100 μ A).

For a 100 nF filter capacitor, a shift of 500 mV is expected. If the input pins are connected correctly, a voltage drop of approximately 100 mV is measured between the primary and secondary inputs when using a 1 k Ω input resistor, R_F .

Cell Balance Sense

An alternative method is using the cell balance function. This technique is useful for detecting board edge open wire conditions. When enabled, a cell balance FET that is off for the first conversion is switched on for the second conversion. If the input wire disconnects, the enabled FET causes the input that disconnected to pull toward the pin on the opposite side of the enabled FET.

Sequence of Operations

To perform an open wire diagnostic on an input, use the following procedure:

1. Enable the OISx bit for the cell connection under investigation using the OISCTRL control register and/or the OISGPOP control register, or set the appropriate cell balance enable bit in the cell balance control register.
2. In the Control 3 register, select the appropriate input sense function via the IN_SNSE bits, set the ADC delay bit (ADCDLY), and select the conversion order with the ADCORDR bit. If not in delay mode, the GOE_x bits gate the respective cell balance or the OISCTRL register settings.
3. Set the CBPDB bit in Control Register 1 for the cell balance method.
4. Initiate a conversion and read back the primary and secondary data.

POWER MANAGEMENT

AD7284 SUPPLIES

The AD7284 is powered from the cell stack. The device connects to the cell stack positive terminal (+HV) through the V_{DD} pin and the cell stack negative terminal (–HV) through the V_{SS} pin. An internal regulator generates a 5 V supply (V_{REG5}) for the internal core of the AD7284, as shown in Figure 35.

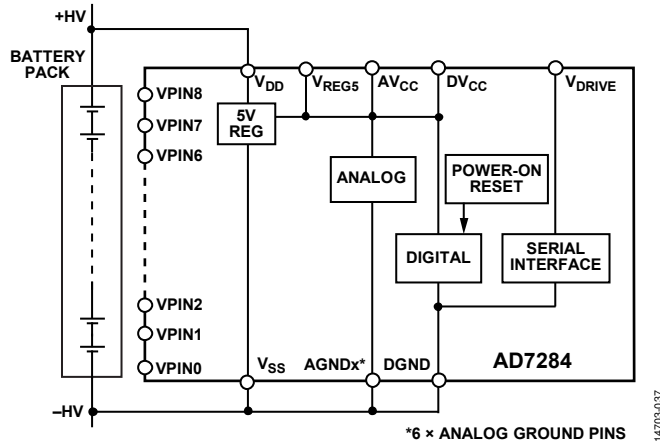


Figure 35. Power Supply Overview (External Circuitry Omitted for Clarity)

A total decoupling capacitance of 4.7 μ F is recommended on the V_{DD} pins. Optionally, use 2.2 μ F in parallel with 100 nF on each of the V_{DD} pins.

It is required that 100 nF be present on the regulator output pin, V_{REG5}, and on each of the low voltage supplies, AV_{CC} and DV_{CC}. Connect these three pins together on the PCB.

V_{DRIVE}

For the master device only, an external V_{DRIVE} supply is required to power the digital input/output pins to ensure interface compatibility with host supplies operating at 3.3 V or 5 V. Therefore, do not drive the digital input pins when V_{DRIVE} is low.

V_{DRIVE} is also an integral part of the power-up/power-down scheme within the AD7284, as described in the Active Mode, Power-Up section and the Power-Down section. Pulling V_{DRIVE} low places the AD7284 into the lowest power mode, unless an active power-down timer is running.

A 100 nF decoupling capacitor is recommended on the V_{DRIVE} pin for the master device only.

On slave devices, connect V_{DRIVE} directly to V_{REG5} at all times. In this configuration, all currents supplied by the low voltage pins, such as V_{REFBUF}, GPOP1, and GPOP2, are supplied by the internal regulator. This regulator delivers 2 mA typically for use external to the AD7284.

MODES OF OPERATION

The three modes of operation for the AD7284 include the following: active mode (power-up), software partial power-down mode, and hardware full power-down mode.

In active mode, the AD7284 can be idle or perform the following tasks:

- ADC conversions.
- Conversion data readback.
- Register read and write.
- Cell balancing (cell balancing and register reads or writes, can also be performed in partial power-down mode).

The current consumption is specified in Table 1.

ACTIVE MODE, POWER-UP

Connect the V_{DRIVE} pin on the AD7284 master device to an external voltage supply. A rising edge on the V_{DRIVE} supply signals the AD7284 master device to power up. If V_{DRIVE} is already held high, an alternate method of powering up the master is via a pulse of 100 ns minimum on the RESET pin.

Power-Up Time

The time required for an AD7284 master device to power up and to receive SPI communications is typically 200 μ s with a total capacitance of 300 nF on V_{REG5} (100 nF on each pin). The time required to perform accurate ADC conversions is typically 5 ms. These figures apply when V_{REF1} and V_{REF2} are decoupled with a 1 μ F in parallel with 100 nF.

The AD7284 slave devices power up through a slave wake-up signal that is automatically transmitted through the daisy chain. The master device transmits the slave wake-up signal to the first slave device, the first slave device transmits the wake-up signal to the device above it in the daisy chain, and so on. Each device transmits a slave wake-up signal typically within 100 μ s of receiving its own wake-up signal. The time required for a slave device to power up and perform accurate ADC conversions is typically 5 ms (see Figure 36).

Calculate the total power-up time for a chain of AD7284 devices connected in the direct current configuration by

$$\text{Total Power-Up Time} = 5 \text{ ms} + ((N - 1) \times 100 \mu\text{s})$$

where N is the number of AD7284 devices in the daisy chain.

Connect the V_{DRIVE} pin on each slave device to its own V_{REG5} pin.

Multiple dummy register writes are required to wake up the chain in a configuration with an isolated daisy chain.