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Quad 2:1 Multiplexer/ Demultiplexer Bus Switch

The ON Semiconductor 74FST3257 is a quad 2:1, high performance multiplexer/demultiplexer bus switch. The device is CMOS TTL compatible when operating between 4 and 5.5 Volts. The device exhibits extremely low R_{ON} and adds nearly zero propagation delay. The device adds no noise or ground bounce to the system.

Features

- $R_{ON} < 4 \Omega$ Typical
- Less Than 0.25 ns-Max Delay Through Switch
- Nearly Zero Standby Current
- No Circuit Bounce
- Control Inputs are TTL/CMOS Compatible
- Pin-For-Pin Compatible With QS3257, FST3257, CBT3257
- All Popular Packages: SOIC-16, TSSOP-16, QFN16
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

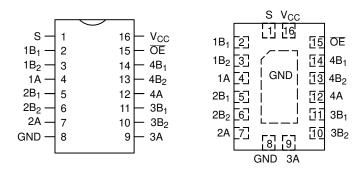


Figure 1. 16-Lead Pinout Diagrams

S	ŌĒ	Function
Х	Н	Disconnect
L	L	A = B ₁
Н	L	A = B ₂

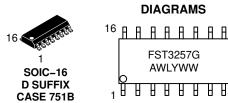
Figure 2. Truth Table

1

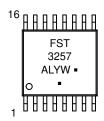


ON Semiconductor®

www.onsemi.com







MARKING





A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or = Pb-Free Package
(Note: Microdot may be in either location)

PIN NAMES

Pin	Description
\overline{OE}_1 , \overline{OE}_2	Bus Switch Enables
S ₀ , S ₁	Select Inputs
А	Bus A
B ₁ , B ₂ , B ₃ , B ₄	Bus B

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

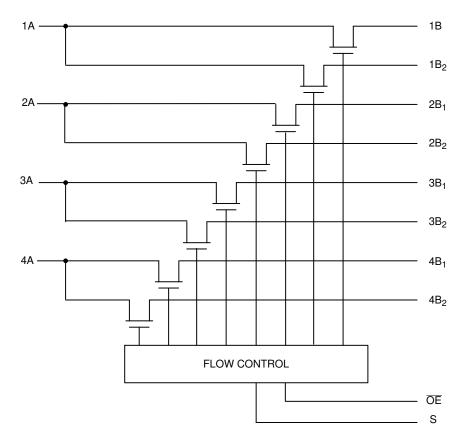


Figure 3. Logic Diagram

ORDERING INFORMATION

Device Order Number	Package	Shipping [†]
74FST3257DR2G	SOIC-16	2500 Unite / Tone 9 Deel
NLV74FST3257DR2G*	(Pb-Free)	2500 Units / Tape & Reel
74FST3257DTR2G	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel
74FST3257MNTWG	QFN16 (Pb-Free)	3000 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging

Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.

MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
VI	DC Input Voltage	-0.5 to +7.0	V
Vo	DC Output Voltage	-0.5 to +7.0	V
I _{IK}	DC Input Diode Current VI < GND	-50	mA
l _{OK}	DC Output Diode Current V _O < GND	-50	mA
IO	DC Output Sink Current	128	mA
I _{CC}	DC Supply Current per Supply Pin	±100	mA
I _{GND}	DC Ground Current per Ground Pin	±100	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
TJ	Junction Temperature Under Bias	+150	°C
$\theta_{\sf JA}$	Thermal Resistance SOIC TSSOP QFN	125 170 N/A	°C/W
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	>2000 >200 N/A	V
I _{Latchup}	Latchup Performance Above V _{CC} and Below GND at 85°C (Note 4)	±500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Tested to EIA/JESD22-A114-A.
- 2. Tested to EIA/JESD22-A115-A.
- 3. Tested to JESD22-C101-A.
- 4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V _{CC}	Supply Voltage Operating, Data Retention Only	4.0	5.5	V
VI	Input Voltage (Note 5)	0	5.5	V
V _O	Output Voltage (HIGH or LOW State)	0	5.5	V
T _A	Operating Free-Air Temperature	-40	+85	°C
Δt/ΔV		witch Control Input $_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ 0	DC 5	ns/V

5. Unused control inputs may not be left open. All control inputs must be tied to a high or low logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

			V _{CC}	T _A = -40°C to +85°C		85°C	
Symbol	Parameter	Conditions	(V)	Min	Тур*	Max	Units
V _{IK}	Clamp Diode Voltage	I _{IN} = -18 mA	4.5			-1.2	V
V _{IH}	High-Level Input Voltage		4.0 to 5.5	2.0			V
V _{IL}	Low-Level Input Voltage		4.0 to 5.5			0.8	V
II	Input Leakage Current	0 ≤ V _{IN} ≤ 5.5 V	5.5			±1.0	μΑ
loz	Off-State Leakage Current	$0 \le A, B \le V_{CC}$	5.5			±1.0	μΑ
R _{ON}	Switch On Resistance (Note 6)	V _{IN} = 0 V, I _{IN} = 64 mA	4.5		4	7	Ω
		V _{IN} = 0 V, I _{IN} = 30 mA	4.5		4	7	
		V _{IN} = 2.4 V, I _{IN} = 15 mA	4.5		8	15	
		V _{IN} = 2.4 V, I _{IN} = 15 mA	4.0		11	20	
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND, I _{OUT} = 0	5.5			3	μΑ
Δl _{CC}	Increase In I _{CC} per Input	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5			2.5	mA

AC ELECTRICAL CHARACTERISTICS

			$T_A = -40$ °C to +85 °C $C_L = 50$ pF, RU = RD = 500 Ω				
			V _{CC} = 4	.5–5.5 V	V _{CC} =	4.0 V]
Symbol	Parameter	Conditions	Min	Max	Min	Max	Units
t _{PHL} ,	Prop Delay Bus to Bus (Note 7)	V _I = OPEN		0.25		0.25	ns
t _{PLH}	Prop Delay, Select to Bus A		1.0	4.7		5.2	
t _{PZH} ,	Output Enable Time, Select to Bus B	$V_I = 7 \text{ V for } t_{PZL}$	1.0	5.2		5.7	ns
t _{PZL}	Output Enable Time, I _{OE} to Bus A, B	V _I = OPEN for t _{PZH}	1.0	5.1		5.6	
t _{PHZ} ,	Output Disable Time, Select to Bus B	$V_I = 7 \text{ V for } t_{PLZ}$	1.0	5.2		5.5	ns
t _{PLZ}	Output Disable Time, I _{OE} to Bus A, B	V _I = OPEN for t _{PHZ}	1.0	5.5		5.5	1

^{7.} This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

CAPACITANCE (Note 8)

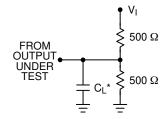
Symbol	Parameter	Conditions	Тур	Max	Units
C _{IN}	Control Pin Input Capacitance	V _{CC} = 5.0 V	3		pF
C _{I/O}	A Port Input/Output Capacitance	V_{CC} , $\overline{OE} = 5.0 \text{ V}$	7		pF
C _{I/O}	B Port Input/Output Capacitance	V_{CC} , $\overline{OE} = 5.0 \text{ V}$	5		pF

^{8.} $T_A = +25$ °C, f = 1 MHz, Capacitance is characterized but not tested.

^{*}Typical values are at V_{CC} = 5.0 V and T_A = 25°C.

6. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Loading and Waveforms



NOTES:

- 1. Input driven by 50 Ω source terminated in 50 $\Omega.$
- 2. CL includes load and stray capacitance.

Figure 4. AC Test Circuit

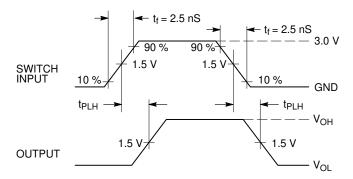


Figure 5. Propagation Delays

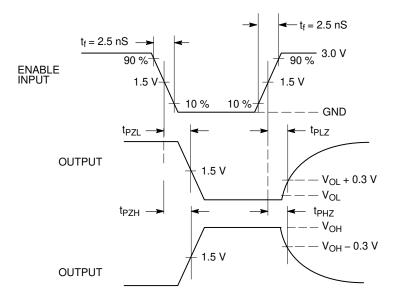
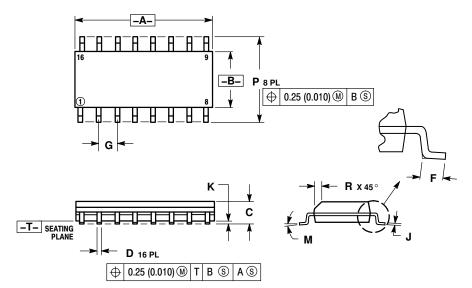


Figure 6. Enable/Disable Delays

 $^{{}^{*}}C_{L} = 50 pF$

PACKAGE DIMENSIONS

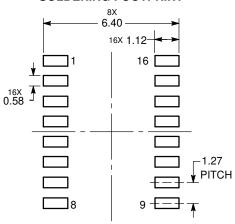
SOIC-16 **D SUFFIX** CASE 751B-05 ISSUE K



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

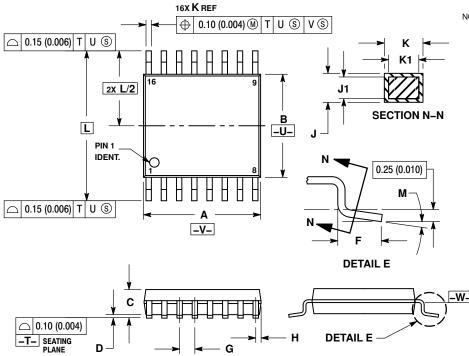
	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	9.80	10.00	0.386	0.393
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT



PACKAGE DIMENSIONS

TSSOP-16 **DT SUFFIX** CASE 948F ISSUE B

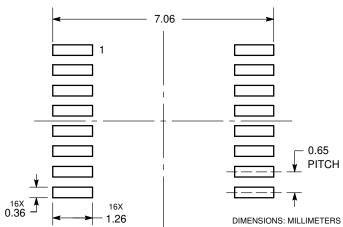


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER
 - 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION. INTERLEAD SUBJECT OF THE SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K

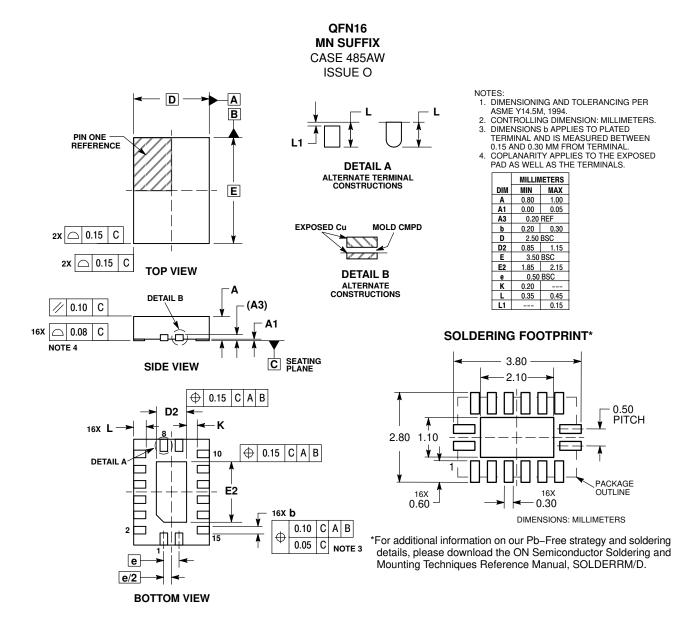
 - (0.003) TOTAL IN EXCESS OF THE K
 DIMENSION AT MAXIMUM MATERIAL CONDITION.
 - 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
C		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026	BSC	
Н	0.18	0.28	0.007	0.011	
7	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40	BSC	0.252 BSC		
М	0°	8°	0°	8°	

SOLDERING FOOTPRINT



PACKAGE DIMENSIONS



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