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ST72561xx-Auto

8-bit MCU for automotive with Flash or ROM,
10-bit ADC, 5 timers, SPI, LINSICI™, active CAN

Features

■ Memories

- 16 K to 60 K High Density Flash (HDFlash) or ROM with read-out protection capability. In-application programming and in-circuit programming for HDFlash devices
- 1 to 2 K RAM
- HDFlash endurance: 100 cycles, data retention 20 years at 55 °C

■ Clock, reset and supply management

- Low power crystal/ceramic resonator oscillators and bypass for external clock
- PLL for 2 x frequency multiplication
- 5 power saving modes: halt, auto wake up from halt, active halt, wait and slow

■ Interrupt management

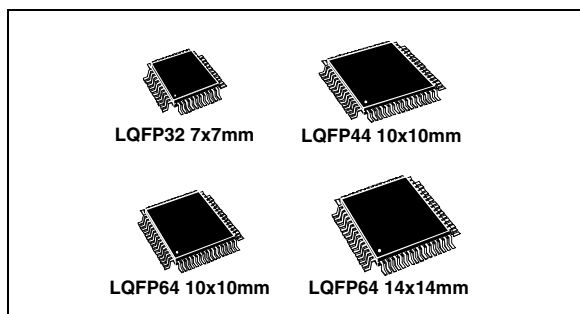
- Nested interrupt controller
- 14 interrupt vectors plus TRAP and RESET
- TLI top level interrupt (on 64-pin devices)
- Up to 21 ext. interrupt lines (on 4 vectors)

■ Up to 48 I/O ports

- Up to 48 multifunctional bidirectional I/Os
- Up to 36 alternate I/O functions
- Up to 6 high sink outputs

■ 5 timers

- 16-bit timer with 2 input captures, 2 output compares, external clock input, PWM and pulse generator modes
- 8-bit timer with 1 or 2 input captures, 1 or 2 output compares, PWM and pulse generator modes
- 8-bit PWM auto-reload timer with 1 or 2 input captures, 2 or 4 independent PWM output channels, output compare and time base interrupt, external clock with event detector
- Main clock controller with real-time base and clock output
- Window watchdog timer



■ Up to 4 communications interfaces

- SPI synchronous serial interface
- Master/ slave LINSICI™ asynchronous serial interface
- Master only LINSICI™ asynchronous serial interface
- CAN 2.0B active

■ Analog peripheral (low current coupling)

- 10-bit A/D converter with up to 16 inputs
- Up to 9 robust ports (low current coupling)

■ Instruction set

- 8-bit data manipulation
- 63 basic instructions, 17 main addressing modes
- 8 x 8 unsigned multiply instruction

■ Development tools

- Full hardware/ software development package

Table 1. Device summary

Reference	Part number
ST72561xx-Auto	ST72561K4-Auto, ST72561K6-Auto, ST72561K7-Auto, ST72561K9-Auto, ST72561J4-Auto, ST72561J6-Auto, ST72561J7-Auto, ST72561J9-Auto, ST72561R4-Auto, ST72561R6-Auto, ST72561R7-Auto, ST72561R9-Auto, ST72561AR4-Auto, ST72561AR6-Auto, ST72561AR7-Auto, ST72561AR9-Auto

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1 Description

The ST72561xx-Auto devices are members of the ST7 microcontroller family designed for automotive mid-range applications with CAN (Controller Area Network) and LIN (Local Interconnect Network) interface.

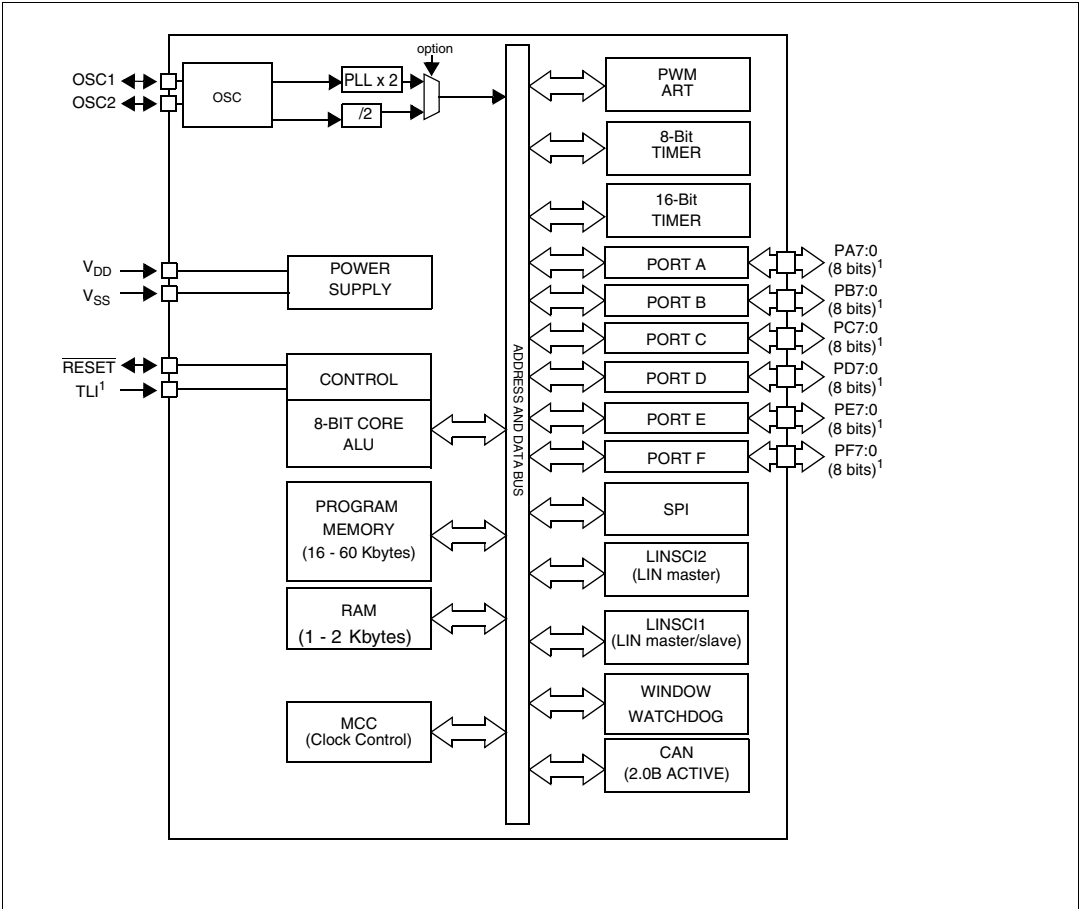
All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set and are available with Flash or ROM program memory.

The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

Table 2. Product overview

Features	ST72561(AR/R/J/K)9	ST72561(AR/R/J/K)7	ST72561(AR/R/J/K)6	ST72561(AR/R/J/K)4
Program memory - bytes	60K	48K	32K	16K
RAM (stack) - bytes	2K (256)	2K (256)	1K (256)	1K (256)
Operating supply	4.5V to 5.5V			
CPU frequency	External resonator oscillator w/ PLLx2/8 MHz			
Maximum temperature range	-40°C to +125°C			
Packages	LQFP64 10x10mm (AR), LQFP44 10x10mm (J), LQFP32 7x7mm (K) LQFP64 14x14 (R)			

Figure 1. Device block diagram



1. On some devices only (see [Table 2: Product overview](#))

1.1 Pin description

Figure 2. LQFP 64-pin package pinout

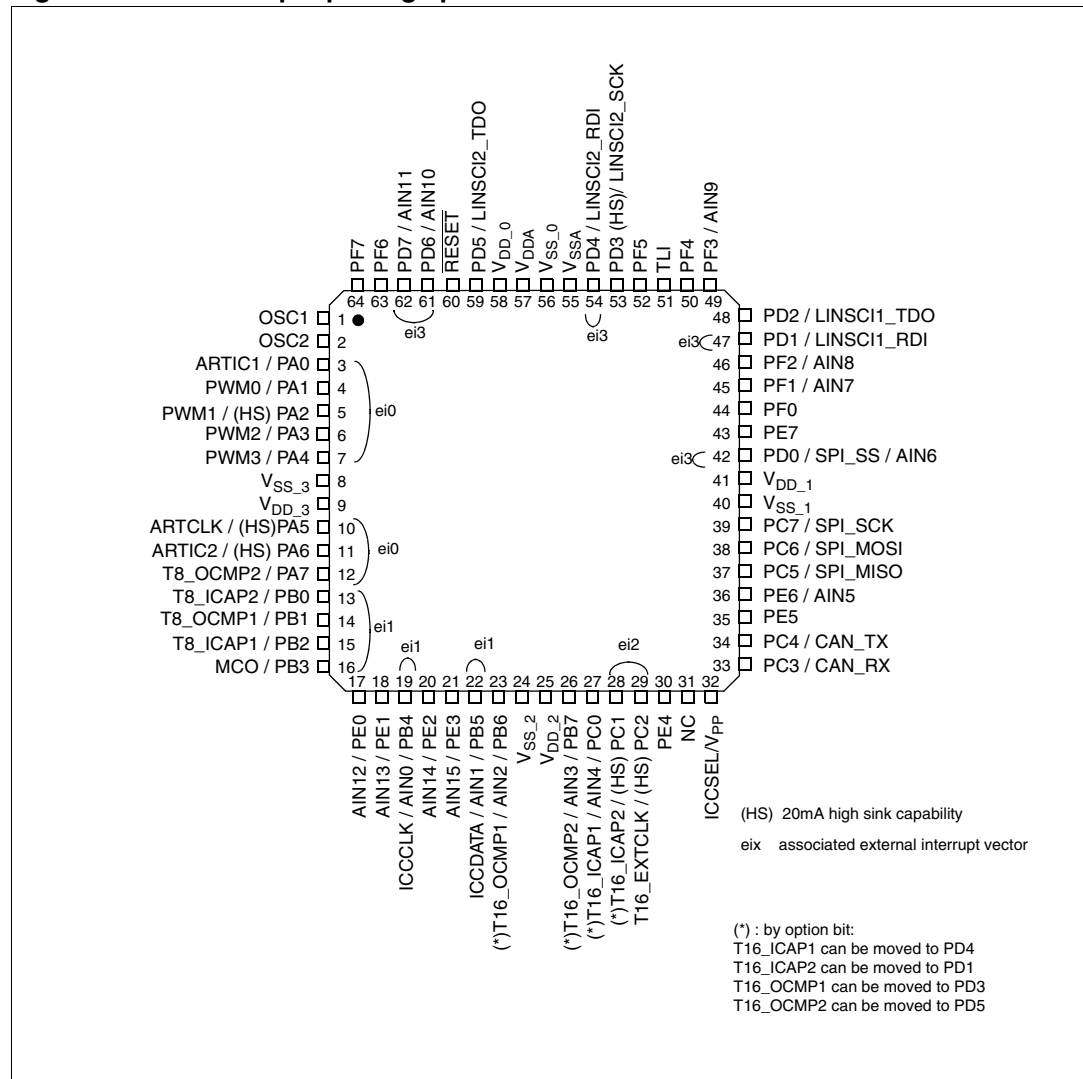


Figure 3. LQFP 44-pin package pinout

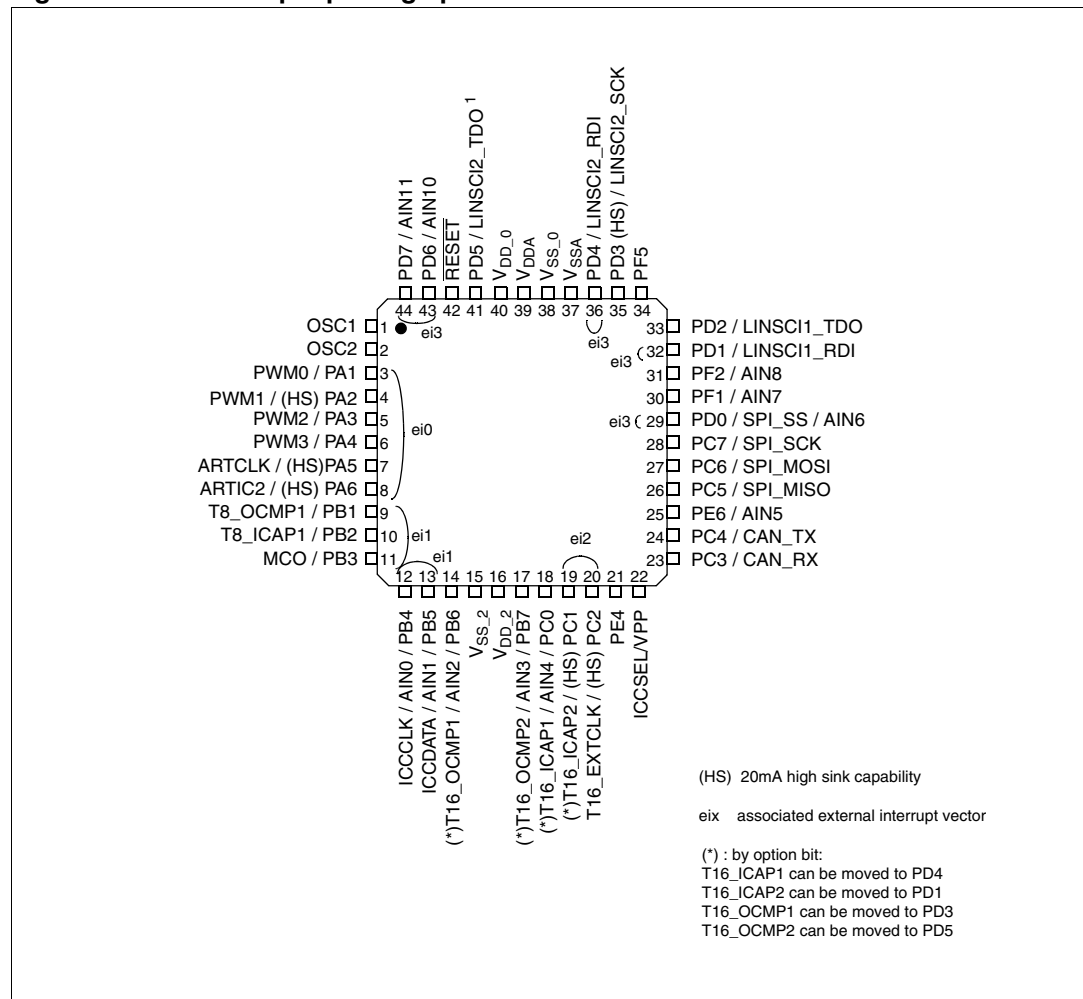
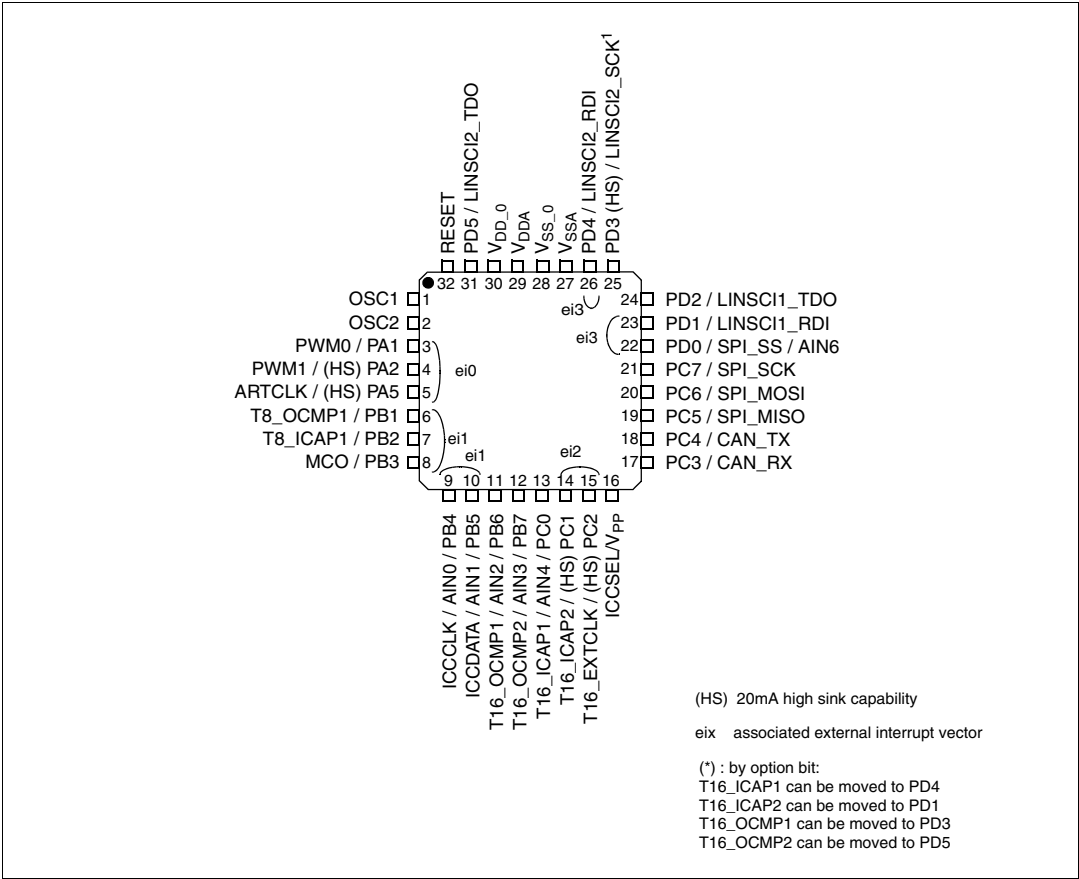


Figure 4. LQFP 32-pin package pinout



For external pin connection guidelines, refer to [Chapter 20: Electrical characteristics](#).

List of abbreviations used in [Table 3](#)

Type: I = input, O = output, S = supply

In/Output level: C_T = CMOS $0.3V_{DD}/0.7V_{DD}$ with Schmitt trigger
 T_T = TTL $0.8V / 2V$ with Schmitt trigger

Output level: HS = 20mA high sink (on N-buffer only)

Port and control configuration:

Input: float = floating, wpu = weak pull-up, int = interrupt, ana = analog,
 RB = robust

Output: OD = open drain, PP = push-pull

Refer to [Chapter 8: I/O ports](#) for more details on the software configuration of the I/O ports.
 The RESET configuration of each pin is shown in bold which is valid as long as the device is in reset state.

Table 3. Device pin description

Pin n°			Pin name	Type	Level		Port						Main function (after reset)	Alternate function	
LQFP64	LQFP44	LQFP32			Input	Output	Input ⁽¹⁾				Output				
							float	wpu	int	ana	OD	PP			
1	1	1	OSC1 ⁽²⁾	I									External clock input or resonator oscillator inverter input		
2	2	2	OSC2 ⁽²⁾	I/O									Resonator oscillator inverter output		
3	-	-	PA0 / ARTIC1	I/O	C _T		X		ei0		X	X	Port A0	ART input capture 1	
4	3	3	PA1 / PWM0	I/O	C _T		X		ei0		X	X	Port A1	ART PWM output 0	
5	4	4	PA2 (HS) / PWM1	I/O	C _T	HS	X		ei0		X	X	Port A2	ART PWM output 1	
6	5	-	PA3 / PWM2	I/O	C _T		X		ei0		X	X	Port A3	ART PWM output 2	
7	6	-	PA4 / PWM3	I/O	C _T		X		ei0		X	X	Port A4	ART PWM output 3	
8	-	-	V _{SS_3}	S									Digital ground voltage		
9	-	-	V _{DD_3}	S									Digital main supply voltage		
10	7	5	PA5 (HS) / ARTCLK	I/O	C _T	HS	X		ei0		X	X	Port A5	ART external clock	
11	8	-	PA6 (HS) / ARTIC2	I/O	C _T	HS	X		ei0		X	X	Port A6	ART input capture 2	
12	-	-	PA7 / T8_OCMP2	I/O	C _T		X		ei0		X	X	Port A7	TIM8 output capture 2	
13	-	-	PB0 / T8_ICAP2	I/O	C _T		X		ei1		X	X	Port B0	TIM8 input capture 2	
14	9	6	PB1 / T8_OCMP1	I/O	C _T		X		ei1		X	X	Port B1	TIM8 output capture 1	
15	10	7	PB2 / T8_ICAP1	I/O	C _T		X		ei1		X	X	Port B2	TIM8 input capture 1	
16	11	8	PB3 / MCO	I/O	C _T		X		ei1		X	X	Port B3	Main clock out (f _{OSC2})	
17	-	-	PE0 / AIN12	I/O	T _T		X	X		RB	X	X	Port E0	ADC analog input 12	
18	-	-	PE1 / AIN13	I/O	T _T		X	X		RB	X	X	Port E1	ADC analog input 13	
19	12	9	PB4 / AIN0 / ICCCLK	I/O	C _T		X		ei1	RB	X	X	Port B4	ICC clock input	ADC analog input 0