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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

General Description

The MAX17230/MAX17231 offers dual synchronous step-down DC-DC controllers with integrated MOSFETs and a step-up/boost controller. They operate over a 3.5V to 36V input voltage range, and down to 2V with the boost controller active. The devices can operate in dropout condition by running at 95% duty cycle. The controllers can generate fixed output voltages of 3.3V/5V, along with the capability to program the output voltage between 1V to 10V.

These devices use current-mode-control architecture and can be operated in the pulse-width modulation (PWM) or pulse-frequency modulation (PFM) control schemes. PWM operation provides constant frequency operation at all loads and is useful in applications sensitive to switching frequency. PFM operation disables negative inductor current and additionally skips pulses at light loads for high-efficiency. The low-resistance, on-chip MOSFETs ensure high efficiency at full load and simplify the layout.

The MAX17230/MAX17231 include a boost controller. This boost circuitry turns on during low input voltage conditions. It is designed to power step-down controller channels with input voltages as low as 2V.

These devices are available in a 40-pin TQFN package with exposed pad, and are specified for operation over -40°C to +85°C.

Applications

- Distributed Supply Regulation
- Wall Transformer Regulation
- General-Purpose Point-of-Load

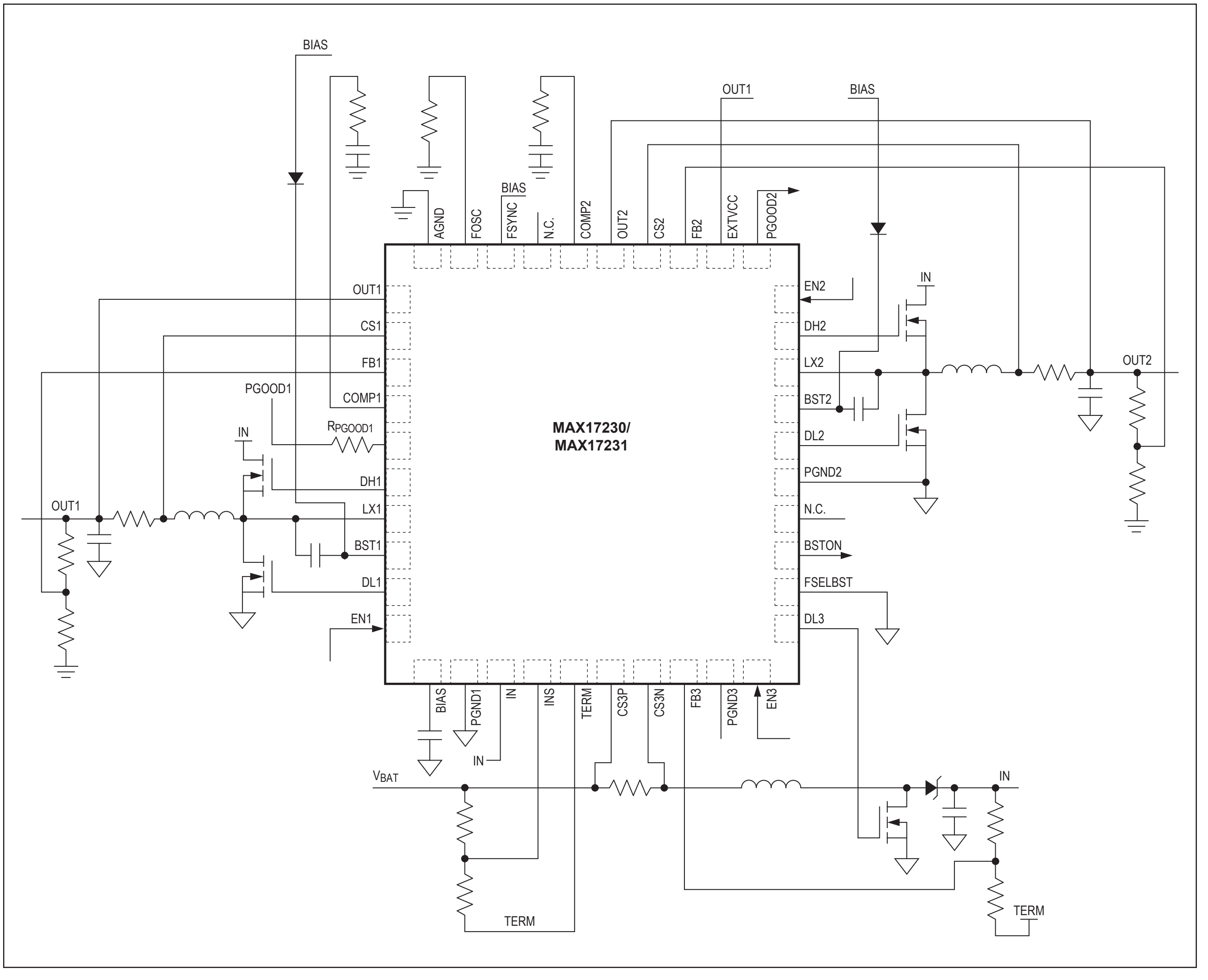
Benefits and Features

- Eliminates External Components and Reduces Total Cost
  - No Schottky-Synchronous Operation for High Efficiency and Reduced Cost
  - Simple External RC compensation for Stable Operation at Any Output Voltage
  - All-Ceramic Capacitor Solution: Ultra-Compact Layout
  - 180° Out-of-Phase Operation Reduces Output Ripple and Enables Cascaded Power Supplies
- Reduces Number of DC-DC Controllers to Stock
  - Fixed Output Voltage with ±1% Accuracy (5V/3.3V) or Externally Resistor Adjustable (1V to 10V)
  - 220kHz to 2.2MHz Adjustable Frequency with External Synchronization
  - Frequency Synchronization Input
- Reduces Power Dissipation
  - 92% Peak Efficiency
  - 8μA (typ) in Shutdown
  - 20μA (typ) Quiescent Current in PFM Mode
- Operates Reliably
  - 42V Input Voltage Transient Protection
  - Cycle-by-Cycle Current Limit, Thermal Shutdown
  - Supply Overvoltage and Undervoltage Lockout
  - Power-OK Monitor
  - Reduced EMI Emission with Spread-Spectrum Control
  - 50ns Minimum On-Time Guarantees PWM Operation at Low Duty Cycle at 2.2MHz

Ordering Information and Selector Guide appear at end of data sheet.

19-8313; Rev 0; 2/16

Typical Application Circuit



Absolute Maximum Ratings

IN, INS, CS3P, CS3N, FB3, EN1, EN2, EN3, TERM to PGND_ .... -0.3V to +42V
CS1, CS2, OUT1, OUT2 to AGND .... -0.3V to +11V
CS1 to OUT1 .... -0.2V to +0.2V
CS2 to OUT2 .... -0.2V to +0.2V
CS3P to CS3N .... -0.2V to +0.2V
BIAS, FSYNC, FOSC to AGND .... -0.3V to +6.0V
COMP1, COMP2, BSTON to AGND .... -0.3V to +6.0V
FB1, FB2, FSELBST, EXTVCC to AGND .... -0.3V to +6.0V
DL_ to PGND_ (Note 1) .... -0.3V to +6.0V
BST_ to LX_ (Note 1) .... -0.3V to + 6.0V
DH_ to LX_ (Note 1) .... -0.3V to + 6.0V
LX_ to PGND_ (Note 1) .... -0.3V to +42V
PGND_ to AGND .... -0.3V to +0.3V
PGOOD1, PGOOD2 to AGND .... -0.3V to +6.0V
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 37mW/°C above +70°C) 2963mW
QFND (derate 29.4mW/°C above +70°C) 2350mW
Operating Temperature Range .... -40°C to +85°C
Junction Temperature Range .... +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
Soldering Temperature (reflow) .... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 27°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .... 1°C/W

QFND
Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 34°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .... 3.9°C/W

Note 1: Self-protected against transient voltages exceeding these limits for ≤ 50ns under normal operation and loads up to the maximum rated output current.
Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 14V, V_{BIAS} = 5V, C_{BIAS} = 6.8µF, T_A = T_J = -40°C to +85°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SYNCHRONOUS STEP-DOWN DC-DC CONVERTERS						
Supply Voltage Range	V_{IN}	Normal operation	3.5		36	V
		t < 1s			42	
		With preboost after initial startup condition is satisfied	2.0		36	
Supply Current	I_{IN}	V_{EN1} = V_{EN2} = V_{EN3} = 0V		8	20	µA
		V_{EN1} = 5V, V_{OUT1} = 5V, V_{EN2} = V_{EN3} = 0V, V_{EXTVCC} = 5V, no switching		30	40	
		V_{EN2} = 5V, V_{OUT2} = 3.3V, V_{EN1} = V_{EN3} = 0V, V_{EXTVCC} = 3.3V, no switching		20	30	
		V_{EN1} = V_{EN2} = 5V, V_{OUT1} = 5V, V_{OUT2} = 3.3V, V_{EN3} = 0V, V_{EXTVCC} = 3.3V, no switching		25	40	
Buck 1 Fixed Output Voltage	V_{OUT1}	V_{FB1} = V_{BIAS}, PWM mode	4.95	5	5.05	V
		V_{FB1} = V_{BIAS}, skip mode	4.95	5	5.075	
Buck 2 Fixed Output Voltage	V_{OUT2}	V_{FB2} = V_{BIAS}, PWM mode	3.234	3.3	3.366	V
		V_{FB2} = V_{BIAS}, skip mode	3.234	3.3	3.4	
Output Voltage Adjustable Range		Buck 1, buck 2	1		10	V

Electrical Characteristics (continued)

(V_{IN} = 14V, V_{BIAS} = 5V, C_{BIAS} = 6.8µF, T_A = T_J = -40°C to +85°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Regulated Feedback Voltage	$V_{FB1,2}$		0.99	1.0	1.01	V
Output Overvoltage Threshold		FB rising	+10	+15	+20	%
		FB falling (Note 4)	+5	+10	+15	
Feedback Leakage Current	$I_{FB1,2}$	T_A = +25°C		0.01	1	µA
Feedback Line Regulation Error		V_{IN} = 3.5V to 36V, V_{FB} = 1V		0.00		%/V
Transconductance (from FB_ to COMP_)	g_m	V_{FB} = 1V, V_{BIAS} = 5V (Note 5)		1200	2400	µS
Dead Time		MAX17231, DL_ low to DH_ high		35		ns
		MAX17231, DH_ low to DL_ high		60		
		MAX17230, DL_ low to DH_ high		60		
		MAX17230, DH_ low to DL_ high		100		
Maximum Duty-Cycle		Buck 1, buck 2			95	%
Minimum On-Time	$t_{ON(MIN)}$	Buck 1, buck 2		50		ns
PWM Switching Frequency Range		Programmable, high frequency, MAX17231	1		2.2	MHz
		Programmable, low frequency, MAX17230	0.2		1	
Switching Frequency Accuracy	f_{SW}	MAX17231, R_{FOSC} = 13.7kΩ, V_{BIAS} = 5V	1.98	2.2	2.42	MHz
		MAX17230, R_{FOSC} = 80.6kΩ, V_{BIAS} = 5V	360	400	440	kHz
Spread-Spectrum Range		Spread spectrum enabled		±6		%
FSYNC INPUT						
FSYNC Frequency Range		Minimum sync pulse of 100ns, MAX17231	1.2		2.4	MHz
		Minimum sync pulse of 100ns, MAX17230	240		1200	kHz
FSYNC Switching Thresholds		High threshold	1.5			V
		Low threshold			0.6	
CS Current-Limit Voltage Threshold	$V_{LIMIT1,2}$	V_{CS} - V_{OUT}, V_{BIAS} = 5V, V_{OUT} ≥ 2.5V	64	80	96	mV
Skip Mode Threshold		Current sense = 80mV		15		mV
Soft-Start Ramp Time		Buck 1 and buck 2, fixed soft-start time regardless of frequency	2	6	10	ms
Phase Shift Between Buck1 and Buck 2				180		°
LX1, LX2 Leakage Current		V_{IN} = 6V, $V_{LX\_}$ = V_{IN}, T_A = +25°C		0.01	1	µA
DH1, DH2 Pullup Resistance		V_{BIAS} = 5V, $I_{DH\_}$ = -100mA		10	20	Ω
DH1, DH2 Pulldown Resistance		V_{BIAS} = 5V, $I_{DH\_}$ = +100mA		2	4	Ω

Electrical Characteristics (continued)

(V_{IN} = 14V, V_{BIAS} = 5V, C_{BIAS} = 6.8μF, T_A = T_J = -40°C to +85°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DL1, DL2 Pullup Resistance		V_{BIAS} = 5V, $I_{DL\_}$ = -100mA		4	8	Ω
DL1, DL2 Pulldown Resistance		V_{BIAS} = 5V, $I_{DL\_}$ = +100mA		1.5	3	Ω
PGOOD1, PGOOD2 Threshold	P_{GOOD_H}	% of $V_{OUT\_}$, rising	85	90	95	%
	P_{GOOD_F}	% of $V_{OUT\_}$, falling	80	85	90	
PGOOD1, PGOOD2 Leakage Current		$V_{PGOOD1,2}$ = 5V, T_A = +25°C		0.01	1	μA
PGOOD1, PGOOD2 Startup Delay Time		Buck 1 and buck 2 after soft-start is complete		64		Cycles
PGOOD1, PGOOD2 Debounce Time		Fault detection	8	20	40	μs
INTERNAL LDO: BIAS						
Internal BIAS Voltage		V_{IN} > 6V	4.75	5	5.25	V
BIAS UVLO Threshold		V_{BIAS} rising		3.1	3.4	V
		V_{BIAS} falling	2.7	2.9		
Hysteresis				0.2		V
External V_{CC} Threshold	$V_{TH,EXTVCC}$	EXTVCC rising, HYST = 110mV		3	3.2	V
THERMAL OVERLOAD						
Thermal Shutdown Temperature		(Note 5)		170		°C
Thermal Shutdown Hysteresis		(Note 5)		20		°C
EN LOGIC INPUT						
High Threshold			1.8			V
Low Threshold					0.8	V
Input Current		EN1, EN2 logic inputs only, T_A = +25°C		0.01	1	μA
PREBOOST						
Minimum On Time	TON_{BST}			60		ns
Minimum Off Time	$TOFF_{BST}$			60		ns
Switching Frequency	f_{BOOST}	$V_{FSELBST}$ = 0V, R_{FOSC} = 13.7kΩ	1.98	2.2	2.42	MHz
		$V_{FSELBST}$ = V_{BIAS}, R_{FOSC} = 13.7kΩ	0.4	0.44	0.48	
Current Limit	I_{LIMBST}	CS3P - CS3N	108	120	132	mV
INS Unlock Threshold	$V_{INS,UV}$	One-time latch during startup; preboost is disabled until the V_{INS} rises above this threshold (MAX17231ATLV/V+, MAX17231ATLW/V+ (Note 6))	1	1.05	1.1	V

Electrical Characteristics (continued)

(V_{IN} = 14V, V_{BIAS} = 5V, C_{BIAS} = 6.8μF, T_A = T_J = -40°C to +85°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
INS Off Threshold	$V_{INS,OFF}$	Battery rising and EN3 high, preboost turns off if V_{INS} is above this threshold (MAX17231ATLV/V+, MAX17231ATLW/V+ (Note 6))	1.2	1.25	1.3	V
INS On Threshold	$V_{INS,ON,SW}$	Battery falling and EN3 high, preboost turns back on when V_{INS} falls below this threshold (MAX17231ATLV/V+, MAX17231ATLW/V+ (Note 6))	1.1	1.15	1.2	
INS Threshold Undervoltage Lockout	$V_{INS,UV}$	Battery rising and EN3 high (MAX17231ATLV/V+, MAX17231ATLW/V+ (Note 6))	0.325	0.35	0.375	V
		Battery falling and EN3 high, preboost turns off when V_{INS} falls below this threshold (MAX17231ATLV/V+, MAX17231ATLW/V+ (Note 6))	0.275	0.3	0.325	
BSTON Leakage Current		V_{BSTON} = 5V, T_A = +25°C		0.01	1	μA
BSTON Debounce Time		Fault detection		10		μs
DL3 Pullup Resistance		V_{BIAS} = 5V, I_{DL3} = -100mA		4	8	Ω
DL3 Pulldown resistance		V_{BIAS} = 5V, I_{DL3} = +100mA		1	2	Ω
Feedback Voltage	V_{FB3}	No load on boost output	1.1875	1.25	1.3125	V
Boost Load Regulation Error		0mV < V_{CS3P} - V_{CS3N} < 120mV, error proportional to input current		0.7		%/A
EN3 Threshold		High threshold	3.5			V
		Low threshold			2	
EN3 Input Current		V_{EN3} = 5.5V		7	14	μA
TERM Resistance		I_{TERM} = 10mA		70	150	Ω
TERM Leakage Current		V_{TERM} = 14V, V_{EN3} = 0V, T_A = +25°C		0.01	1	μA
INS and FB3 Leakage Current		T_A = +25°C		0.01	1	μA

Note 3: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at T_A = +25°C.

Note 4: Overvoltage protection is detected at the FB1/FB2 pins. If the feedback voltage reaches overvoltage threshold of FB1/FB2 + 15% (typ), the corresponding controllers stop switching. The controllers resume switching once the output drops below FB1/FB2 + 10% (typ).

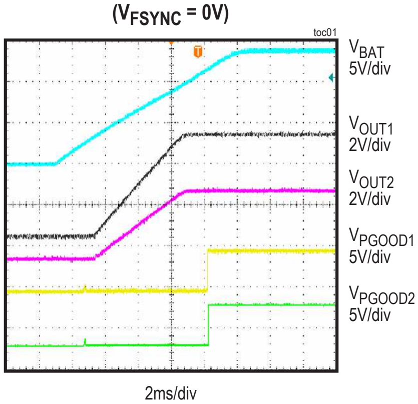
Note 5: Guaranteed by design; not production tested.

Note 6: INS pin functionality is disabled for the MAX17231ATLV/V+, MAX17231ATLW/V+. EN3 directly controls the turn-on and turn-off of the boost controller.

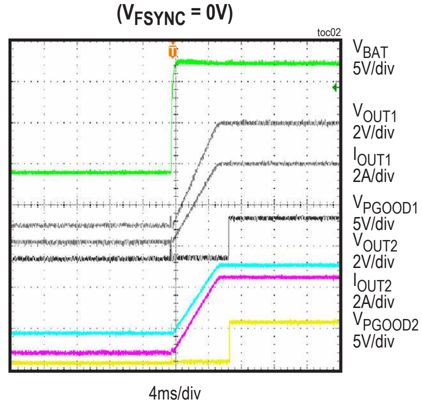
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

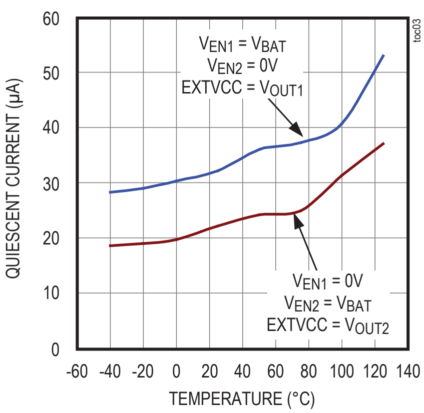
NO-LOAD STARTUP SEQUENCE (V_{FSYNC} = 0V)



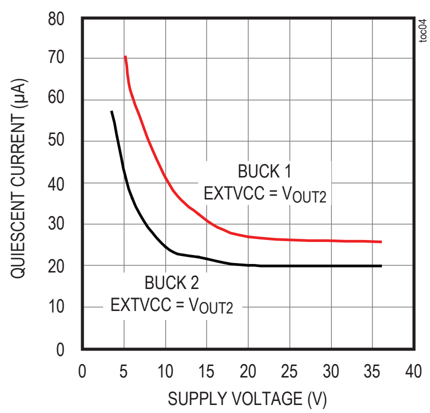
FULL-LOAD STARTUP SEQUENCE (V_{FSYNC} = 0V)



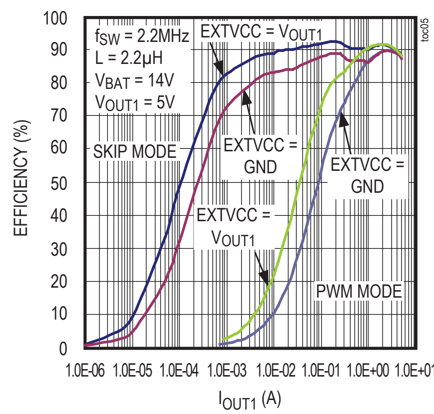
QUIESCENT CURRENT vs. TEMPERATURE



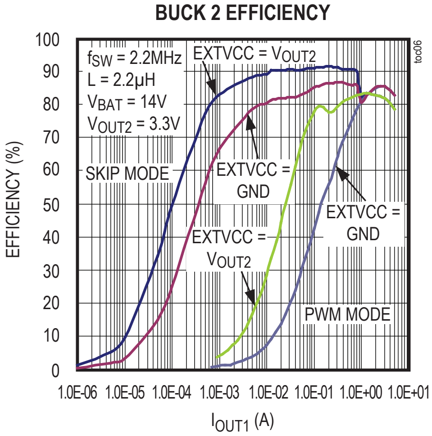
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



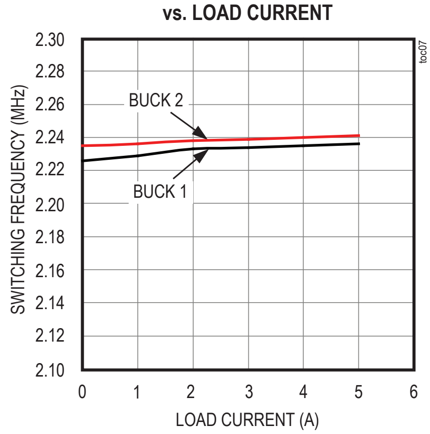
BUCK 1 EFFICIENCY



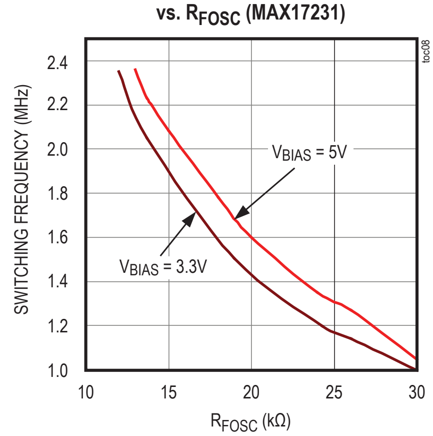
BUCK 2 EFFICIENCY



SWITCHING FREQUENCY vs. LOAD CURRENT



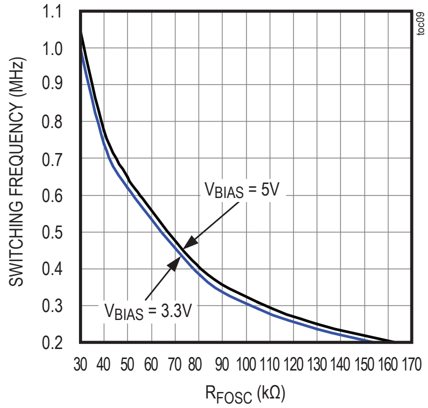
SWITCHING FREQUENCY vs. R_{FOSC} (MAX17231)



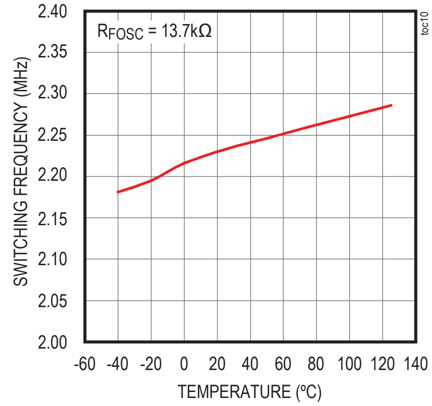
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

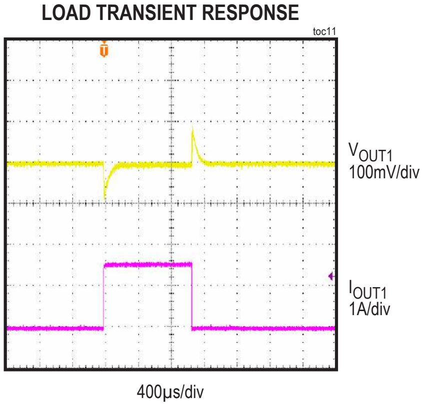
SWITCHING FREQUENCY vs. R_{FOSC} (MAX17230)



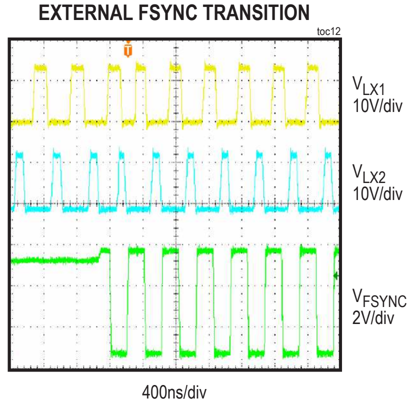
SWITCHING FREQUENCY vs. TEMPERATURE



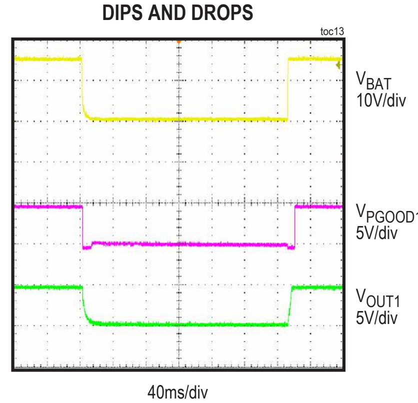
LOAD TRANSIENT RESPONSE



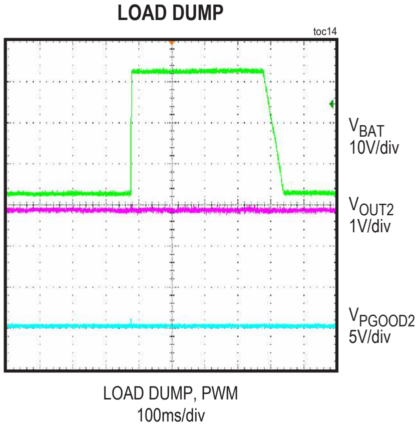
EXTERNAL FSYNC TRANSITION



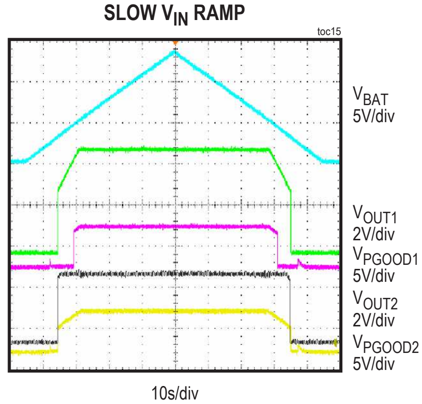
DIPS AND DROPS



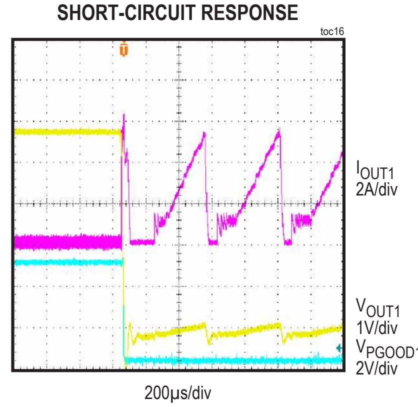
LOAD DUMP



SLOW V_{IN} RAMP



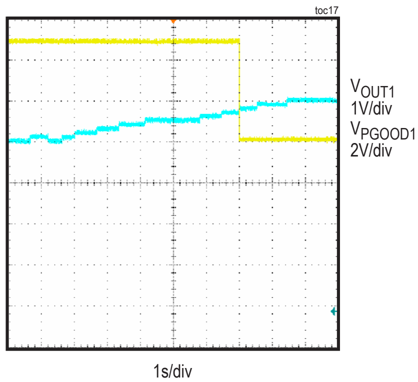
SHORT-CIRCUIT RESPONSE



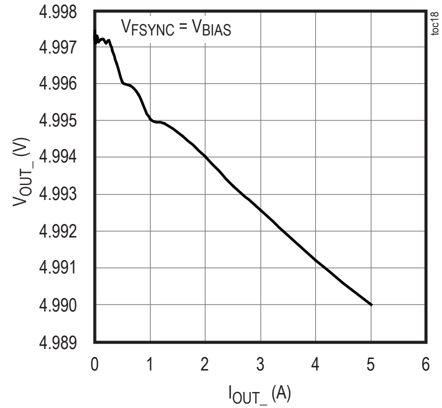
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

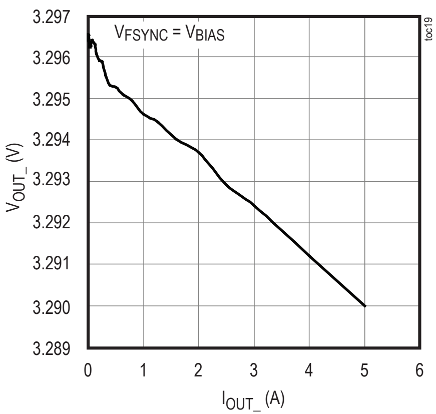
OUTPUT OVERVOLTAGE RESPONSE



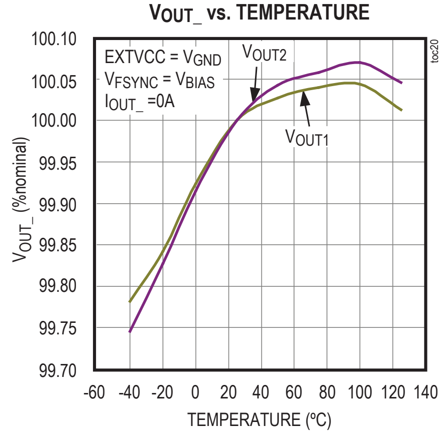
BUCK 1 LOAD REGULATION



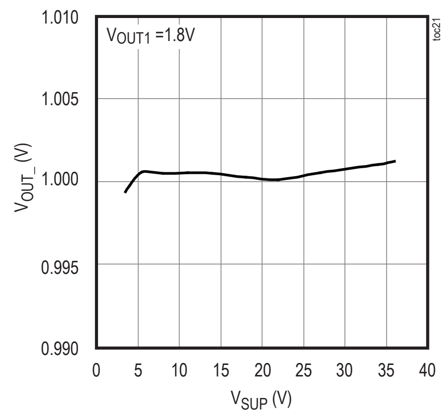
BUCK 2 LOAD REGULATION



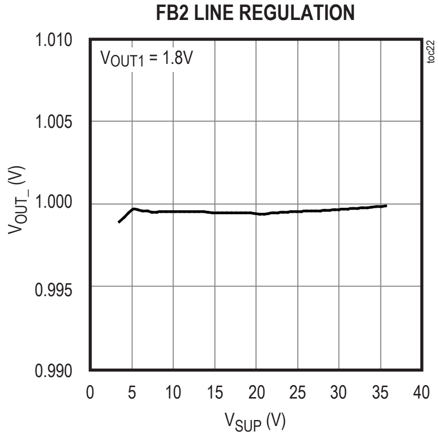
VOUT_ vs. TEMPERATURE



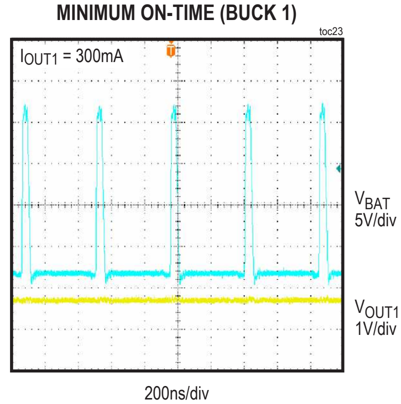
FB1 LINE REGULATION



FB2 LINE REGULATION



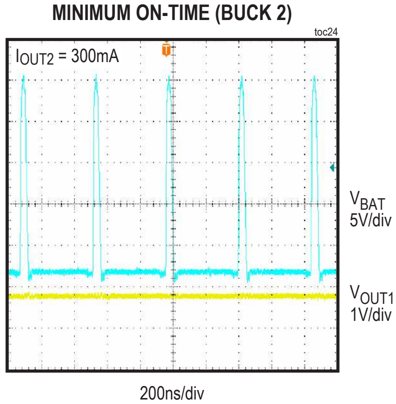
MINIMUM ON-TIME (BUCK 1)



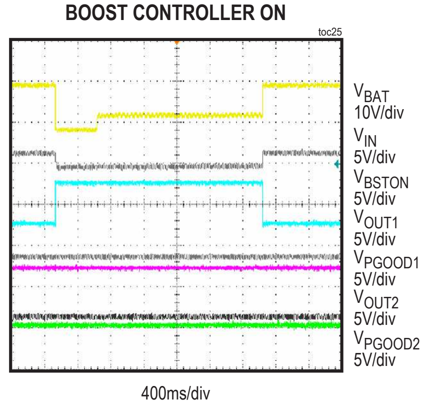
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

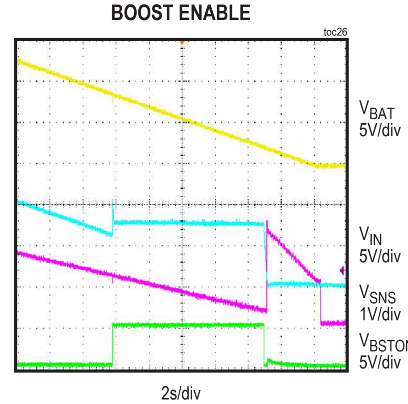
MINIMUM ON-TIME (BUCK 2)



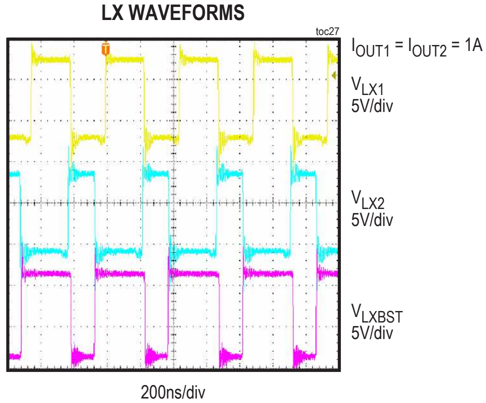
BOOST CONTROLLER ON



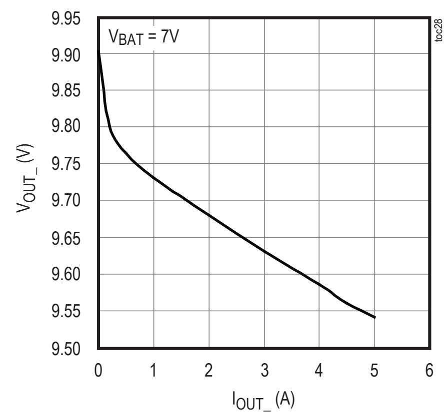
BOOST ENABLE



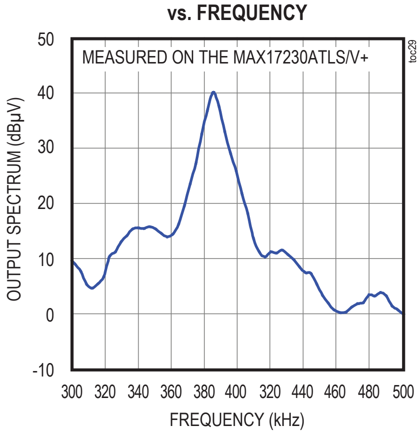
LX WAVEFORMS



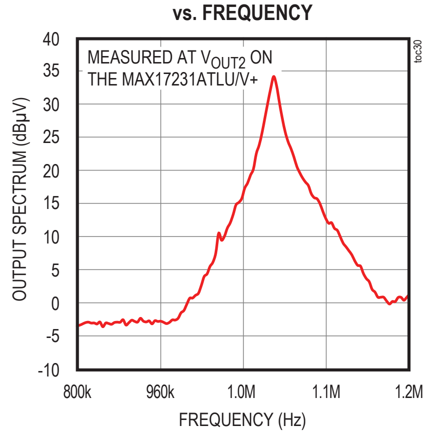
PREBOOST LOAD REGULATION



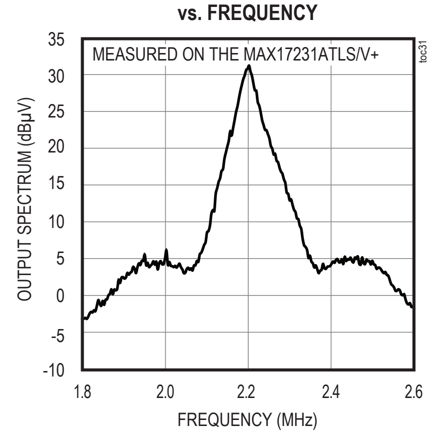
SPECTRAL ENERGY DENSITY vs. FREQUENCY



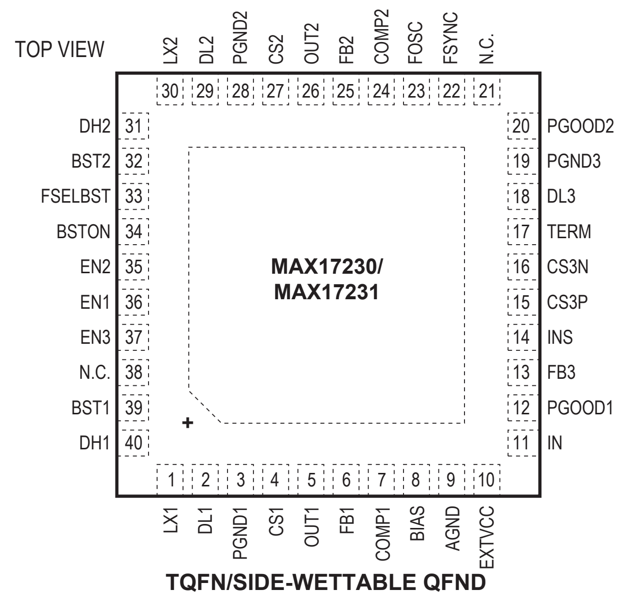
SPECTRAL ENERGY DENSITY vs. FREQUENCY



SPECTRAL ENERGY DENSITY vs. FREQUENCY



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	LX1	Inductor Connection for Buck 1. Connect LX1 to the switched side of the inductor. LX1 serves as the lower supply rail for the DH1 high-side gate drive.
2	DL1	Low-Side Gate Drive Output for Buck 1. DL1 output voltage swings from V_{PGND1} to V_{BIAS}.
3	PGND1	Power Ground for Buck 1
4	CS1	Positive Current-Sense Input for Buck 1. Connect CS1 to the positive terminal of the current-sense resistor. See the *Current Limiting and Current-Sense Inputs* and *Current-Sense Measurement* sections.
5	OUT1	Output Sense and Negative Current-Sense Input for Buck 1. When using the internal preset 5V feedback divider (FB1 = BIAS), the buck uses OUT1 to sense the output voltage. Connect OUT1 to the negative terminal of the current-sense resistor. See the *Current Limiting and Current-Sense Inputs* and *Current-Sense Measurement* sections.
6	FB1	Feedback Input for Buck 1. Connect FB1 to BIAS for the 5V fixed output or to a resistive divider between OUT1 and GND to adjust the output voltage between 1V and 10V. In adjustable mode, FB1 regulates to 1V (typ). See the *Setting the Output Voltage in Buck Converters* section.
7	COMP1	Buck 1 Error-Amplifier Output. Connect an RC network to COMP1 to compensate buck 1.
8	BIAS	5V Internal Linear Regulator Output. Bypass BIAS to GND with a low-ESR ceramic capacitor of 6.8μF minimum value. BIAS provides the power to the internal circuitry and external loads. See the *Fixed 5V Linear Regulator (BIAS)* section.
9	AGND	Signal Ground for IC
10	EXTVCC	3.1V to 5.2V Input to the Switchover Comparator

Pin Description (continued)

PIN	NAME	FUNCTION
11	IN	Supply Input. Connect IN to the output of the preboost. Bypass IN with sufficient capacitance to supply the two out-of-phase buck converters.
12	PGOOD1	Open-Drain Power-Good Output for Buck 1. PGOOD1 is low if OUT1 is more than 15% (typ) below the normal regulation point. PGOOD1 asserts low during soft-start and in shutdown. PGOOD1 becomes high impedance when OUT1 is in regulation. To obtain a logic signal, pullup PGOOD1 with an external resistor connected to a positive voltage lower than 5.5V. Place a minimum of 100Ω (R_{PGOOD1}) in series with PGOOD1. See the *Voltage Monitoring (PGOOD_)* section for details.
13	FB3	Preboost Feedback Input. Connect FB3 to the center tap of a resistive-divider between the boost regulator output and TERM to adjust the output voltage. FB3 regulates to 1.25V (typ). Ensure that the parallel combination of the resistor-divider network is > 500Ω. See the *Setting the Output Voltage in Boost Converter* section.
14	INS	Input Voltage Sense for Preboost. The voltage at INS is compared to internal comparator reference. Program the preboost threshold by using resistor-divider from BAT to INS to TERM pin. Ensure that the parallel combination of the resistor-divider network is > 500Ω. For the MAX17231ATLV/V+ and MAX17231ATLW/V+, the INS functionality is disabled; however, the INS pin should still be connected using the resistor-divider between V_{BAT} and the TERM pin.
15	CS3P	Positive Current-Sense Input for Preboost. Connect CS3P to the positive terminal of the current-sense resistor. See the *Current Limit in Boost Controller* and *Shunt Resistor Selection in Boost Converter* sections.
16	CS3N	Negative Current-Sense Input for Preboost. Connect CS3N to the negative terminal of the current-sense resistor. See the *Current Limit in Boost Controller* and *Shunt Resistor Selection in Boost Converter* sections.
17	TERM	Ground Switch. TERM opens when the voltage at EN3 is logic-low. Use TERM to terminate the preboost feedback and INS resistive divider.
18	DL3	Preboost nMOSFET Gate-Drive Output
19	PGND3	Power Ground for Preboost. All the high-current paths for the preboost should terminate to this ground.
20	PGOOD2	Open-Drain Power-Good Output for Buck 2. PGOOD2 is low if OUT2 is more than 90% (typ) below the normal regulation point. PGOOD2 asserts low during soft-start and in shutdown. PGOOD2 becomes high impedance when OUT2 is in regulation. To obtain a logic signal, pullup PGOOD2 with an external resistor connected to a positive voltage lower than 5.5V.
21, 38	N.C.	No Connection
22	FSYNC	External Clock Synchronization Input. Synchronization to the controller operating frequency ratio is 1. Keep f_{SYNC} a minimum of 10% greater than the maximum internal switching frequency for stable operation. See the *Switching Frequency/External Synchronization* section.
23	FOSC	Frequency Setting Input. Connect a resistor from FOSC to AGND to set the switching frequency of the DC-DC converters.
24	COMP2	Buck 2 Error Amplifier Output. Connect an RC network to COMP2 to compensate buck 2.
25	FB2	Feedback Input for Buck 2. Connect FB2 to BIAS for the 3.3V fixed output or to a resistive divider between OUT2 and GND to adjust the output voltage between 1V and 10V. In adjustable mode, FB2 regulates to 1V (typ). See the *Setting the Output Voltage in Buck Converters* section.

Pin Description (continued)

PIN	NAME	FUNCTION
26	OUT2	Output Sense and Negative Current-Sense Input for Buck 2. When using the internal preset 3.3V feedback-divider (FB2 = BIAS), the buck uses OUT2 to sense the output voltage. Connect OUT2 to the negative terminal of the current-sense resistor. See the *Current Limiting and Current-Sense Inputs* and *Current-Sense Measurement* sections.
27	CS2	Positive Current-Sense Input for Buck 2. Connect CS2 to the positive terminal of the current-sense resistor. See the *Current Limiting and Current-Sense Inputs* and *Current-Sense Measurement* sections.
28	PGND2	Power Ground for Buck 2
29	DL2	Low-Side Gate Drive Output for Buck 2. DL2 output voltage swings from V_{PGND2} to V_{BIAS}.
30	LX2	Inductor Connection for Buck 2. Connect LX2 to the switched side of the inductor. LX2 serves as the lower supply rail for the DH2 high-side gate drive.
31	DH2	High-Side Gate Drive Output for Buck 2. DH2 output voltage swings from V_{LX2} to V_{BST2}.
32	BST2	Boost Capacitor Connection for High-Side Gate Voltage of Buck 2. Connect a high-voltage diode between BIAS and BST2. Connect a ceramic capacitor between BST2 and LX2. See the *High-Side Gate-Driver Supply (BST_)* section.
33	FSELBST	Frequency Select Pin for the Preboost. When pulled low, the preboost will have the same switching frequency as buck 1. When pulled high, the preboost will have a switching frequency that is 1/5th that of buck 1. FSELBST is only active for the MAX17231. FSELBST should be connected to ground for the MAX17230.
34	BSTON	Preboost On-Indicator Output. To obtain a logic signal, pull up BSTON with an external resistor connected to a positive voltage lower than 5.5V. BSTON goes high to indicate that the preboost is on.
35	EN2	High-Voltage Tolerant, Active-High Digital Enable Input for Buck 2. Driving EN2 high enables buck 2.
36	EN1	High-Voltage Tolerant, Active-High Digital Enable Input for Buck 1. Driving EN1 high enables buck 1.
37	EN3	High-Voltage Tolerant, Active-High Digital Enable Input for Preboost. When EN3 is high, the external preboost is enabled and begins switching if V_{INS} drops below $V_{INS,OLV}$ and required conditions are met (see the *Preboost* section).
39	BST1	Boost Capacitor Connection for High-Side Gate Voltage of Buck 1. Connect a high-voltage diode between BIAS and BST1. Connect a ceramic capacitor between BST1 and LX1. See the *High-Side Gate-Driver Supply (BST_)* section.
40	DH1	High-Side Gate-Drive Output for Buck 1. DH1 output voltage swings from V_{LX1} to V_{BST1}.
—	EP	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PGND1, PGND2, PGND3, and AGND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Detailed Description

The MAX17230/MAX17231 are automotive-rated triple-output switching power supplies. These devices integrate two synchronous step-down controllers and an non-synchronous step-up controller and can provide up to three independently controlled power rails as follows:

- A boost controller with adjustable output voltage.
- A buck controller with a fixed 5V output voltage or an adjustable 1V to 10V output voltage.
- A buck controller with a fixed 3.3V output voltage or an adjustable 1V to 10V output voltage.

The buck controllers and the preboost can each provide up to 10A output current and are independently controllable.

Buck 1, buck 2, and the preboost are enabled and disabled by the EN1, EN2, EN3 control inputs, respectively. These are active-high inputs and can be connected directly to car battery.

- EN1 and EN2 enable the respective buck controllers. Connect EN1 and EN2 directly to V_{BAT} or to power-supply sequencing logic.
- EN3 controls the boost controller.

In standby mode (only buck 2 is active), the total supply current is reduced to 30μA (typ). When all three controllers are disabled, the total current drawn is further reduced to 6.8μA.

Fixed 5V Linear Regulator (BIAS)

The internal circuitry of the devices require a 5V bias supply. An internal 5V linear regulator (BIAS) generates this bias supply. Bypass BIAS with a 6.8μF or greater ceramic capacitor to guarantee stability under the full-load condition.

The internal linear regulator can source up to 100mA (150mA under EXTVCC switchover, see the EXTVCC Switchover section). Use the following equation to estimate the internal current requirements for the devices:

$$I_{BIAS} = I_{CC} + f_{SW}(Q_{G\_DL3} + Q_{G\_DH1} + Q_{G\_DL1} + Q_{G\_DH2} + Q_{G\_DL2}) = 10mA \text{ to } 50mA \text{ (typ)}$$

where I_{CC} is the internal supply current, 5mA (typ), f_{SW} is the switching frequency, and $Q_{G\_}$ is the MOSFET's total gate charge (specification limits at V_{GS} = 5V). To minimize the internal power dissipation, bypass BIAS to an external 5V rail.

EXTVCC Switchover

The internal linear regulator can be bypassed by connecting an external supply (3V to 5.2V) or the output of one of the buck converters to EXTVCC. BIAS internally switches to EXTVCC and the internal linear regulator turns off. This configuration has several advantages:

- It reduces the internal power dissipation of the MAX17230/MAX17231.
- The low-load efficiency improves as the internal supply current gets scaled down proportionally to the duty cycle.

If V_{EXTVCC} drops below $V_{TH,EXTVCC}$ = 3.0V (min), the internal regulator enables and switches back to BIAS.

Undervoltage Lockout (UVLO)

The BIAS input undervoltage-lockout (UVLO) circuitry inhibits switching if the 5V bias supply (BIAS) is below its 2.9V (typ) UVLO falling threshold. Once the 5V bias supply (BIAS) rises above its UVLO rising threshold and EN1 and EN2 enable the buck controllers, the controllers start switching and the output voltages begin to ramp up using soft-start.

Buck Controllers

The devices provide two buck controllers with synchronous rectification. The step-down controllers use a PWM, current-mode control scheme. External logic-level MOSFETs allow for optimized load-current design. Fixed-frequency operation with optimal interleaving minimizes input ripple current from the minimum to the maximum input voltages. Output-current sensing provides an accurate current limit with a sense resistor or power dissipation can be reduced using lossless current sensing across the inductor.

Soft-Start

Once a buck converter is enabled by driving the corresponding EN_ high, the soft-start circuitry gradually ramps up the reference voltage during soft-start time (t_{SSTART} = 6ms (typ)) to reduce the input surge currents during startup. Before the device can begin the soft-start, the following conditions must be met:

1) V_{BIAS} exceeds the 3.4V (max) undervoltage lockout threshold.
2) $V_{EN\_}$ is logic-high.

Switching Frequency/External Synchronization

The MAX17231 provides an internal oscillator adjustable from 1MHz to 2.2MHz. The MAX17230 provides an internal oscillator adjustable from 200kHz to 1MHz. High-frequency operation optimizes the application for the smallest component size, trading off efficiency to higher switching losses. Low-frequency operation offers the best overall efficiency at the expense of component size and board space. To set the switching frequency, connect a resistor R_{FOSC} from FOSC to AGND. See TOCs 8 and 9 in the Typical Operating Characteristics section to determine the relationship between switching frequency and R_{FOSC}.

Buck 1 and the boost converter are synchronized with the internal clock-signal rising edge, while buck 2 is synchronized with the clock-signal falling edge. The preboost enables the low-side switch (DL3) with the rising edge of the cycle while buck 1 turns on its high-side nMOSFET (DH1).

The devices can be synchronized to an external clock by connecting the external clock signal to FSYNC. A rising edge on FSYNC resets the internal clock. Keep the FSYNC frequency between 110% and 125% of the internal frequency. The FSYNC signal should have a 50% duty cycle.

Light-Load Efficiency Skip Mode (V_{FSYNC} = 0V)

Drive FSYNC low to enable skip mode. In skip mode, the devices stop switching until the FB voltage drops below the reference voltage. Once the FB voltage has dropped below the reference voltage, the devices begin switching until the inductor current reaches 30% (skip threshold) of the maximum current defined by the inductor DCR or output shunt resistor.

Forced-PWM Mode (V_{FSYNC})

Driving FSYNC high prevents the devices from entering skip mode by disabling the zero-crossing detection of the inductor current. This forces the low-side gate-driver waveform to constantly be the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads and discharges the output capacitor. The benefit of forced PWM mode is to keep the switching frequency constant under all load conditions. However, forced-frequency operation diverts a considerable amount of the output current to PGND, reducing the efficiency under light-load conditions.

Forced-PWM mode is useful for improving load-transient response and eliminating unknown frequency harmonics that can interfere with AM radio bands.

Maximum Duty-Cycle Operation

The devices have a maximum duty cycle of 95%. The internal logic of the IC looks for approximately 8 to 10 consecutive high-side FET ON pulses and decides to turn ON the low-side FET for 150ns (typ) every 12µs. The input voltage at which the devices enter dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design. The input voltage at which the devices enter dropout can be approximated as:

$$V_{OUT} = [V_{OUT} + (I_{OUT} \times R_{ON\_H})]/0.95$$

Note: The above equation does not take into account the efficiency and switching frequency, but is a good first-order approximation. Use the R_{ON_H} max number from the data sheet of the high-side MOSFET used.

Spread Spectrum

The MAX17231AGLS/MAX17231AGLU/MAX17230AGLS feature enhanced EMI performance. They perform ±6% dithering of the switching frequency to reduce peak emission noise at the clock frequency and its harmonics, making it easier to meet stringent emission limits. When using an external clock source (i.e., driving the FSYNC input with an external clock), spread spectrum is disabled.

MOSFET Gate Drivers (DH_ and DL_)

The DH_ high-side nMOSFET drivers are powered from capacitors at BST_ while the low-side drivers (DL_) are powered by the 5V linear regulator (BIAS). On each channel, a shoot-through protection circuit monitors the gate-to-source voltage of the external MOSFETs to prevent a MOSFET from turning on until the complementary switch is fully off. There must be a low-resistance, low-inductance path from the DL_ and DH_ drivers to the MOSFET gates for the protection circuits to work properly. Follow the instructions listed to provide the necessary low-resistance and low-inductance path:

- Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

It may be necessary to decrease the slew rate for the gate drivers to reduce switching noise or to compensate for low-gate charge capacitors. For the low-side drivers, use gate capacitors in the range of 1nF to 5nF from DL_ to GND. For the high-side drivers, connect a small 5Ω to 10Ω resistor between BST_ and the bootstrap capacitor.

Note: Gate drivers must be protected during shutdown, at the absence of the supply voltage (V_{BIAS} = 0V) when the gate is pulled high either capacitively or by the leakage path on the PCB. Therefore, external gate pulldown resistors are needed, especially at DL3 to prevent making a direct path from V_{BAT} to GND.

High-Side Gate-Driver Supply (BST_)

The high-side MOSFET is turned on by closing an internal switch between BST_ and DH_ and transferring the bootstrap capacitor's (at BST_) charge to the gate of the high-side MOSFET. This charge refreshes when the high-side MOSFET turns off and the LX_ voltage drops down to ground potential, taking the negative terminal of the capacitor to the same potential. At this time the bootstrap diode recharges the positive terminal of the bootstrap capacitor.

The selected n-channel high-side MOSFET determines the appropriate boost capacitance values ($C_{BST\_}$ in the *Typical Operating Circuit*) according to the following equation:

$$I_{FAULT} < \frac{V_{IN} \times t_{ON,MIN}[s] \times f_{SW}[Hz]}{R_{DCR} + R_{ON} + R_{SH}}$$

where Q_G is the total gate charge of the high-side MOSFET and $\Delta V_{BST\_}$ is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose $\Delta V_{BST\_}$ such that the available gate-drive voltage is not significantly degraded (e.g., $\Delta V_{BST\_}$ = 100mV to 300mV) when determining $C_{BST\_}$. The boost capacitor should be a low-ESR ceramic capacitor. A minimum value of 100nF works in most cases.

Current Limiting and Current-Sense Inputs (OUT_ and CS_)

The current-limit circuit uses differential current-sense inputs (OUT_ and CS_) to limit the peak inductor current. If the magnitude of the current-sense signal exceeds the current-limit threshold ($V_{LIMIT1,2}$ = 80mV (typ)), the PWM controller turns off the high-side MOSFET. The actual maximum load current is less than the peak current-limit threshold by an amount equal to half of the inductor ripple current. Therefore, the maximum load capability is a function of the current-sense resistance, inductor value, switching frequency, and duty cycle ($V_{OUT\_}/V_{IN}$).

For the most accurate current sensing, use a current-sense shunt resistor (R_{SH}) between the inductor and the output capacitor. Connect CS_ to the inductor side of R_{SH} and OUT_ to the capacitor side. Dimension R_{SH} such that the maximum inductor current ($I_{L,MAX} = I_{LOAD,MAX}$+1/2 $I_{RIPPLE,PP}$) induces a voltage of $V_{LIMIT1,2}$ across R_{SH} including all tolerances. For higher efficiency, the current can also be measured directly across the inductor. This method could cause up to 30% error over the entire temperature range and requires a filter network in the current-sense circuit. See the *Current-Sense Measurement* section.

Voltage Monitoring (PGOOD_)

The MAX17230/MAX17231 include several power monitoring signals to facilitate power-supply sequencing and supervision. PGOOD_ can be used to enable circuits that are supplied by the corresponding voltage rail, or to turn on subsequent supplies.

Each PGOOD_ goes high (high impedance) when the corresponding regulator output voltage is in regulation. Each PGOOD_ goes low when the corresponding regulator output voltage drops below 15% (typ) or rises above 15% (typ) of its nominal regulated voltage. Connect a 10kΩ (typ) pullup resistor from PGOOD_ to the relevant logic rail to level-shift the signal. PGOOD_ asserts low during soft-start, soft-discharge, and when either buck converter is disabled (either EN1 or EN2 is low). To ensure latchup immunity on the PGOOD1 pin, a minimum resistance of 100Ω should be placed between the PGOOD1 pin and any other external components.

Preboost

The MAX17230/MAX17231 include an non-synchronous current-mode preboost with adjustable output. This preboost can be used independently, but is ideally suited for applications that need to stay fully functional during input voltage dropouts typical in systems that have an the input voltage that varies over a wide range and where the input voltage can drop below the output voltage.

The preboost is turned on by bringing EN3 high and meeting the INS requirement.

EN3 can be used for power-supply sequencing and implementing a boost timeout to prevent overheating the components used for the boost converter.

While the boost circuit is essential to maintain functionality during undervoltage events, it reduces system efficiency. During normal operation, the boost diode dissipates power and the resistive dividers at INS and FB3 sink significant amounts of quiescent current. To ensure latch-up immunity on the INS and FB3 pins, ensure that the parallel combination of this resistor-divider network used on these pins is > 500ω.

Supply Monitoring (INS)

The devices include a dedicated voltage sensor at INS to quickly detect overvoltage and undervoltage for the boost converter input power.

The boost converter turns off when EN3 is low. When EN3 is high AND:

- INS voltage rises above 0.35V or falls below 1.15V (normal input range): Boost turns on
- INS voltage rises above 1.25V or falls below 0.3V (OV or UV): Boost turns off

Connect INS to the center tap of a resistive divider from the input voltage (battery) to TERM to set the proper turn-on/turn-off of the preboost. If this setting is not sufficient, optimize the divider for the most critical level. For the MAX17231ATLV/V+ and MAX17231ATLW/V+, the INS pin functionality is disabled; however, the INS pin should still be connected using the resistor-divider between V_{BAT} and the TERM pin, as explained above.

Increasing the Efficiency of the Boost Circuit (TERM)

The MAX17230/MAX17231 provide a feature to improve the efficiency of the boost circuit when it is not active:

- TERM provides a switch to GND for the INS and FB3 voltage-dividers. This switch opens during standby mode and shutdown mode to reduce the quiescent current by 240μA, assuming that resistors used in the voltage-divider network are in the range of 100kΩ.

Preboost nMOSFET Driver (DL3)

DL3 drives the gate of an external nMOSFET. The driver is powered by the 5V (typ) internal regulator (BIAS) or the external bypass supply (EVTVCC). DL3 asserts low during standby mode.

Switching Frequency in Boost Controller

The preboost switching frequency (f_{BOOST}) is derived from the buck controllers switching frequency (f_{SW}) by setting FOSC. See the *Electrical Characteristics* table. On the MAX17231, f_{BOOST} can be set equal to f_{SW} by connecting FBSTSEL to ground or to $1/5f_{SW}$ by connecting FBSTSEL to BIAS. The gate driver of the preboost turns on simultaneously with the high-side driver of buck 1. FSELBST should be connected to ground on the MAX17230.

Current Limit in Boost Controller

A current-sense resistor (R_{CS}), connected CS3P and CS3N, sets the current limit of the boost converter. The CS input has a voltage trip level (V_{CS}) of 120mV (typ). The low 120mV current-limit threshold reduces the power dissipation in the current-sense resistor. Use a current-sense filter to reduce capacitive coupling during turn on. See the *Shunt Resistor Selection in Boost Converter* section.

Thermal-Overload, Overcurrent, and Overvoltage and Undervoltage Behavior

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the devices. When the junction temperature exceeds +170°C, an internal thermal sensor shuts down the devices, allowing them to cool. The thermal sensor turns on the devices again after the junction temperature cools by 20°C.

Overcurrent Protection

If the inductor current on the MAX17231 and MAX17230 exceed the maximum current limit programmed at CS_ and OUT_, the respective driver turns off. In an overcurrent mode, this results in shorter and shorter high-side pulses.

A hard short results in a minimum on-time pulse every clock cycle.

Choose the components so they can withstand the short-circuit current if required.

Overvoltage Protection

The devices limit the output voltage of the buck converters by turning off the high-side gate driver at approximately 115% of the regulated output voltage. The output voltage needs to come back in regulation before the high-side gate driver starts switching again.

Design Procedure

Buck Converter Design Procedure

Effective Input Voltage Range in Buck Converters

Although the MAX17230/MAX17231 can operate from input supplies up to 36V (42V transients) and regulate down to 1V, the minimum voltage conversion ratio (V_{OUT}/V_{IN}) might be limited by the minimum controllable on-time. For proper fixed-frequency PWM operation and optimal efficiency, buck 1 and buck 2 should operate in continuous conduction during normal operating conditions. For continuous conduction, set the voltage conversion ratio as follows:

$$\frac{V_{OUT}}{V_{IN}} > t_{ON(MIN)} \times f_{SW}$$

where $t_{ON(MIN)}$ is 50ns (typ) and f_{SW} is the switching frequency in Hz. If the desired voltage conversion does not meet the above condition, pulse skipping occurs to decrease the effective duty cycle. Decrease the switching frequency if constant switching frequency is required. The same is true for the maximum voltage conversion ratio.

The maximum voltage conversion ratio is limited by the maximum duty cycle (95%).

$$\frac{V_{OUT}}{V_{IN} - V_{DROP}} < 0.95$$

where $V_{DROP} = I_{OUT}(R_{ON,HS} + R_{DCR})$ is the sum of the parasitic voltage drops in the high-side path and f_{SW} is the programmed switching frequency. During low drop operation, the devices reduce f_{SW} to 25% (max) of the programmed frequency. In practice, the above condition should be met with adequate margin for good load-transient response.

Setting the Output Voltage in Buck Converters

Connect FB1 and FB2 to BIAS to enable the fixed buck controller output voltages (5V and 3.3V) set by a preset internal resistive voltage-divider connected between the feedback (FB_) and AGND. To externally adjust the output voltage between 1V and 10V, connect a resistive divider from the output (OUT_) to FB_ to AGND (see the *Typical Operating Circuit*. Calculate R_{FB_1} and R_{FB_2} with the following equation:

$$R_{FB\_1} = R_{FB\_2}\left[\left(\frac{V_{OUT\_}}{V_{FB\_}}\right) - 1\right]$$

where $V_{FB\_}$ = 1V (typ) (see the *Electrical Characteristics* table).

DC output accuracy specifications in the *Electrical Characteristics* table refer to the error comparator's threshold, $V_{FB\_}$ = 1V (typ). When the inductor conducts continuously, the devices regulate the peak of the output ripple, so the actual DC output voltage is lower than the slope-compensated trip level by 50% of the output ripple voltage.

In discontinuous conduction mode (skip or STDBY active and $I_{OUT} < I_{LOAD(SKIP)}$), the devices regulate the valley of the output ripple, so the output voltage has a DC regulation level higher than the error-comparator threshold.

Inductor Selection in Buck Converters

Three key inductor parameters must be specified for operation with the MAX17230/MAX17231: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To determine the optimum inductance, knowing the typical duty cycle (D) is important.

$$D = \frac{V_{OUT}}{V_{IN}} \text{ OR } D = \frac{V_{OUT}}{V_{IN} - I_{OUT}(R_{DS(ON)} + R_{DCR})}$$

if the R_{DCR} of the inductor and $R_{DS(ON)}$ of the MOSFET are available with $V_{IN} = (V_{BAT} - V_{DIODE})$. All values should be typical to optimize the design for normal operation.

Inductance

The exact inductor value is not critical and can be adjusted in order to make trade-offs among size, cost, efficiency, and transient response requirements.

- Lower inductor values increase LIR, which minimizes size and cost and improves transient response at the cost of reduced efficiency due to higher peak currents.
- Higher inductance values decrease LIR, which increases efficiency by reducing the RMS current at the cost of requiring larger output capacitors to meet load-transient specifications.

The ratio of the inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good initial value is a 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determine the inductor value as follows:

$$L[\mu H] = \frac{(V_{IN} - V_{OUT}) \times D}{f_{SW}[MHz] \times I_{OUT} \times LIR}$$

where V_{IN}, V_{OUT}, and I_{OUT} are typical values (so that efficiency is optimum for typical conditions).

Peak Inductor Current

Inductors are rated for maximum saturation current. The maximum inductor current equals the maximum load current in addition to half of the peak-to-peak ripple current:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}$$

For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is calculated as:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

where $\Delta I_{INDUCTOR}$ is in mA, L is in µH, and f_{SW} is in kHz.

Once the peak current and the inductance are known, the inductor can be selected. The saturation current should be larger than I_{PEAK} or at least in a range where the inductance does not degrade significantly. The MOSFETs are required to handle the same range of current without dissipating too much power.

MOSFET Selection in Buck Converters

Each step-down controller drives two external logic-level n-channel MOSFETs as the circuit switch elements. The key selection parameters to choose these MOSFETs include the items in the following sections.

Threshold Voltage

All four n-channel MOSFETs must be a logic-level type with guaranteed on-resistance specifications at V_{GS} = 4.5V. If the internal regulator is bypassed (for example: V_{EXTVCC} = 3.3V), then the nMOSFETs should be chosen to have guaranteed on-resistance at that gate-to-source voltage.

Maximum Drain-to-Source Voltage ($V_{DS(MAX)}$)

All MOSFETs must be chosen with an appropriate V_{DS} rating to handle all V_{IN} voltage conditions.

Current Capability

The nMOSFETs must deliver the average current to the load and the peak current during switching. Choose MOSFETs with the appropriate average current at V_{GS} = 4.5V or V_{GS} = V_{EXTVCC} when the internal linear regulator is bypassed. For load currents below approximately 3A, dual MOSFETs in a single package can be an economical solution. To reduce switching noise for smaller MOSFETs, use a series resistor in the BST_ path and additional gate capacitance. Contact the factory for guidance using gate resistors.

Current-Sense Measurement

For the best current-sense accuracy and overcurrent protection, use a ±1% tolerance current-sense resistor between the inductor and output as shown in Figure 1A. This configuration constantly monitors the inductor current, allowing accurate current-limit protection. Use low-inductance current-sense resistors for accurate measurement.

Alternatively, high-power applications that do not require highly accurate current-limit protection can reduce the overall power dissipation by connecting a series RC circuit across the inductor (Figure 1B) with an equivalent time constant:

$$R_{CSHL} = \left(\frac{R2}{R1 + R2}\right) R_{DCR}$$

and:

$$R_{DCR} = \frac{L}{C_{EQ}}\left(\frac{1}{R1} + \frac{1}{R2}\right)$$

where R_{CSHL} is the required current-sense resistor and R_{DCR} is the inductor's series DC resistor. Use the inductance and R_{DCR} values provided by the inductor manufacturer.

Carefully observe the PCB layout guidelines to ensure the noise and DC errors do no corrupt the differential current-sense signals seen by CS_ and OUT_. Place the sense resistor close to the devices with short, direct traces, making a Kelvin-sense connection to the current-sense resistor.

Input Capacitor in Buck Converters

The discontinuous input current of the buck converter causes large input ripple currents and therefore the input capacitor must be carefully chosen to withstand the input ripple current and keep the input voltage ripple within design requirements. The 180° ripple phase operation increases the frequency of the input capacitor ripple current to twice the individual converter switching frequency. When using ripple phasing, the worst-case input capacitor ripple current is when the converter with the highest output current is on.

The input voltage ripple is composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR} that peaks at the end of an on-cycle. Calculate the input capacitance and ESR required for a specific ripple using the following equation:

$$ESR[\Omega] = \frac{\Delta V_{ESR}}{\left(I_{LOAD(MAX)} + \frac{\Delta I_{P-P}}{2}\right)}$$

$$C_{IN}[\mu F] = \frac{I_{LOAD(MAX)} \times \left(\frac{V_{OUT}}{V_{IN}}\right)}{\left(\Delta V_Q \times f_{SW}\right)}$$

where:

$$\Delta I_{P-P} = \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

$I_{LOAD(MAX)}$ is the maximum output current in A, ΔI_{P-P} is the peak-to-peak inductor current in A, f_{SW} is the switching frequency in MHz, and L is the inductor value in µH.

The internal 5V linear regulator (BIAS) includes an output UVLO with hysteresis to avoid unintentional chattering during turn-on. Use additional bulk capacitance if the input source impedance is high. At lower input voltage, additional input capacitance helps avoid possible undershoot below the undervoltage lockout threshold during transient loading.

Output Capacitor in Buck Converters

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. The capacitor is usually selected by ESR and the voltage rating rather than by capacitance value.

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from

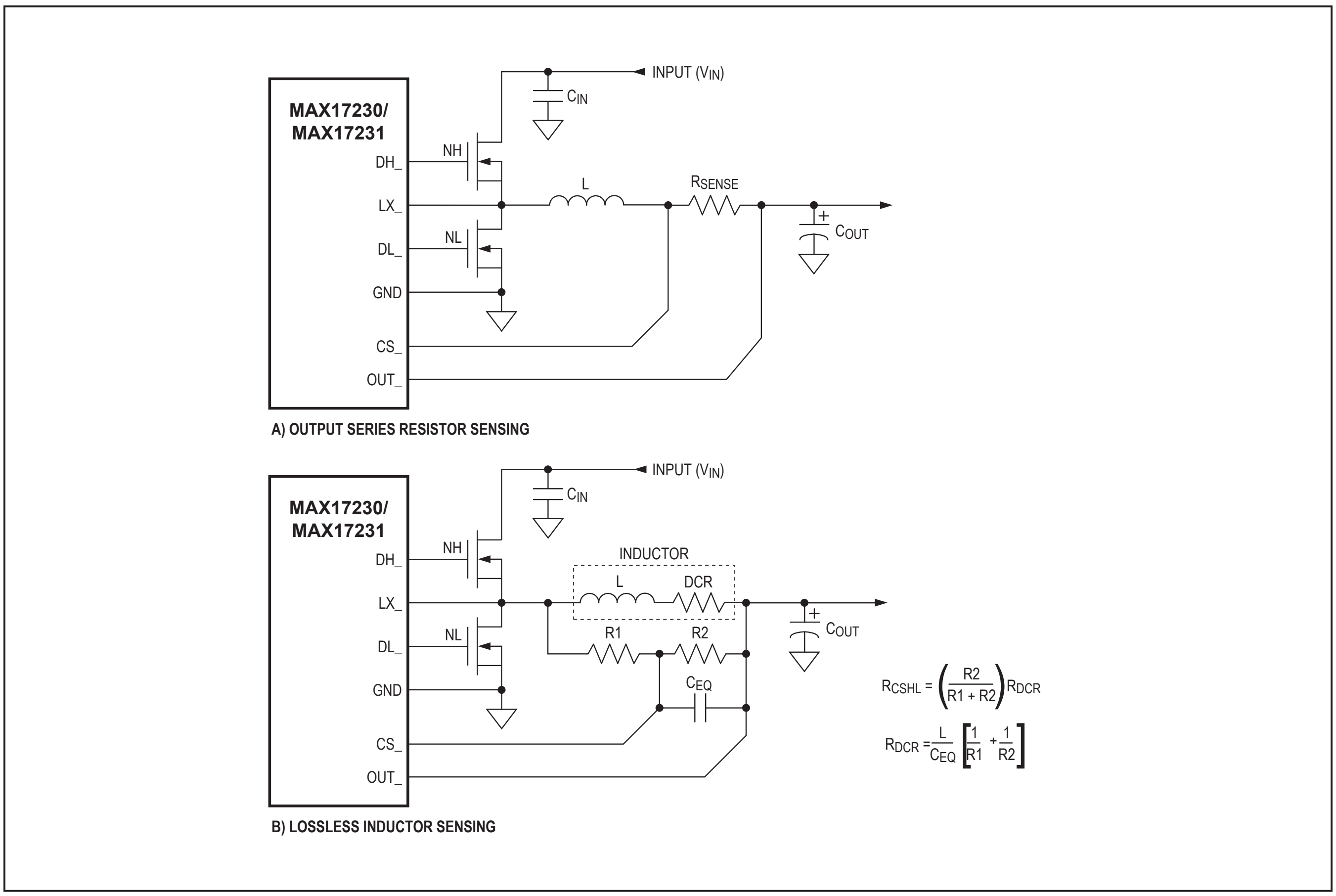


Figure 1. Current-Sense Configurartions

causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the *Transient Considerations* section). However, low-capacity filter capacitors typically have high-ESR zeros that can affect the overall stability.

The total voltage sag (V_{SAG}) can be calculated as follows:

$$V_{SAG} = \frac{L(\Delta I_{LOAD(MAX)})^2}{2C_{OUT}((V_{IN} \times D_{MAX}) - V_{OUT})} + \frac{\Delta I_{LOAD(MAX)}(t - \Delta t)}{C_{OUT}}$$

The amount of overshoot (V_{SOAR}) during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{(\Delta I_{LOAD(MAX)})^2 L}{2C_{OUT} V_{OUT}}$$

ESR Considerations

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output-voltage ripple. So the output capacitor's size depends on the maximum ESR required to meet the output-voltage ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$$

In standby mode, the inductor current becomes discontinuous, with peak currents set by the idle-mode current-sense threshold ($V_{CS,SKIP}$ = 26mV (typ)).

Transient Considerations

The output capacitor must be large enough to absorb the inductor energy while transitioning from no-load to full-load condition without tripping the overvoltage fault protection. The total output-voltage sag is the sum of the voltage sag while the inductor is ramping up and the voltage sag before the next pulse can occur. Therefore:

$$C_{OUT} = \frac{L(\Delta I_{LOAD(MAX)})^2}{2V_{SAG}(V_{IN} \times D_{MAX} - V_{OUT})} + \frac{\Delta I_{LOAD(MAX)}(t - \Delta t)}{V_{SAG}}$$

where D_{MAX} is the maximum duty factor (approximately 95%), L is the inductor value in µH, C_{OUT} is the output capacitor value in µF, t is the switching period ($1/f_{SW}$) in µs, and Δt equals (V_{OUT}/V_{IN}) x t.

The devices use a current-mode-control scheme that regulates the output voltage by forcing the required current through the external inductor, so the controller uses the voltage drop across the DC resistance of the inductor or the alternate series current-sense resistor to measure the inductor current. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor resulting in a smaller phase shift and requiring less elaborate error-amplifier compensation than voltage-mode control. A single series resistor (R_C) and capacitor (C_C) is all that is required to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering (see Figure 2). For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a nonceramic output capacitor loop, add another compensation capacitor (C_F) from COMP to AGND to cancel this ESR zero.

The basic regulator loop is modeled as a power modulator, output feedback divider, and an error amplifier as shown in Figure 2. The power modulator has a DC gain set by g_{mc} x R_{LOAD}, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR. The loop response is set by the following equations:

$$GAIN_{MOD(dc)} = g_{mc} \times R_{LOAD}$$

where R_{LOAD} = $V_{OUT}/I_{LOUT(MAX)}$ in Ω and g_{mc} = $1/(A_{V\_CS}$ x $R_{DC})$ in S. A_{V_CS} is the voltage gain of the current-sense amplifier and is typically 11V/V. R_{DC} is the DC resistance of the inductor or the current-sense resistor in Ω.

In a current-mode step-down converter, the output capacitor and the load resistance introduce a pole at the following frequency:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}}$$

The unity gain frequency of the power stage is set by C_{OUT} and g_{mc}:

$$f_{UGAINpMOD} = \frac{g_{mc}}{2\pi \times C_{OUT}}$$

The output capacitor and its ESR also introduce a zero at:

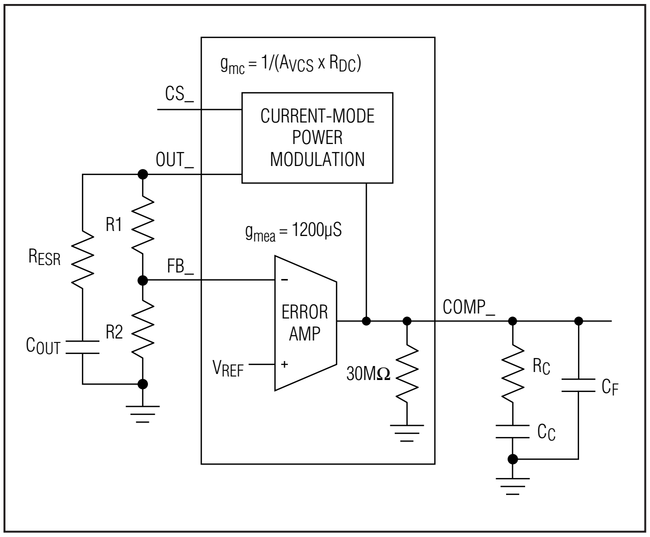


Figure 2. Compensation Network

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

When C_{OUT} is composed of "n" identical capacitors in parallel, the resulting C_{OUT} = n x $C_{OUT(EACH)}$, and ESR = $ESR_{(EACH)}$/n. Note that the capacitor zero for a parallel combination of alike capacitors is the same as for an individual capacitor.

The feedback voltage-divider has a gain of $GAIN_{FB}$ = V_{FB}/V_{OUT}, where V_{FB} is 1V (typ).

The transconductance error amplifier has a DC gain of $GAIN_{EA(DC)}$ = $g_{m,EA}$ x $R_{OUT,EA}$, where $g_{m,EA}$ is the error amplifier transconductance, which is 1200µS (typ), and $R_{OUT,EA}$ is the output resistance of the error amplifier, which is 30MΩ (typ) (see the *Electrical Characteristics* table.)

A dominant pole (f_{dpEA}) is set by the compensation capacitor (C_C) and the amplifier output resistance ($R_{OUT,EA}$). A zero (f_{ZEA}) is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole (f_{PEA}) set by C_F and R_C to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C), where the loop gain equals 1 (0dB)). Thus:

$$f_{dpEA} = \frac{1}{2\pi \times C_C \times (R_{OUT,EA} + R_C)}$$

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C}$$

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C}$$

The loop-gain crossover frequency (f_C) should be set below 1/5th of the switching frequency and much higher than the power-modulator pole (f_{pMOD}). Select a value for f_C in the range:

$$f_{pMOD} \ll f_C \le \frac{f_{SW}}{5}$$

At the crossover frequency, the total loop gain must be equal to 1. So:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB}}{V_{OUT}} \times GAIN_{EA(f_C)} = 1$$

$$GAIN_{EA(f_C)} = g_{m,EA} \times R_C$$

$$GAIN_{MOD(f_C)} = GAIN_{MOD(dc)} \times \frac{f_{pMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m,EA} \times R_C = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT}}{g_{m,EA} \times V_{FB} \times GAIN_{MOD(f_C)}}$$

Set the error-amplifier compensation zero formed by R_C and C_C at the f_{pMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor C_F from COMP to AGND. The value of C_F is:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly and the crossover frequency remains the same.

Below is a numerical example to calculate the compensation network component values of Figure 2:

A_{V_CS} = 11V/V

R_{DCR} = 15mΩ

g_{mc} = 1/(A_{V_CS} x R_{DC}) = 1/(11 x 0.015) = 6.06

V_{OUT} = 5V

$I_{OUT(MAX)}$ = 5.33A

R_{LOAD} = V_{OUT}/$I_{OUT(MAX)}$ = 5V/5.33A = 0.9375Ω

C_{OUT} = 2x47µF = 94µF

ESR = 9mΩ/2 = 4.5mΩ

f_{SW} = 26.4/65.5kΩ = 0.403MHz

$$GAIN_{MOD(dc)} = 6.06 \times 0.9375 = 5.68$$

$$f_{pMOD} = \frac{1}{2\pi \times 94\mu F \times 0.9375} \approx 1.8kHz$$

$$f_{pMOD} << f_C \le \frac{f_{SW}}{5}$$

$$1.8kHz << f_C \le 80.6kHz$$

select f_C = 40kHz

$$f_{zMOD} = \frac{1}{2\pi \times 4.5m\Omega \times 94\mu F} \approx 376kHz$$

since f_{zMOD} > f_C:

R_C ≈ 16kΩ

C_C ≈ 5.6nF

C_F ≈ 27pF

Boost Converter Design Procedure

Setting the Output Voltage in Boost Converter

Adjust the boost converter output voltage by connecting a resistive divider from the output of the boost converter to FBBST to TERM (Figure 3) and R_{B2} (FB3 to TERM resistor). Calculate R_{B1} ($V_{OUT(BOOST)}$ to FBBST resistor) using the following equation:

$$R_{B1} = R_{B2}\left[\left(\frac{V_{OUT(BOOST)}}{V_{FB3}}\right) - 1\right]$$

where V_{FB3} = 1.2V (typ) (see the *Electrical Characteristics* table).

Inductor Selection in Boost Converter

Duty cycle and frequency are important to calculate the inductor size, as the inductor current ramps up during the on-time of the switch and ramps down during its off-time. A higher switching frequency generally improves transient response and reduces component size.

However, if the boost components are to be used as the input filter components during nonboost operation, a low frequency is advantageous.

The boost frequency is selected as a multiple of the buck frequency by setting the input voltage of FSELBST.

- If $V_{FSELBST}$ =V_{GND}, then f_{BOOST} = f_{SW}
- If $V_{FSELBST}$ = V_{BIAS}, then f_{BOOST} = 1/5f_{SW}

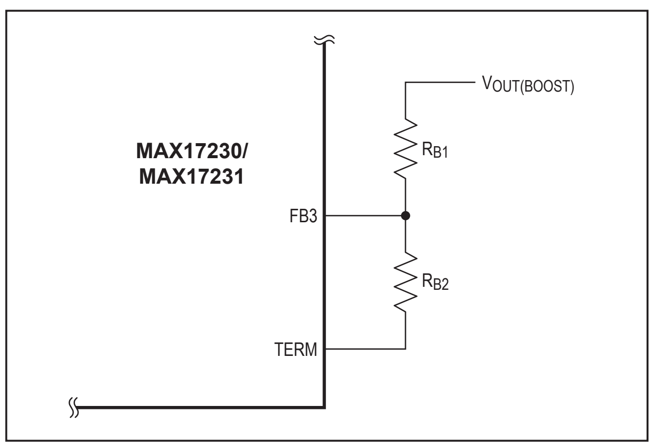


Figure 3. Boost Converter Adjustable Output Voltage

The duty-cycle range of the boost converter depends on the effective input to output-voltage ratio. In the following calculations, the duty cycle refers to the on-time of the boost MOSFET:

$$D_{MAX} = \frac{V_{OUT(MAX)} - V_{BAT(MIN)}}{V_{OUT(MAX)}}$$

or including the voltage drops across the inductor, MOSFET ($V_{ON,FET}$), and the boost diode (V_D):

$$D_{MAX} = \frac{V_{OUT(MAX)} - V_{BAT(MIN)} + V_D + (I_{OUT} \times R_{DC})}{V_{OUT(MAX)}}$$

In some applications, it may be beneficial to maintain discontinuous conduction (DCM) in the boost converter under all conditions. This formula defines the maximum size of the inductor for DCM mode:

$$L_{MAX} < V_{IN(MIN)} \text{ x } D_{MAX}/(2 \text{ x } (I_{OUT(MAX)}/1 - D_{MAX})) \text{ x } f_{SW(MIN)}$$

The ratio of the inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good initial value is a 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR determine the inductor value as follows:

$$L[\mu H] = \frac{V_{IN} \times D}{f_{SW}[MHz] \times LIR}$$

where:

$D = (V_{OUT} - V_{IN})/V_{OUT}$
V_{IN} = Typical input voltage
V_{OUT} = Typical output voltage

LIR = 0.3 x I_{OUT}/1 - D

Select the inductor with a saturation current rating higher than the peak switch current limit of the converter:

$$I_{L,PEAK} > I_{L,MAX} + \frac{\Delta I_{L,RIP,MAX}}{2}$$

Running a boost converter in continuous conduction mode introduces a right-half plane zero into the transfer function, which can only be compensated by reducing bandwidth in the voltage feedback loop by adding a capacitor across the low-side feedback resistor. This results in a system that is slow to respond to load and line changes.

If the boost converter response is too slow, increase the ripple current. A smaller inductor and higher frequency generally improves the preboost, especially for high input to output ratios.

MOSFET Selection in Boost Converter

The key selection parameters to choose the nMOSFET used in the boost converter are as follows.

Threshold Voltage

The boost nMOSFETs must be a logic-level type with guaranteed on-resistance specifications at V_{GS} = 4.5V.

Maximum Drain-to-Source Voltage ($V_{DS(MAX)}$)

The MOSFET must be chosen with an appropriate V_{DS} rating to handle all V_{IN} voltage conditions.

Current Capability

The nMOSFET must deliver the input current ($I_{IN(MAX)}$):

$$I_{IN(MAX)} = I_{LOAD(MAX)} \text{ x } \frac{D_{MAX}}{1 - D_{MAX}}$$

Choose MOSFETs with the appropriate average current at V_{GS} = 4.5V.

Diode Selection in Boost Converter

The diode must deliver the average output current (I_{OUT}) plus the peak inductor current (I_{LPEAK}). The boost diode current can be higher during nonboost operation when it supplies current to both buck converters under full-load conditions.

Use a boost diode with a power dissipation of P = I_{OUT} x V_{DIODE} or higher. To reduce the power dissipation, use a Schottky diode.

Input Capacitor Selection in Boost Converter

The input current for the boost converter is continuous and the RMS ripple current at the input capacitor is low. Calculate the minimum input capacitor value and maximum ESR using the following equations:

$$C_{BAT} = \frac{\Delta I_L \text{ x } D}{4 \text{ x } f_{SW} \text{ x } \Delta V_Q}$$

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_L}$$

where:

$$\Delta I_L = \frac{(V_{BAT} - V_{DS}) \times D}{L \times f_{SW}}$$

V_{DS} is the total voltage drop across the external MOSFET plus the voltage drop across the inductor ESR. ΔI_L is peak-to-peak inductor ripple current as calculated above. ΔV_Q is the portion of input ripple due to the capacitor discharge and ΔV_{ESR} is the contribution due to ESR of the capacitor. Assume the input capacitor ripple contribution due to ESR (ΔV_{ESR}) and capacitor discharge (ΔV_Q) are equal when using a combination of ceramic and aluminum capacitors. During the converter turn-on, a large current is drawn from the input source especially at high output-to-input differential.

Output Capacitor Selection in Boost Converter

In a boost converter, the output capacitor supplies the load current when the boost MOSFET is on. The required output capacitance is high, especially at higher duty cycles. Also, the output capacitor ESR needs to be low enough to minimize the voltage drop while supporting the load current. Use the following equations to calculate the output capacitor for a specified output ripple. All ripple values are peak-to-peak.

$$ESR = \frac{\Delta V_{ESR}}{I_{OUT}}$$

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{\Delta V_Q \times f_{SW}}$$

I_{OUT} is the load current in A, f_{SW} is in MHz, C_{OUT} is µF, ΔV_Q is the portion of the ripple due to the capacitor discharge, and ΔV_{ESR} is the contribution due to the ESR of the capacitor. D_{MAX} is the maximum duty cycle at the minimum input voltage. Use a combination of low-ESR ceramic and high-value, low-cost aluminum capacitors for lower output ripple and noise.

Shunt Resistor Selection in Boost Converter

The current-sense resistor (R_{CS}), connected between the battery and the inductor, sets the current limit. The CS input has a voltage trip level (V_{CS}) of 120mV (typ).

Set the current-limit threshold high enough to accommodate the component variations. Use the following equation to calculate the value of R_{CS}:

$$R_{CS} = \frac{V_{CS}}{I_{IN(MAX)}}$$

where $I_{IN(MAX)}$ is the peak current that flows through the MOSFET at full load and minimum V_{IN}.

$$I_{IN(MAX)} = I_{LOAD(MAX)} / (1 - D_{MAX})$$

When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (DL3) quickly terminates the on-cycle.