Simple cell balancer

EDLC cell balance LSI
BD14000EFV-C evaluation board

BD14000EFV-EVK-001

Summary

BD14000EFV-EVK-001 realizes stand-alone cell balance of 4-6 cell series EDLC using EDLC cell balance LSI (BD14000EFV-C). The cell balance current can be set by shunt resistance. In addition, the cell balance voltage is setable, too.

Performance specifications (this is a representative figure and characteristic is not guaranteed)

VIN = 15V, unless otherwise specified

Parameter	Min	Typ	Max	Units	Conditions
Input voltage range	8.0		24	V	
Cell balance current		100		mA	Vcn-Vcn-1 = 2.5V

Cell balance detection voltage setting : It is setable at VCB = 2.4-3.1V (0.1V step)
Overvoltage detection voltage setting 1 : It is setable at VOVLO1 = VCB+0.15V or 0.25V
Overvoltage detection voltage setting 2 : It is setable at VOVLO2 = VCB+0.30V or 0.50V

Operating procedure

1. Necessary apparatus
   (1) EDLC from 4 cell to 6 cell
   (2) The constant current power supply which is available for voltage upper limit setting
   (3) Monitor with the oscilloscope or DC voltmeter

2. Connection of an apparatus
   (1) Connect EDLC to a board by soldering.
   (2) Connect a constant current power supply to plus side of the high-end cell of EDLC and minus side of the last cell and set a charge current and a voltage upper limit level.
   (3) Set the detection voltage by VSET0-2,OVLOSEL pin setting. (please set it in either H/L by all means.)
   (4) Set ENIN pin setting in 'H' to turn on this LSI.
   (5) Turn on a constant current source and do charge ⇔ discharge.
   When cell voltage is not balanced, cell balance can be realized by repeating charge and discharge several times.
   (6) The operation can be checked by monitoring the current between each cell and a flag output terminal (Dn, OVLO1,2, OK).
   (7) At a end time of evaluation, please completely discharge EDLC by a constant current source.
   * The ENIN,VSET01,2,OVLOSEL setting, please connect a monitor pin to H:VREG/L:VSS.
   It is available to use 2 point of contact switches for the terminal logic's control.
   In that case, please implement 2 point of contact switches at the parts list.

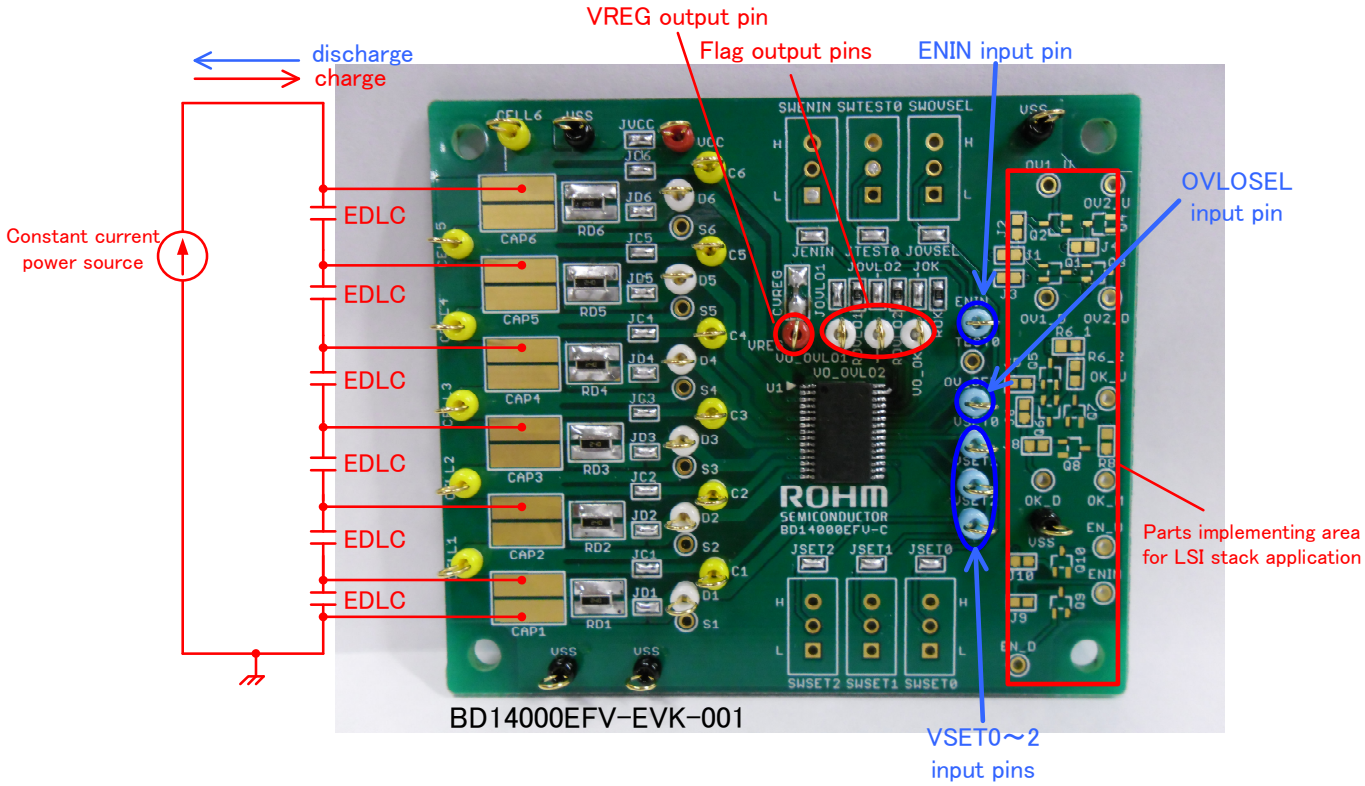


Figure 1. connection image figure

Board circuit diagram

VCC = 8.0V - 24V

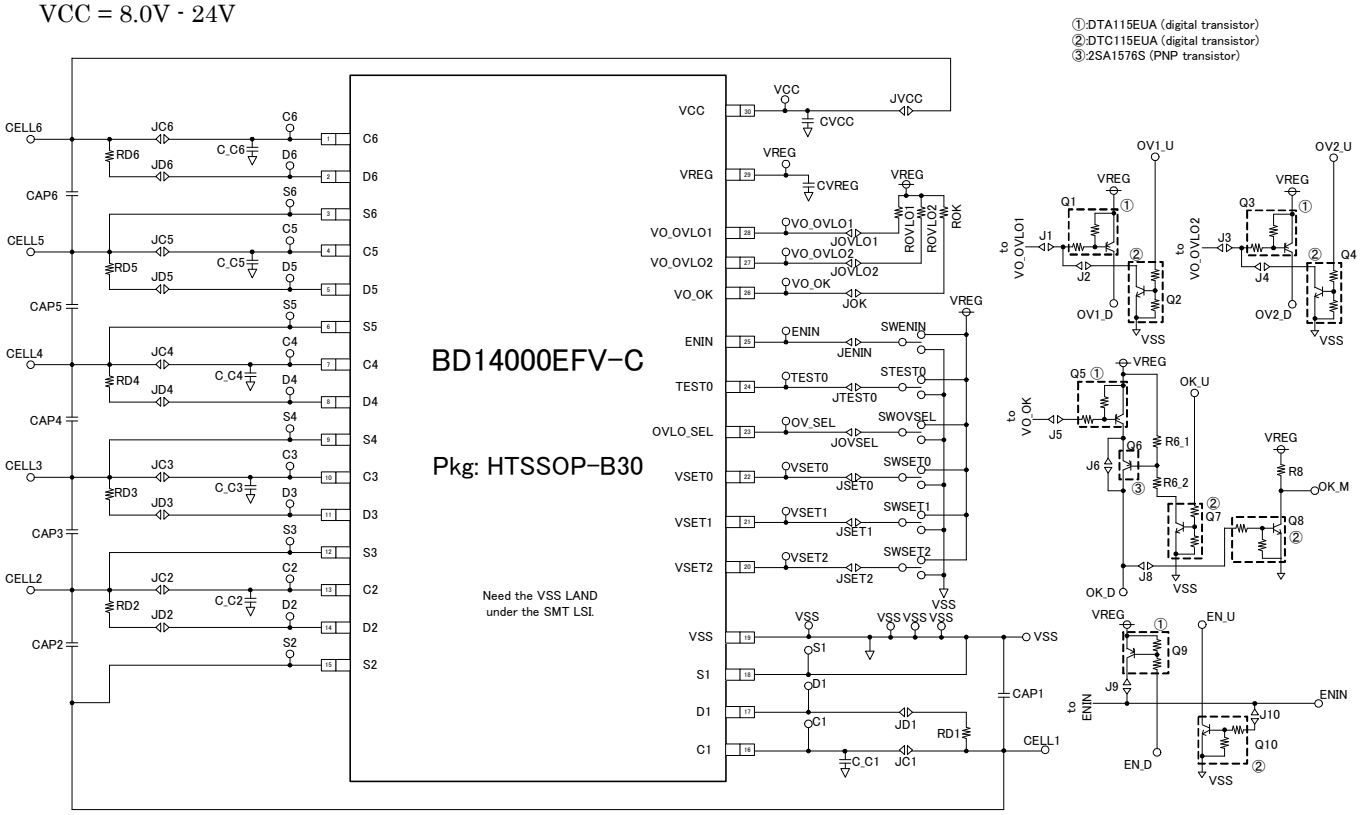


Figure 2. BD14000EFV-EVK-001 board circuit diagram

Parts list

No.	parts name	symbol	count[pcs]	value	Description	Manufacturer Parts Number	Manufacturer	Configuraton [mmxmm]
1	LSI	LSI	1	LSI	EDLC cell balance LSI	BD4000EFV-C	ROHM	HTSSOP-B30
2	shant R	RD1,2,3,4,5,6	6	24Ω	1W,200V,F(±1.0%)	LTR50	ROHM	5.0x2.5
3	capasitor	CAP1,2,3,4,5,6	0	–	not installed for EDLC connection	–	–	–
4	capasitor	C_C1,2,3,4,5,6	1	0.1uF	50V,R,±10%	GCM188R11H104KA42#	MURATA	1.6x0.8
5	capasitor	CVCC	1	1uF	50V,X7R,±10%	GCM21BR71H105KA01#	MURATA	2.0x1.25
6	capasitor	CVREG	1	1uF	16V,X7R,±10%	GCM188R71C105KA49#	MURATA	1.6x0.8
7	pullup R	ROVLO1,2,ROK	3	100kΩ	1/16W,50V,F(±1%)	MCR01	ROHM	1.0x0.5
8	switch	SWENIN,OVSEL,SET0,1,2	0	2pole switch	2 pointed swichs are not installed. If needed, please install them.	ATE1D2M3-10-Z	FUJISOKU	5.0x9.5
9	switch	SWTEST0	0	2pole switch	not installed. TEST0 is connectted to VSS.	ATE1D2M3-10-Z	FUJISOKU	5.0x9.5
10	pullup R	R6_1,R6_2,R8	0	100kΩ	1/16W,50V,F(±1%) not installed. Using for LSI stacking.	MCR01	ROHM	1.0x0.5
11	digital Tr(PNP)	Q1,3,5,9	0	digital Tr(PNP)	not installed. Using for LSI stacking.	DTA115EUA	ROHM	2.0x2.1
12	digital Tr(NPN)	Q2,4,7,8,10	0	digital Tr(NPN)	not installed. Using for LSI stacking.	DTC115EUA	ROHM	2.0x2.1
13	PNP Tr	Q6	0	PNP Tr	not installed. Using for LSI stacking.	2SA1576A	ROHM	2.0x2.1
14	pins	VREG,VCC	2	–	red pin.	–	–	1.2φ
15	pins	VSS(x5)	5	–	black pin.	–	–	1.2φ
16	pins	C1-6,CELL1-6	12	–	yellow pin.	–	–	1.2φ
17	pins	D1-6,VO_OK,VO_OVLO1-2	9	–	white pin.	–	–	1.2φ
18	pins	VSET0-2, OVLO_SEL,ENIN	12	–	sky blue pin.	–	–	1.2φ
19	pins	S1-6,TEST0	0	–	not installed. If needed, please install them.	–	–	1.2φ
20	pins	OV1-2_U,OV1-2_D,OK_U,OK_D,OD_M, EN_U,EN_D,ENIN	0	–	not installed. Using for LSI stacking.	–	–	1.2φ
21	jumper	JC1-6,JD1-6,JSET0-2,JOVSEL,JTEST0, JENIN,JOK,JOVLO1-2,JVCC	22	–	connected.	–	–	–
22	jumper	J1-6,J8-10	0	–	not connected.	–	–	–

Board layout

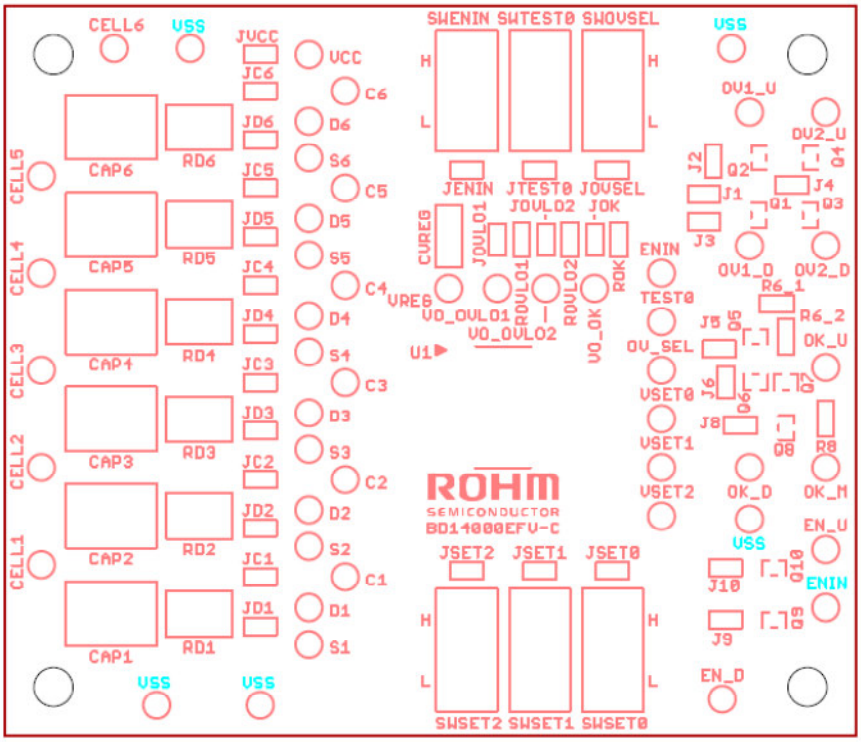


Figure 3. Top layer silkscreen (Top view)

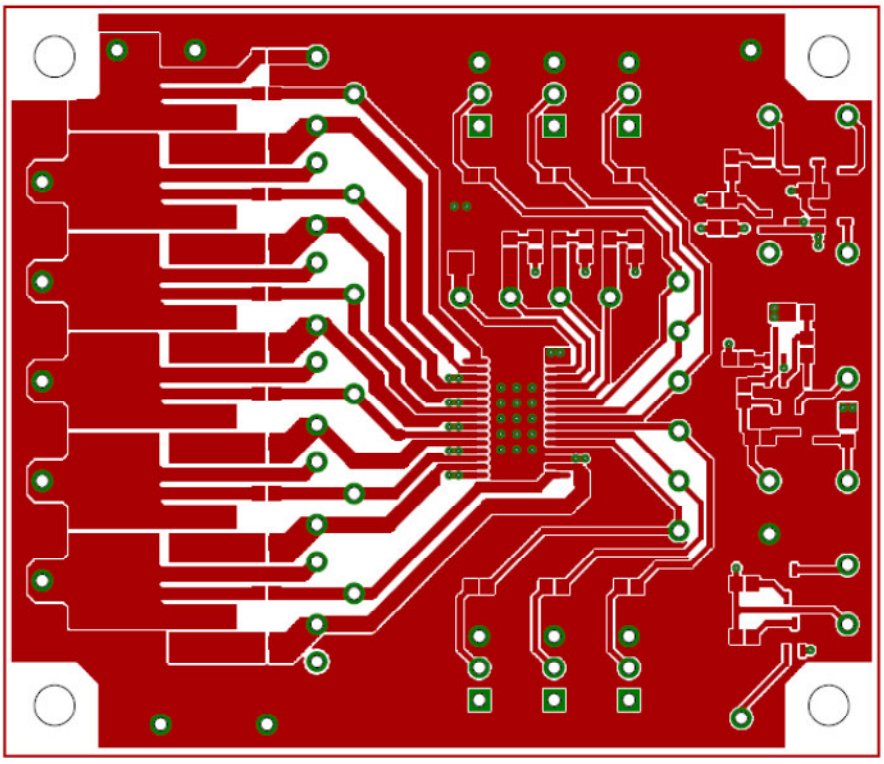


Figure 4. Top layer layout (Top view).

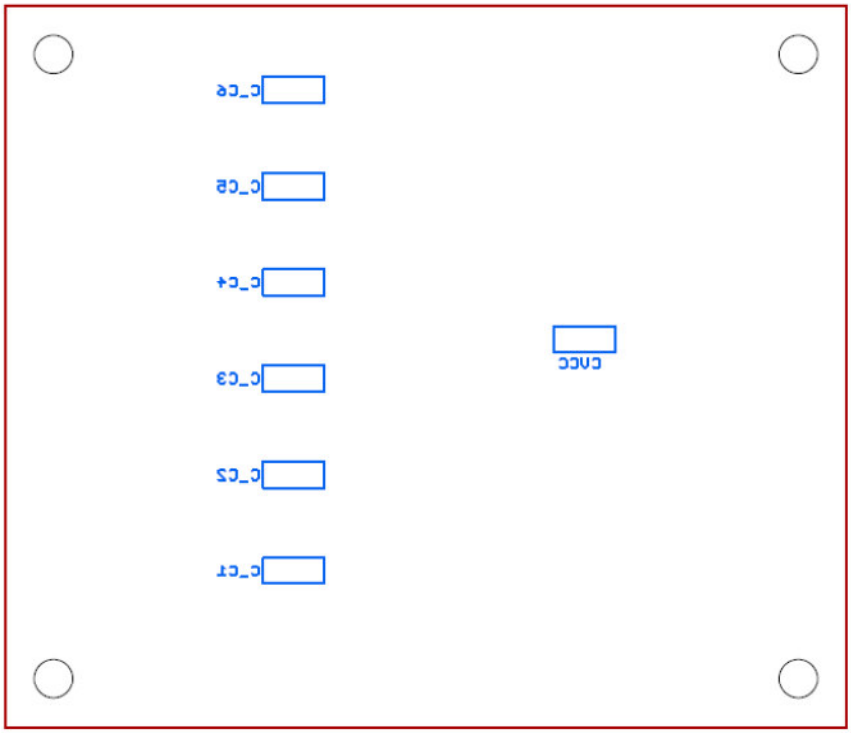


Figure 5. Bottom layer silkscreen (Top view).

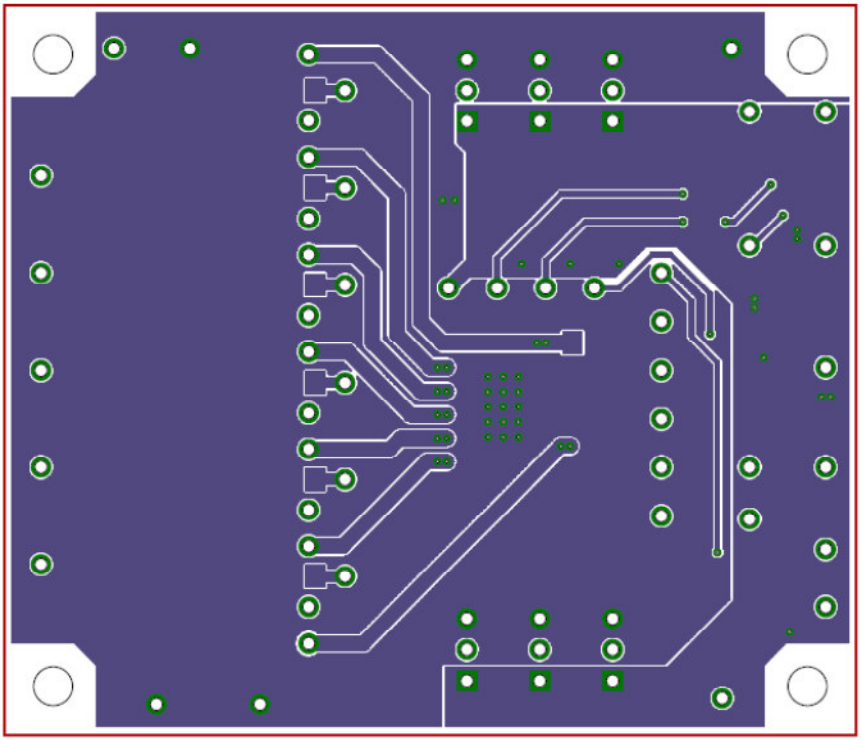


Figure 6. Bottom layer layout (Top view).

About stack of this LSI

When using the power storage element for connection of over 8 cells, series connection of this chip is possible.
Enable control (ENIN pin control) and various flag output (VO_OVLO1, VO_OVLO2, the VO_OK pin output) are also available in the series connection by using the following application circuit.

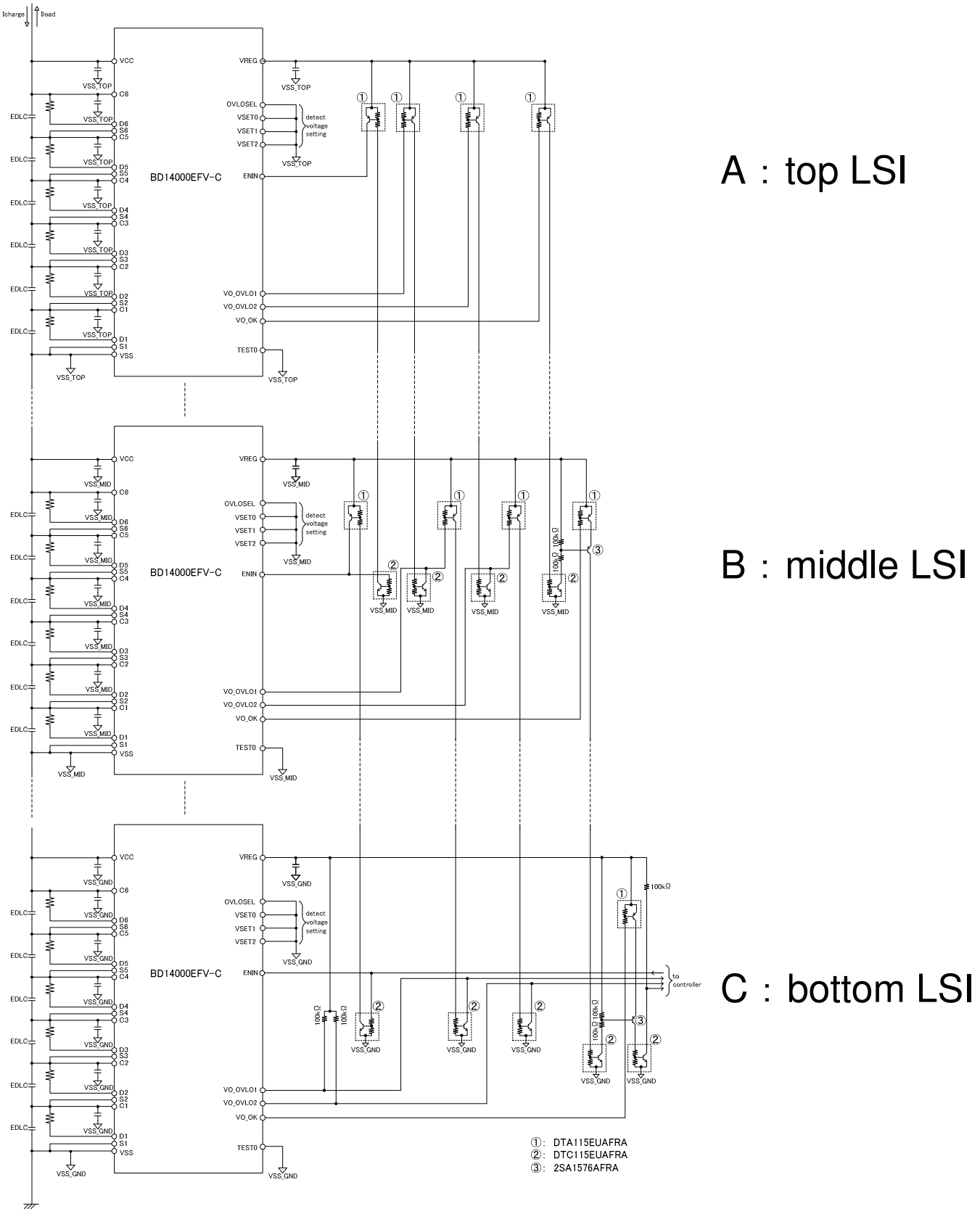


Figure 7. LSI stack application circuit example

Board connection diagrams in Top and Middle, Bottom layer are showed in the following.
Because the parts for the LSI stack are nonimplement, please implement parts depending on a use.

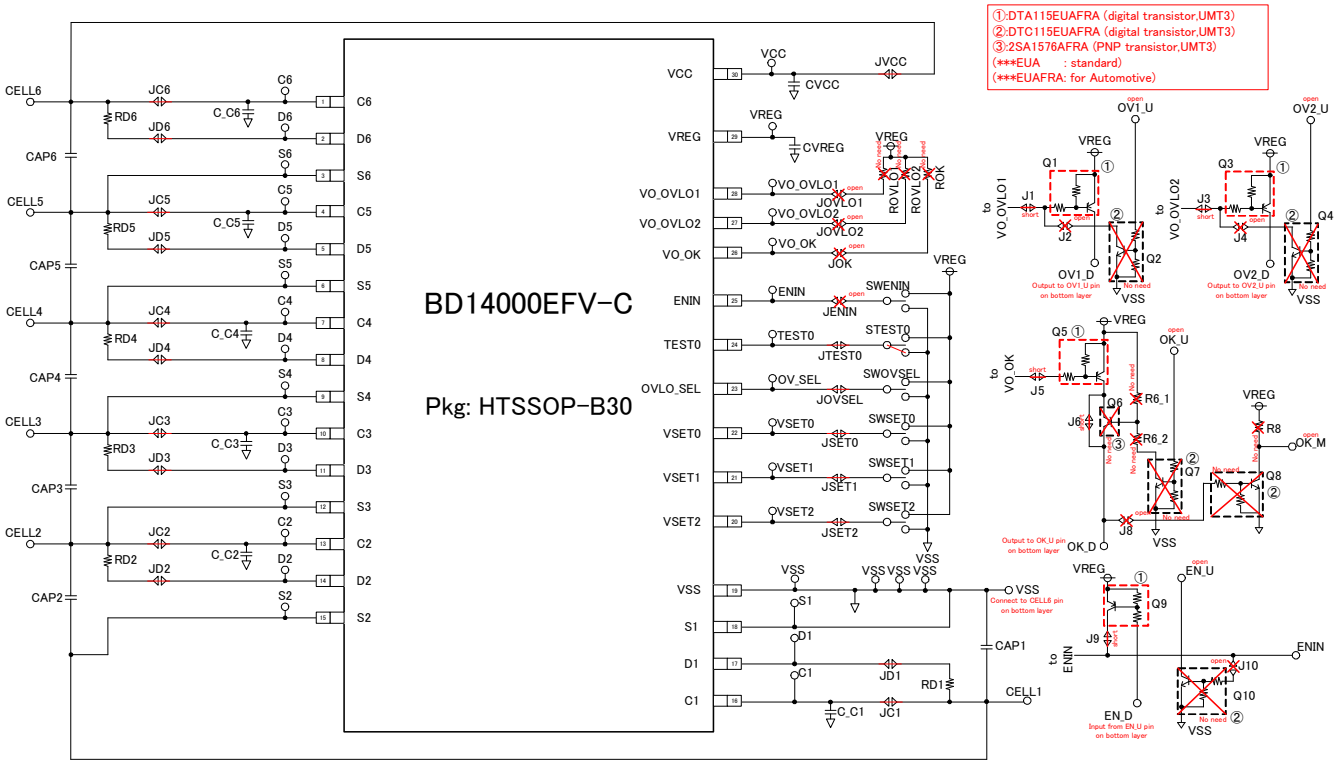


Figure 8. Top LSI board connection diagram

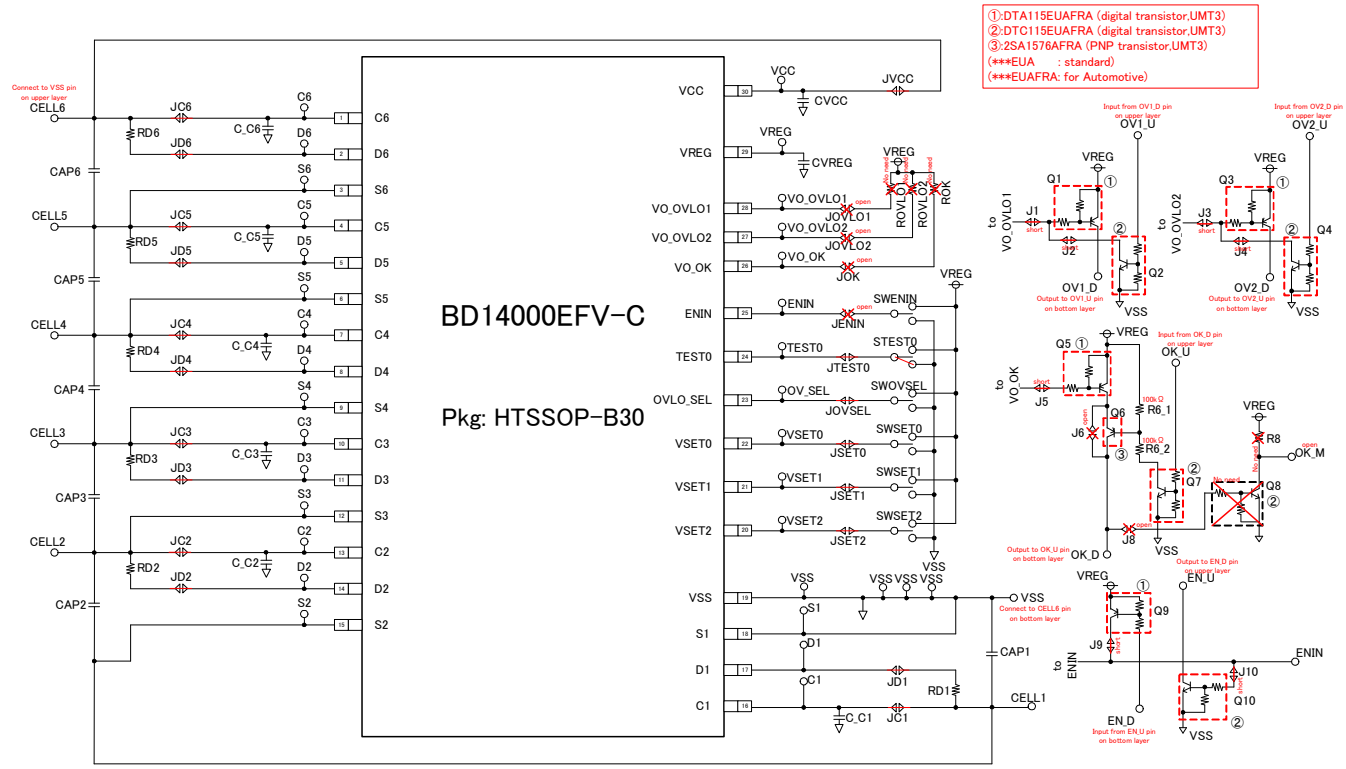


Figure 9. Middle LSI board connection diagram

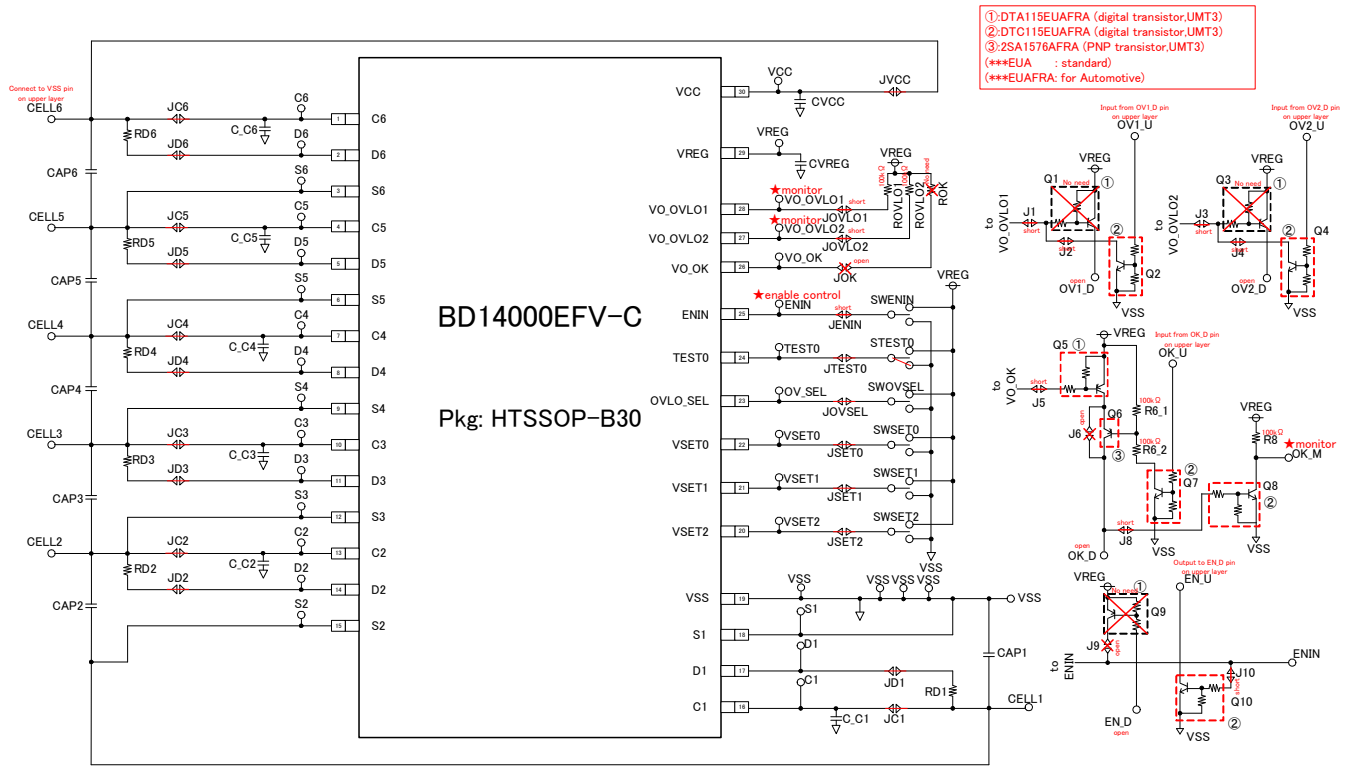
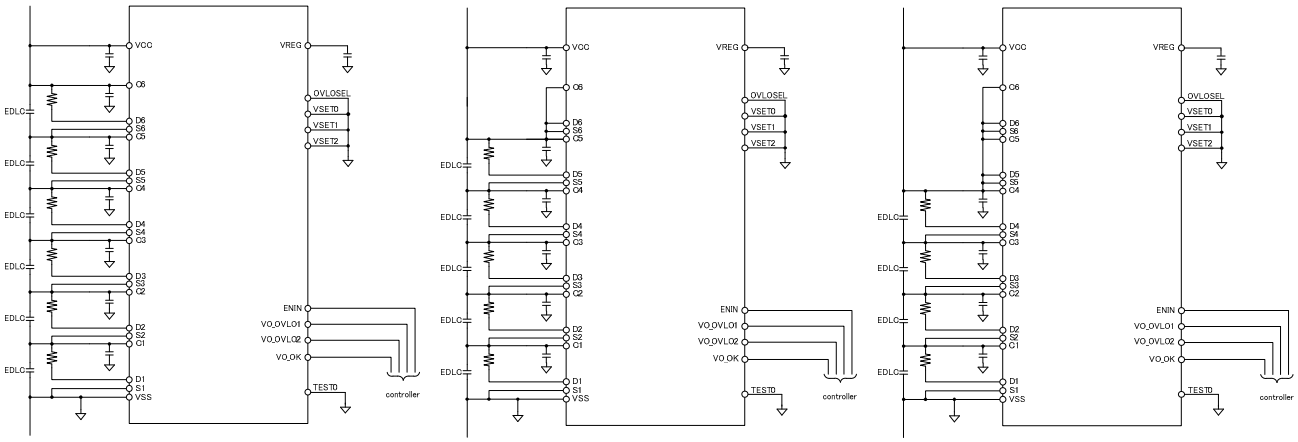


Figure 10. Bottom LSI board connection diagram

About a 4-6 cell application circuit

When using the power storage element with 4 cells and 5cells, please connect all the unused pins to the Cn pin where n is the number of actual cells in series. This chip can respond to 4 to 6 cells, but cannot respond to 3cells or fewer than 3 cells.



6 cell

5 cell
(shunt an unused pin on C5 pin)

4 cell
(shunt an unused pin on C4 pin)

Figure 11. 4-6 cell application circuit example