



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



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NDD60N900U1

N-Channel Power MOSFET 600 V, 900 mΩ

Features

- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	600	V
Gate-to-Source Voltage			V_{GS}	± 25	V
Continuous Drain Current $R_{\theta JC}$	Steady State	$T_C = 25^{\circ}\text{C}$	I_D	5.7	A
		$T_C = 100^{\circ}\text{C}$		3.6	
Power Dissipation – $R_{\theta JC}$	Steady State	$T_C = 25^{\circ}\text{C}$	P_D	74	W
Pulsed Drain Current	$t_p = 10\ \mu\text{s}$		I_{DM}	20	A
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to +150	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	5.7	A
Single Pulse Drain-to-Source Avalanche Energy ($I_D = 2\text{ A}$)			EAS	33	mJ
Peak Diode Recovery (Note 1)			dv/dt	15	V/ns
Lead Temperature for Soldering Leads			T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $I_{SD} < 5.7 \text{ A}$, $di/dt \leq 400 \text{ A}/\mu\text{s}$, $V_{peak} < V_{(BR)DSS}$

THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) NDD60N900U1	$R_{\theta JC}$	1.7	$^\circ\text{C}/\text{W}$
Junction-to-Ambient Steady State (Note 3) NDD60N900U1	$R_{\theta JA}$	47	$^\circ\text{C}/\text{W}$
(Note 2) NDD60N900U1-1		99	
(Note 2) NDD60N900U1-35		95	

2. Insertion mounted
3. Surface mounted on FR4 board using 1" sq. pad size (Cu area = 1.127 in sq [2 oz] including traces)

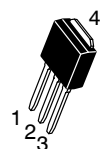
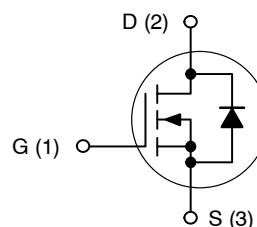


ON Semiconductor®

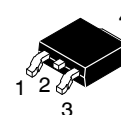
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$
600 V	900 mΩ @ 10 V

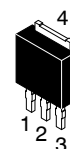
N-Channel MOSFET



IPAK
CASE 369D
STYLE 2



DPAK
CASE 369C
STYLE 2



IPAK
CASE 369AD
STYLE 2

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

NDD60N900U1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 mA	600			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			550		mV/°C
Drain-to-Source Leakage Current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V	T _J = 25°C		1	μA
			T _J = 125°C		100	
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250 μA	2	3.2	4	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J	Reference to 25°C, I _D = 250 μA		7.2		mV/°C
Static Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 2.5 A		820	900	mΩ
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = 2.5 A		4.3		S

DYNAMIC CHARACTERISTICS

Input Capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		360		pF
Output Capacitance	C _{oss}			23		
Reverse Transfer Capacitance	C _{rss}			1.1		
Effective output capacitance, energy related (Note 6)	C _{o(er)}	V _{GS} = 0 V, V _{DS} = 0 to 480 V		17		
Effective output capacitance, time related (Note 7)	C _{o(tr)}	I _D = constant, V _{GS} = 0 V, V _{DS} = 0 to 480 V		57		
Total Gate Charge	Q _g	V _{DS} = 300 V, I _D = 5.9 A, V _{GS} = 10 V		12		nC
Gate-to-Source Charge	Q _{gs}			2.5		
Gate-to-Drain ("Miller") Charge	Q _{gd}			5.8		
Plateau Voltage	V _{GP}			5.4		V
Gate Resistance	R _g			5		Ω

RESISTIVE SWITCHING CHARACTERISTICS (Note 5)

Turn-on Delay Time	t _{d(on)}	V _{DD} = 300 V, I _D = 5.9 A, V _{GS} = 10 V, R _G = 0 Ω		7		ns
Rise Time	t _r			9		
Turn-off Delay Time	t _{d(off)}			17		
Fall Time	t _f			6		

SOURCE-DRAIN DIODE CHARACTERISTICS

Diode Forward Voltage	V _{SD}	I _S = 5.7 A, V _{GS} = 0 V	T _J = 25°C		0.88	1.3	V
			T _J = 100°C		0.80		
Reverse Recovery Time	t _{rr}	V _{GS} = 0 V, V _{DD} = 30 V I _S = 5.9 A, d _i /d _t = 100 A/μs			270		ns
Charge Time	t _a				130		
Discharge Time	t _b				140		
Reverse Recovery Charge	Q _{rr}				1.8		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

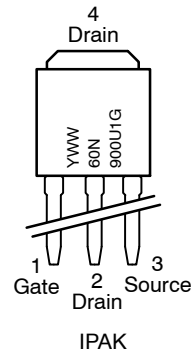
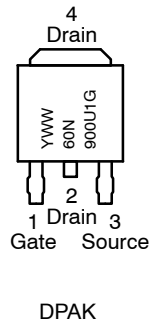
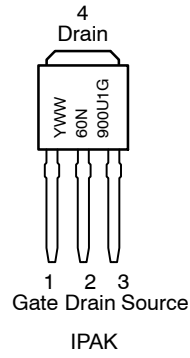
5. Switching characteristics are independent of operating junction temperatures.

6. C_{o(er)} is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}

7. C_{o(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}

NDD60N900U1

MARKING DIAGRAMS



Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping [†]
NDD60N900U1-1G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDD60N900U1-35G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDD60N900U1T4G	DPAK (Pb-Free, Halogen-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

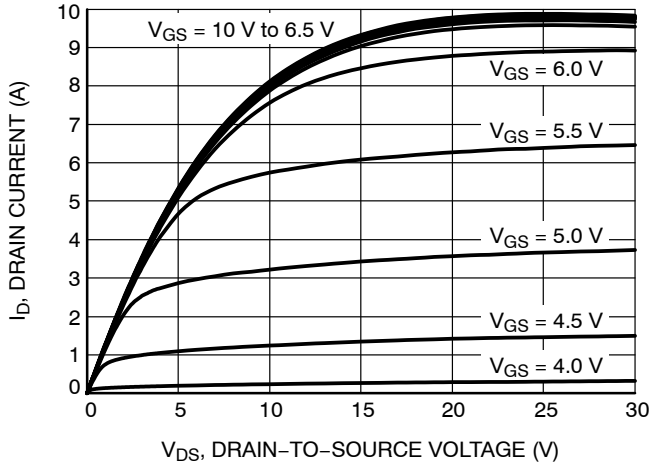


Figure 1. On-Region Characteristics

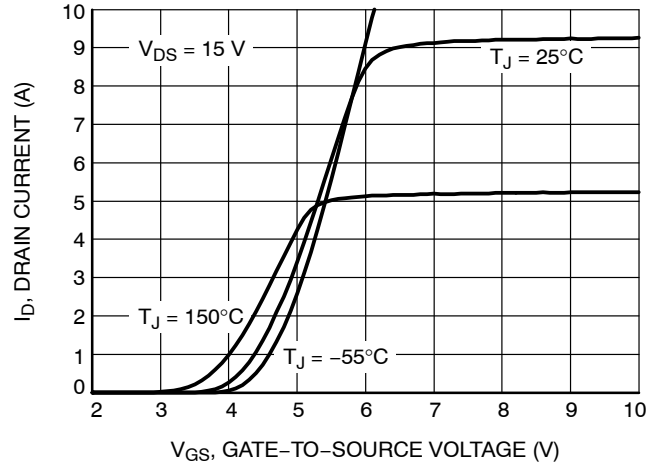


Figure 2. Transfer Characteristics

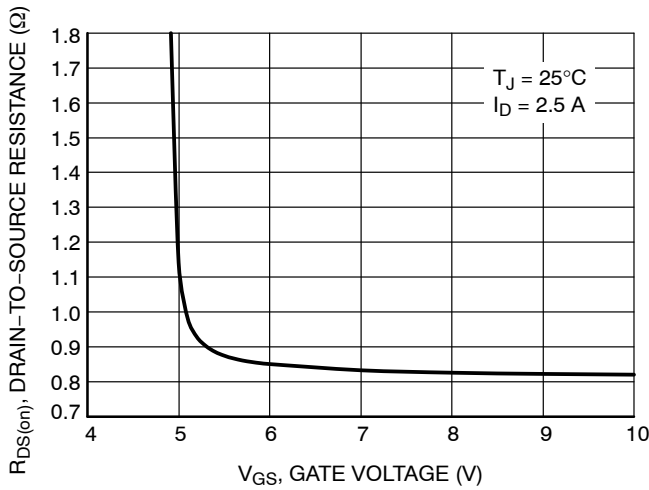


Figure 3. On-Resistance vs. Gate-to-Source Voltage

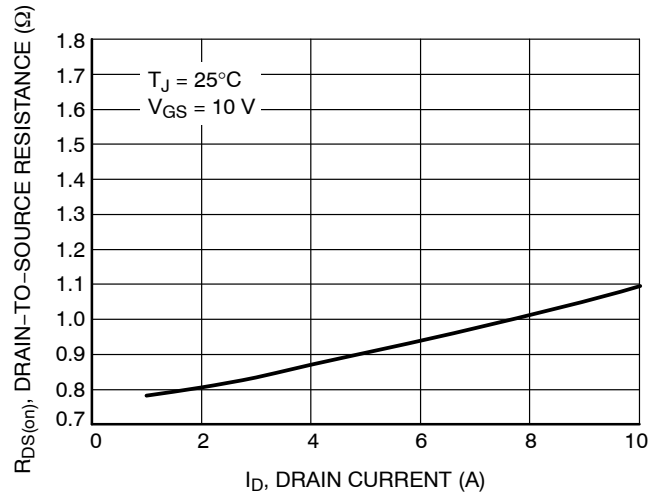


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

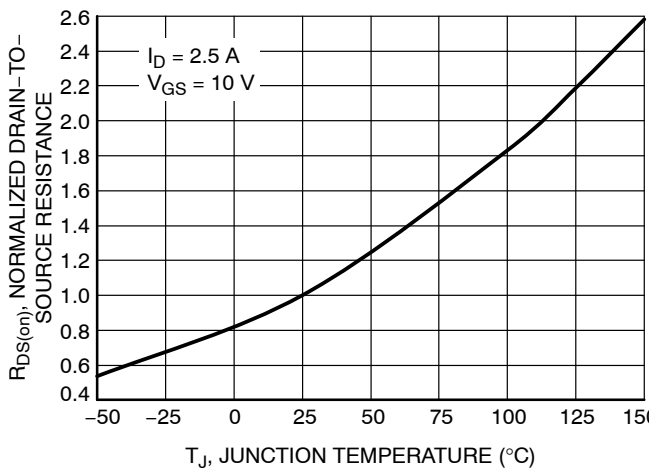


Figure 5. On-Resistance Variation with Temperature

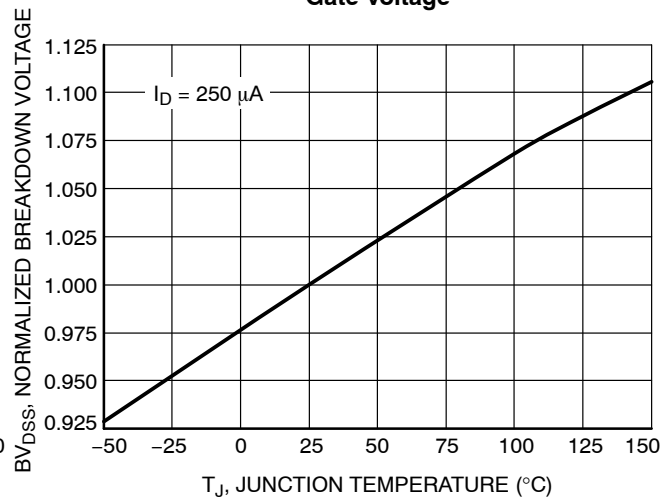


Figure 6. Breakdown Voltage Variation with Temperature

TYPICAL CHARACTERISTICS

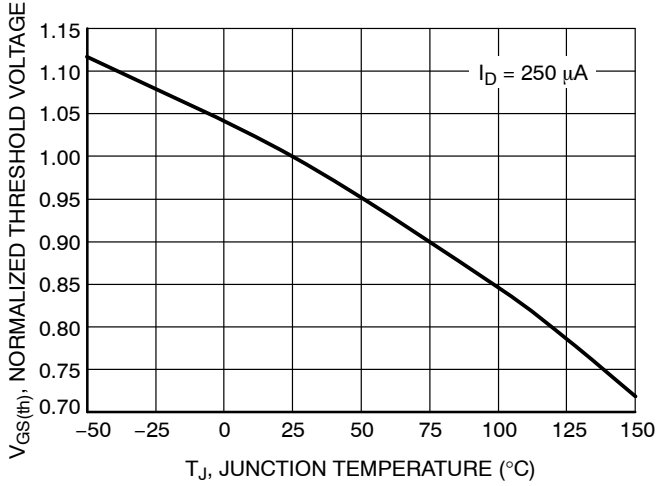


Figure 7. Threshold Voltage Variation with Temperature

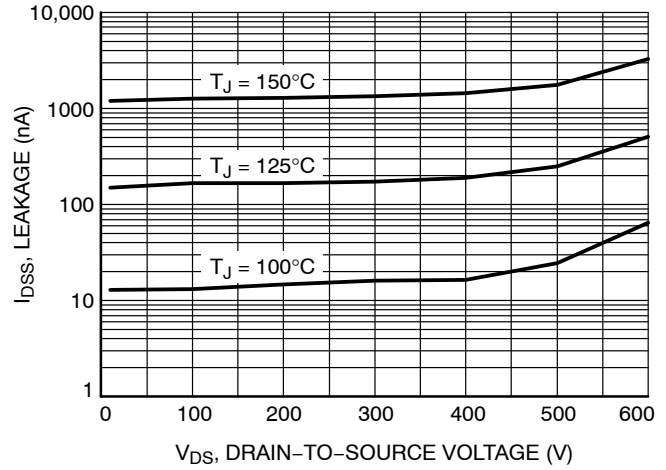


Figure 8. Drain-to-Source Leakage Current vs. Voltage

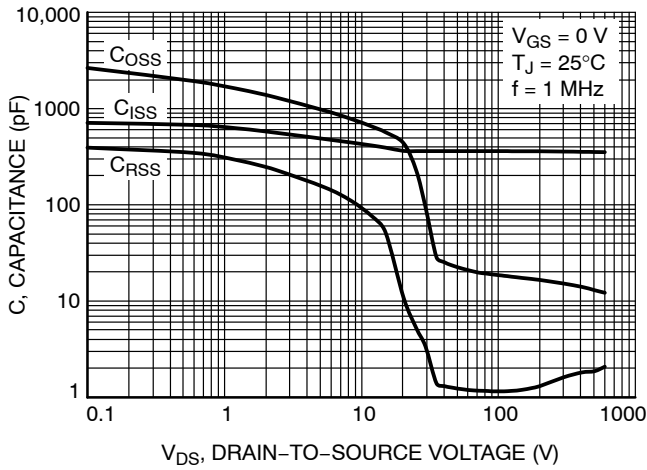


Figure 9. Capacitance Variation

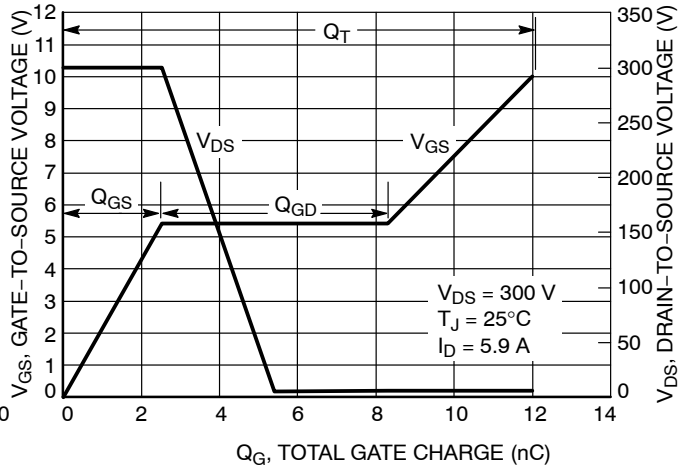


Figure 10. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

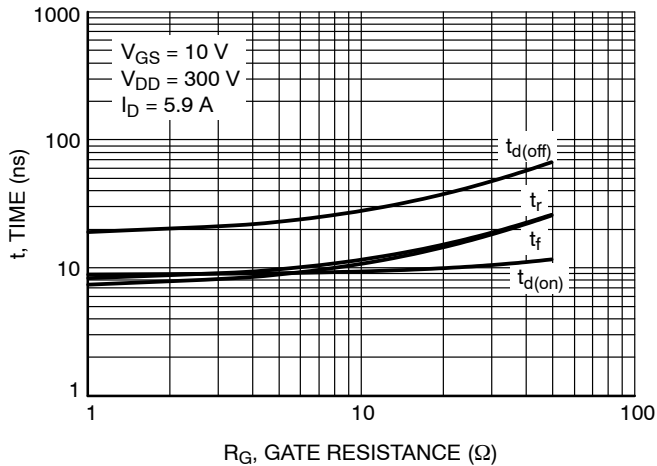


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

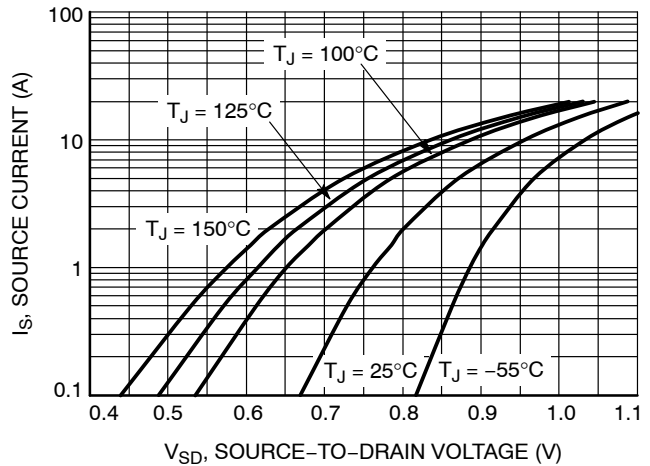


Figure 12. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS

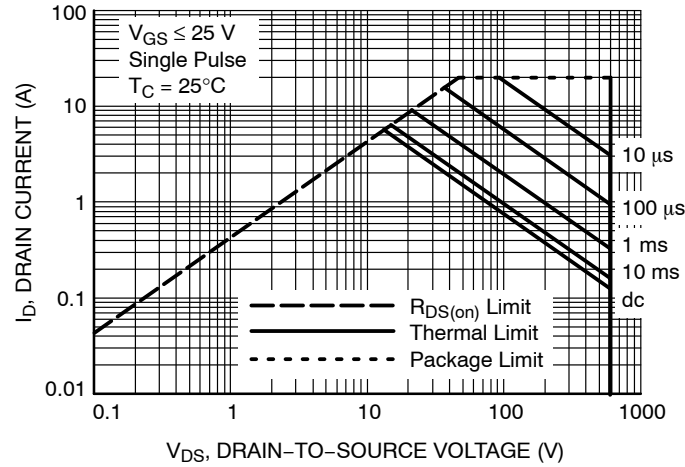


Figure 13. Maximum Rated Forward Biased Safe Operating Area

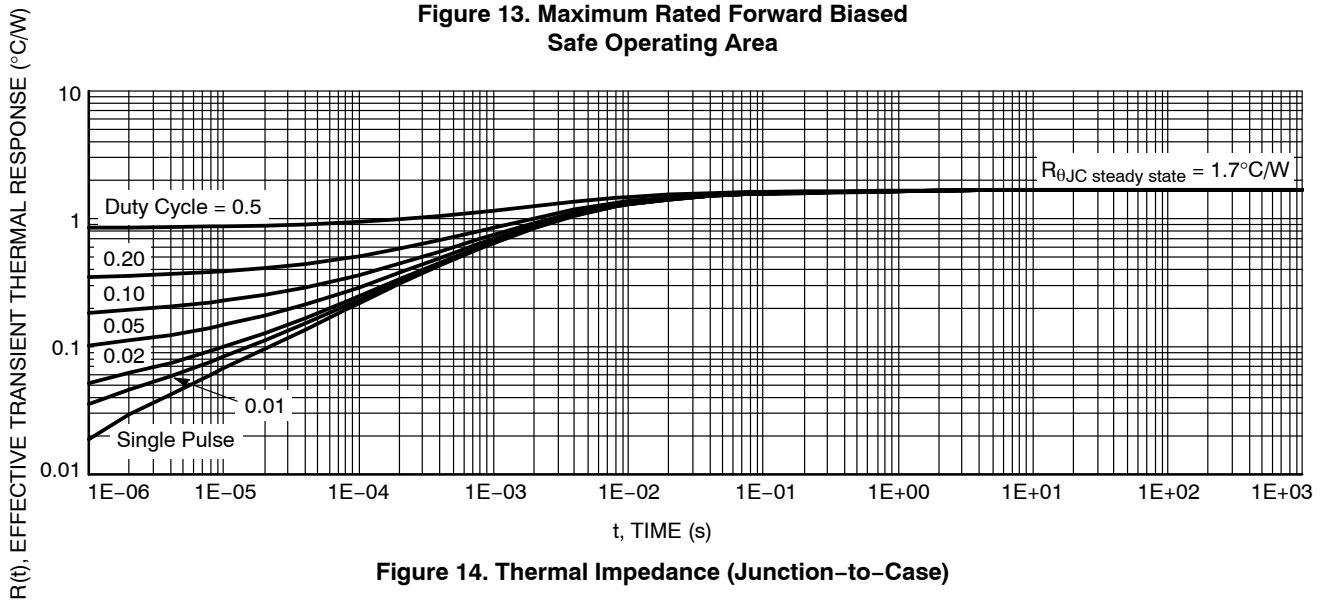
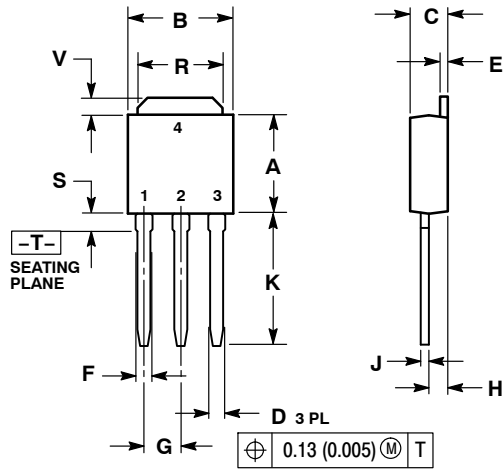


Figure 14. Thermal Impedance (Junction-to-Case)

NDD60N900U1

PACKAGE DIMENSIONS

IPAK CASE 369D-01 ISSUE C

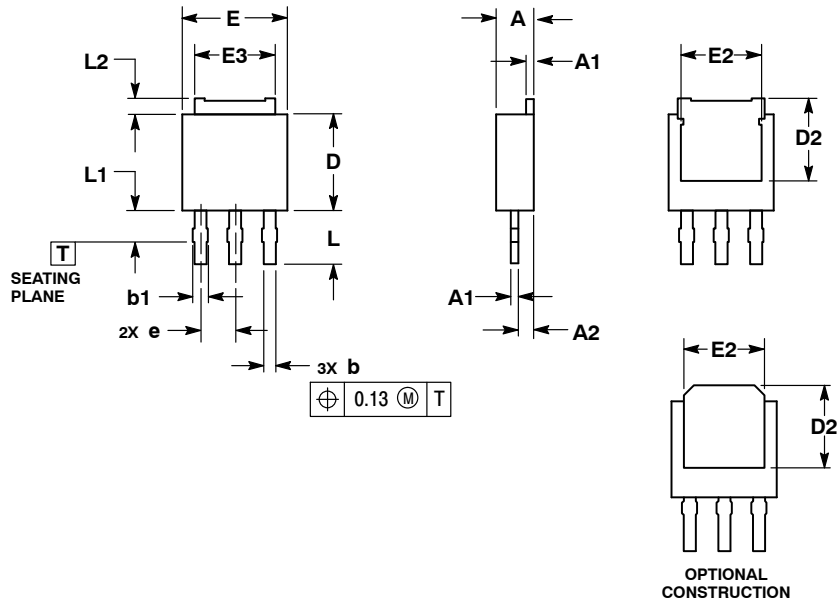


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
L	0.180	0.215	4.45	5.45
M	0.025	0.040	0.63	1.01
N	0.035	0.050	0.89	1.27
O	0.155	---	3.93	---

- STYLE 2:
- PIN 1. GATE
 - PIN 2. DRAIN
 - PIN 3. SOURCE
 - PIN 4. DRAIN

3.5 MM IPAK, STRAIGHT LEAD CASE 369AD ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD GATE OR MOLD FLASH.

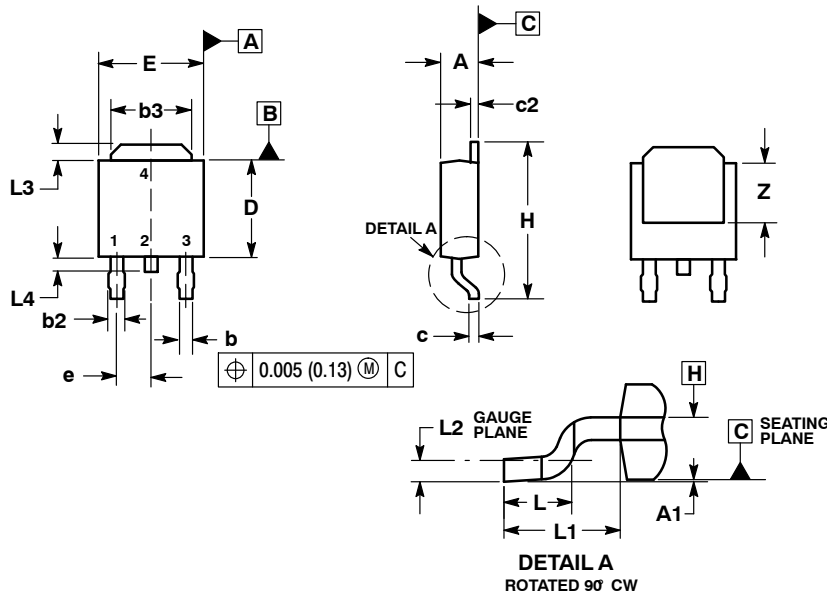
DIM	MILLIMETERS	
	MIN	MAX
A	2.19	2.38
A1	0.46	0.60
A2	0.87	1.10
b	0.69	0.89
b1	0.77	1.10
D	5.97	6.22
D2	4.80	---
E	6.35	6.73
E2	4.57	5.45
E3	4.45	5.46
e	2.28 BSC	
L	3.40	3.60
L1	---	2.10
L2	0.89	1.27

- STYLE 2:
- PIN 1. GATE
 - PIN 2. DRAIN
 - PIN 3. SOURCE
 - PIN 4. DRAIN

NDD60N900U1

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE) CASE 369C ISSUE D



NOTES:

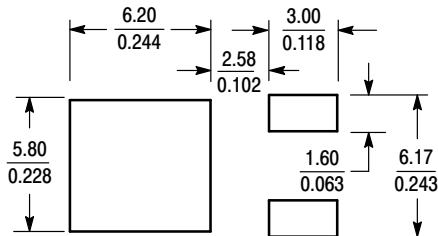
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108	REF	2.74	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 2:


1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



SCALE 3:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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