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Quad, Low Power, 12-Bit, 180 MSPS, Digital-to-Analog Converter and Waveform Generator

Data Sheet

AD9106

FEATURES

- Highly integrated quad DAC
- On-chip 4096 × 12-bit pattern memory
- On-chip DDS
- Power dissipation at 3.3 V, 4 mA output
  - 315 mW at 180 MSPS
- Sleep mode: < 5 mW at 3.3 V
- Supply voltage: 1.8 V to 3.3 V
- SFDR to Nyquist
  - 86 dBc at 1 MHz output
  - 85 dBc at 10 MHz output
- Phase noise at 1 kHz offset, 180 MSPS, 8 mA: −140 dBc/Hz
- Differential current outputs: 8 mA maximum at 3.3 V
- Small footprint 32-lead, 5 mm × 5 mm with 3.5 mm × 3.6 mm exposed paddle LFCSP
- Pb-free package

APPLICATIONS

- Medical instrumentation
  - Ultrasound transducer excitation
- Portable instrumentation
  - Signal generators, arbitrary waveform generators

GENERAL DESCRIPTION

The AD9106 TxDAC® and waveform generator is a high performance quad DAC integrating on-chip pattern memory for complex waveform generation with a direct digital synthesizer (DDS). The DDS is a 12-bit output, up to 180 MHz master clock sinewave generator with a 24-bit tuning word allowing 10.8 Hz/LSB frequency resolution. The DDS has a single frequency output for all four DACs and independent programmable phase shift outputs for each of the four DACs.

SRAM data can include directly generated stored waveforms, amplitude modulation patterns applied to DDS outputs, or DDS frequency tuning words.

An internal pattern control state machine allows the user to program the pattern period for all four DACs as well as the start delay within the pattern period for the signal output on each DAC channel.

An SPI interface is used to configure the digital waveform generator and load patterns into the SRAM.

There are gain adjustment factors and offset adjustments applied to the digital signals on their way into the four DACs.

The AD9106 offers exceptional ac and dc performance and supports DAC sampling rates up to 180 MSPS. The flexible power supply operating range of 1.8 V to 3.3 V and low power dissipation of the AD9106 make it well suited for portable and low power applications.

Rev. A
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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Last Content Update: 02/23/2017

COMPARABLE PARTS

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EVALUATION KITS

- AD9106 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9106: Quad, Low Power, 12-Bit, 180 MSPS, Digital-to-Analog Converter and Waveform Generator Data Sheet

TOOLS AND SIMULATIONS

- AD9106 IBIS Model

REFERENCE MATERIALS

Informational

- Advantiv™ Advanced TV Solutions

Press

- Quad 12-Bit and Single 14-Bit, 180-MSPS D/A Converters Integrate Complex Waveform Generation Function

DESIGN RESOURCES

- AD9106 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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11/12—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

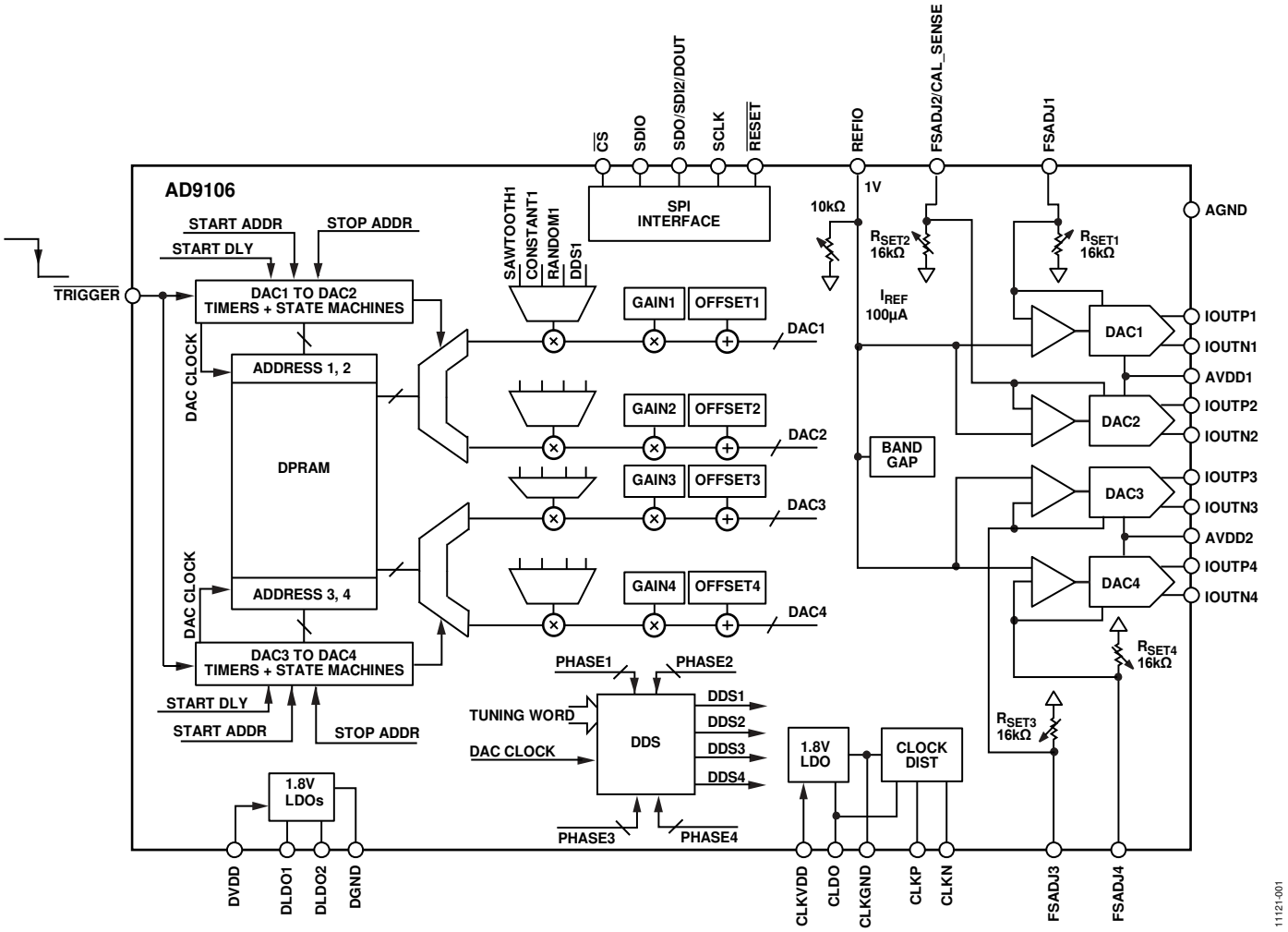

Figure 1.

SPECIFICATIONS

DC SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V; internal CLDO, DLDO1, and DLDO2; I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION		12		Bits
ACCURACY at 3.3 V				
Differential Nonlinearity (DNL)		±0.4		LSB
Integral Nonlinearity (INL)		±0.5		LSB
DAC OUTPUTS				
Offset Error		±.00025		% of FSR
Gain Error Internal Reference—No Automatic I_{OUTFS} Calibration	−1.0		+1.0	% of FSR
Full-Scale Output Current[1] at 3.3 V	2	4	8	mA
Output Resistance		200		MΩ
Output Compliance Voltage	−0.5		+1.0	V
Crosstalk, DAC to DAC (f_{OUT} = 10 MHz)		96		dBC
Crosstalk, DAC to DAC (f_{OUT} = 60 MHz)		82		dBc
DAC TEMPERATURE DRIFT				
Gain with Internal Reference		±251		ppm/°C
Internal Reference Voltage		±119		ppm/°C
REFERENCE OUTPUT				
Internal Reference Voltage with AVDD = 3.3 V	0.8	1.0	1.2	V
Output Resistance		10		kΩ
REFERENCE INPUT				
Voltage Compliance	0.1		1.25	V
Input Resistance External, Reference Mode		1		MΩ
DAC MATCHING				
Gain Matching—No Automatic I_{OUTFS} Calibration		±0.75		% of FSR

[1] Based on use of 8 kΩ external xR_{SET} resistors.

DC SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}, AVDD = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V, I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
RESOLUTION		12		Bits
ACCURACY at 1.8 V				
Differential Nonlinearity (DNL)		±0.4		LSB
Integral Nonlinearity (INL)		±0.4		LSB
DAC OUTPUTS				
Offset Error		±.00025		% of FSR
Gain Error Internal Reference—No Automatic I_{OUTFS} Calibration	−1.0		+1.0	% of FSR
Full-Scale Output Current[1] at 1.8 V	2	4	4	mA
Output Resistance		200		MΩ
Output Compliance Voltage	−0.5		+1.0	V
Crosstalk, DAC to DAC (f_{OUT} = 30 MHz)		94		dB
Crosstalk, DAC to DAC (f_{OUT} = 60 MHz)		78		dB
DAC TEMPERATURE DRIFT				
Gain		±228		ppm/°C
Reference Voltage		±131		ppm/°C
REFERENCE OUTPUT				
Internal Reference Voltage with AVDD = 1.8 V	0.8	1.0	1.2	V
Output Resistance		10		kΩ
REFERENCE INPUT				
Voltage Compliance	0.1		1.25	V
Input Resistance External, Reference Mode		1		MΩ
DAC MATCHING				
Gain Matching—No Automatic I_{OUTFS} Calibration		±0.75		% of FSR

[1] Based on use of 8 kΩ external xR_{SET} resistors.

DIGITAL TIMING SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V; internal CLDO, DLDO1, and DLDO2; I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUT (CLKIN)				
Maximum Clock Rate	180			MSPS
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (SCLK)	80			MHz
Minimum Pulse Width High		6.25		ns
Minimum Pulse Width Low		6.25		ns
Setup Time SDIO to SCLK	4.0			ns
Hold Time SDIO to SCLK	5.0			ns
Output Data Valid SCLK to SDO or SDIO		6.2		ns
Setup Time $\overline{CS}$ to SCLK	4.0			ns

DIGITAL TIMING SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}, AVDD = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V, I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUT (CLKIN)				
Maximum Clock Rate	180			MSPS
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (SCLK)	80			MHz
Minimum Pulse Width High		6.25		ns
Minimum Pulse Width Low		6.25		ns
Setup Time SDIO to SCLK	4.0			ns
Hold Time SDIO to SCLK	5.0			ns
Output Data Valid SCLK to SDO or SDIO		8.8		ns
Setup Time $\overline{CS}$ to SCLK	4.0			ns

INPUT/OUTPUT SIGNAL SPECIFICATIONS

Table 5.

Parameter	Test Conditions/ Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL (SCLK, $\overline{CS}$, SDIO, SDO/SDI2/DOUT, $\overline{RESET}$, $\overline{TRIGGER}$)					
Input V_{IN} Logic High	DVDD = 1.8 V	1.53			V
	DVDD = 3.3 V	2.475			V
Input V_{IN} Logic Low	DVDD = 1.8 V			0.27	V
	DVDD = 3.3 V			0.825	V
CMOS OUTPUT LOGIC LEVEL (SDIO, SDO/SDI2/DOUT)					
Output V_{OUT} Logic High	DVDD = 1.8 V	1.79			V
	DVDD = 3.3 V	3.28			V
Output V_{OUT} Logic Low	DVDD = 1.8 V			0.25	V
	DVDD = 3.3 V			0.625	V
DAC CLOCK INPUT (CLKP, CLKN)					
Minimum Peak-to-Peak Differential Input Voltage, V_{CLKP}/V_{CLKN}			150		mV
Maximum Voltage at V_{CLKP} or V_{CLKN}			V_{DVDD}		V
Minimum Voltage at V_{CLKP} or V_{CLKN}			V_{DGND}		V
Common-Mode Voltage Generated on Chip			0.9		V

AC SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V; internal CLDO, DLDO1, and DLDO2; I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 6.

Parameter	Min	Typ	Max	Unit
SPURIOUS FREE DYNAMIC RANGE (SFDR)				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		86		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		73		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		92		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		77		dBc
NSD				
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		−167		dBm/Hz
PHASE NOISE at 1 kHz FROM CARRIER				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		−135		dBc/Hz
DYNAMIC PERFORMANCE				
Output Settling Time, Full Scale Output Step (to 0.1%)[1]		31.2		ns
Trigger to Output Delay, f_{DAC} = 180 MSPS[2]		96		ns
Rise Time, Full-Scale Swing[1]		3.25		ns
Fall Time, Full-Scale Swing[1]		3.26		ns

[1] Based on the 85 Ω resistors from DAC output terminals to ground.
[2] Start delay = 0 f_{DAC} clock cycles.

AC SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}, AVDD = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V, I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 7.

Parameter	Min	Typ	Max	Unit
SPURIOUS FREE DYNAMIC RANGE (SFDR)				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		83		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		74		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		91		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		83		dBc
NSD				
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		−163		dBm/Hz
PHASE NOISE at 1 kHz FROM CARRIER				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		−135		dBc/Hz
DYNAMIC PERFORMANCE				
Output Settling Time (to 0.1%)[1]		31.2		ns
Trigger to Output Delay, f_{DAC} = 180 MSPS[2]		96		ns
Rise Time[1]		3.25		ns
Fall Time[1]		3.26		ns

[1] Based on the 85 Ω resistors from DAC output terminals to ground.
[2] Start delay = 0 f_{DAC} clock cycles.

POWER SUPPLY VOLTAGE INPUTS AND POWER DISSIPATION

Table 8.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG SUPPLY VOLTAGES					
AVDD1, AVDD2		1.7		3.6	V
CLKVDD		1.7		3.6	V
CLDO	On-chip LDO not in use	1.7		1.9	V
DIGITAL SUPPLY VOLTAGES					
DVDD		1.7		3.6	V
DLDO1, DLDO2	On-chip LDO not in use	1.7		1.9	V
POWER CONSUMPTION	AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, internal CLDO, DLDO1, and DLDO2				
f_{DAC} = 180 MSPS, Pure CW Sine Wave	12.5 MHz (DDS only), all four DACs		315.25		mW
I_{AVDD}			28.51		mA
I_{DVDD}					
DDS Only	CW sine wave output		60.3		mA
RAM Only	50% duty cycle FS pulse output		27.1		mA
DDS and RAM Only	50% duty cycle sine wave output		39.75		mA
I_{CLKVDD}			6.72		mA
Power-Down Mode	REF_PDN = 0, DACs sleep, CLK power down, external CLK, and supplies on		4.73		mW
POWER CONSUMPTION	AVDD = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V				
f_{DAC} = 180 MSPS, Pure CW Sine Wave	12.5 MHz (DDS only)		167		mW
I_{AVDD}			28.14		mA
I_{DVDD}			0.151		mA
I_{DLDO2}					
DDS Only	CW sine wave output		53.75		mA
RAM Only	50% duty cycle FS pulse output		17.78		mA
DDS and RAM Only—50% Duty Cycle Sine Wave Output			35.4		mA
I_{DLDO1}			4.0		mA
I_{CLKVDD}			0.0096		mA
I_{CLDO}			6.6		mA
Power-Down Mode	REF_PDN = 0, DACs sleep, CLK power down, external CLK, and supplies on		1.49		mW

ABSOLUTE MAXIMUM RATINGS

Table 9.

Parameter	Rating
AVDD1, AVDD2, DVDD to AGND, DGND, CLKGND	−0.3 V to +3.9 V
CLKVDD to AGND, DGND, CLKGND	−0.3 V to +3.9 V
CLDO, DLDO1, DLDO2 to AGND, DGND, CLKGND	−0.3 V to +2.2 V
AGND to DGND, CLKGND	−0.3 V to +0.3V
DGND to AGND, CLKGND	−0.3 V to +0.3 V
CLKGND to AGND, DGND	−0.3 V to +0.3 V
$\overline{CS}$, SDIO, SCLK, SDO/SDI2/DOUT, $\overline{RESET}$, $\overline{TRIGGER}$ to DGND	−0.3 V to DVDD + 0.3 V
CLKP, CLKN to CLKGND	−0.3 V to CLKVDD + 0.3 V
REFIO to AGND	−1.0 V to AVDD + 0.3 V
IOUTP1, IOUTN1, IOUTP2, IOUTN2, IOUTP3, IOUTN3, IOUTP4, IOUTN4 to AGND	−0.3 V to DVDD + 0.3 V
FSADJ1, FSADJ2/CAL_SENSE, F4DJ3, FSADJ4 to AGND	−0.3 V to AVDD + 0.3 V
Junction Temperature	125 °C
Storage Temperature	−65 °C to +150 °C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a standard circuit board for surface-mount packages. θ_{JC} is measured from the solder side (bottom) of the package.

Table 10. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
32-Lead LFCSP with Exposed Paddle	30.18	6.59	3.84	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

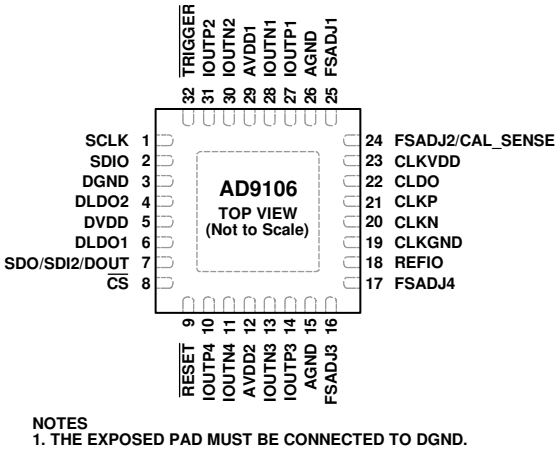

Figure 2. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCLK	SPI Clock Input.
2	SDIO	SPI Data Input/Output. Primary bidirectional data line for the SPI port.
3	DGND	Digital Ground.
4	DLDO2	1.8 V Internal Digital LDO1 Output. When the internal digital LDO1 is enabled, this pin should be bypassed with a 0.1 µF capacitor.
5	DVDD	3.3 V External Digital Power Supply. DVDD defines the level of the digital interface of the AD9106 (SPI interface).
6	DLDO1	1.8 V Internal Digital LDO2 Outputs. When the internal digital LDO2 is enabled, this pin should be bypassed with a 0.1 µFcapacitor.
7	SDO/SDI2/DOUT	Digital I/O Pin. In 4-wire SPI mode, this pin outputs the data from the SPI. In double SPI mode, this pin is a second data input line, SDI2, for the SPI port used to write to the SRAM. In data output mode, this terminal is a programmable pulse output.
8	$\overline{CS}$	SPI Port Chip Select, Active Low.
9	$\overline{RESET}$	Active Low Reset Pin. Resets registers to their default values.
10	IOUTP4	DAC4 Current Output, Positive Side.
11	IOUTN4	DAC4 Current Output, Negative Side.
12	AVDD2	1.8 V to 3.3 V Power Supply Input for DAC3 and DAC4.
13	IOUTN3	DAC3 Current Output, Negative Side.
14	IOUTP3	DAC3 Current Output, Positive Side.
15	AGND	Analog Ground.
16	FSADJ3	External Full-Scale Current Output Adjust for DAC3.
17	FSADJ4	External Full-Scale Current Output Adjust for DAC4.
18	REFIO	DAC Voltage Reference Input/Output.
19	CLKGND	Clock Ground.
20	CLKN	Clock Input, Negative Side.
21	CLKP	Clock Input, Positive Side.
22	CLDO	Clock Power Supply Output (Internal Regulator in Use), Clock Power Supply Input (Internal Regulator Bypassed).
23	CLKVDD	Clock Power Supply Input.
24	FSADJ2/CAL_SENSE	External Full-Scale Current Output Adjust for DAC2 or Sense Input for Automatic I_{OUTFS} Calibration.
25	FSADJ1	External Full-Scale Current Output Adjust for DAC1 or Full-Scale Current Output Adjust Reference for Automatic I_{OUTFS} Calibration.
26	AGND	Analog Ground.
27	IOUTP1	DAC1 Current Output, Positive Side.

Pin No.	Mnemonic	Description
28	IOUTN1	DAC1 Current Output, Negative Side.
29	AVDD1	1.8 V to 3.3 V Power Supply Input for DAC1 and DAC2.
30	IOUTN2	DAC2 Current Output, Negative Side.
31	IOUTP2	DAC2 Current Output, Positive Side.
32	$\overline{\text{TRIGGER}}$	Pattern Trigger Input.
	EPAD	Exposed Pad. The exposed pad must be connected to DGND.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, internal CLDO, DLDO1, and DLDO2.

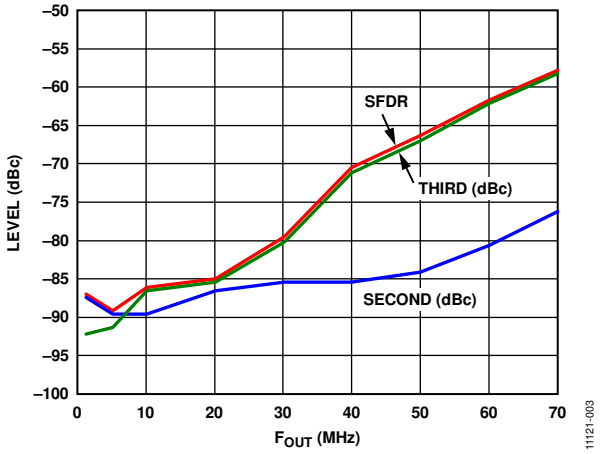

Figure 3. SFDR, 2nd and 3rd Harmonics at I_{OUTFS} = 8 mA vs. F_{OUT}

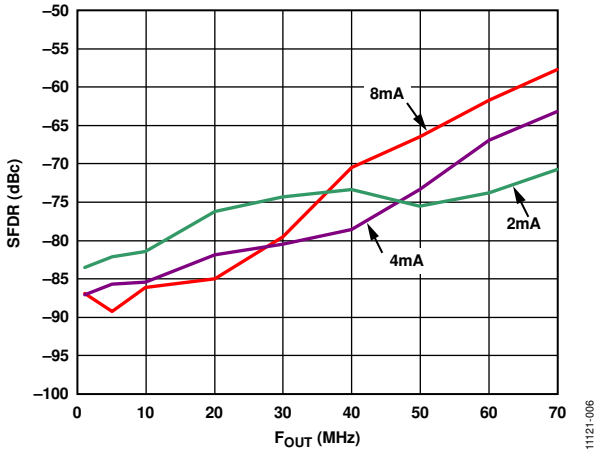

Figure 6. SFDR at Three I_{OUTFS} vs. F_{OUT}

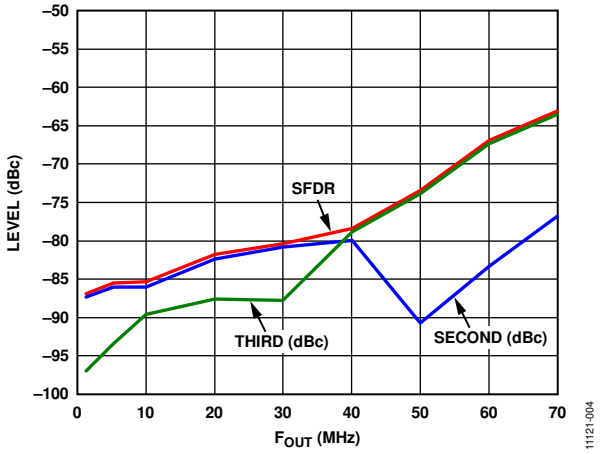

Figure 4. SFDR, 2nd and 3rd Harmonics at I_{OUTFS} = 4 mA vs. F_{OUT}

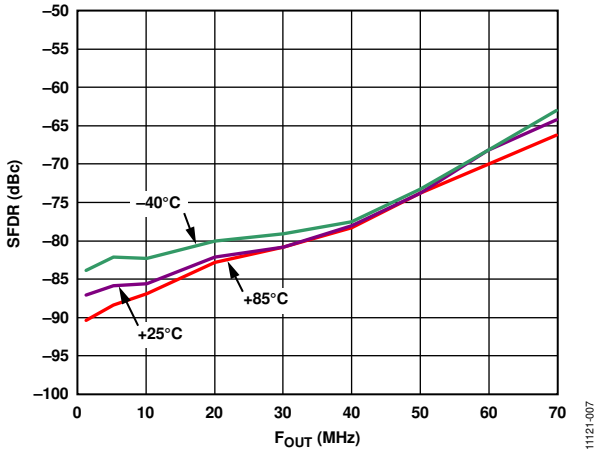

Figure 7. SFDR at Three Temperatures vs. F_{OUT}

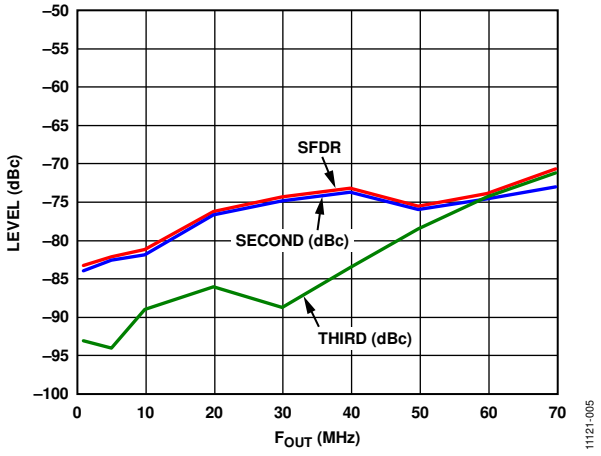

Figure 5. SFDR, 2nd and 3rd Harmonics at I_{OUTFS} = 2 mA vs. F_{OUT}

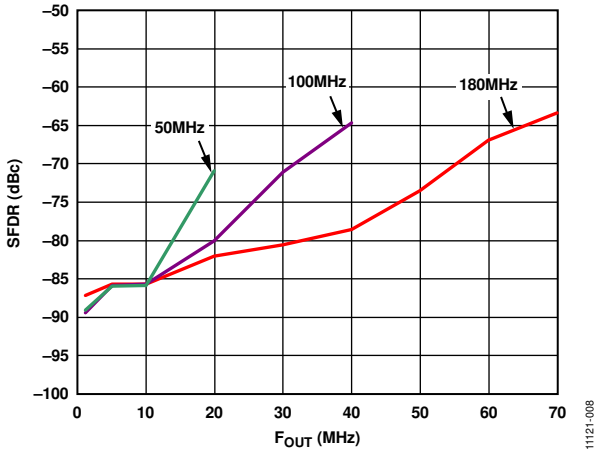

Figure 8. SFDR at Three F_{DAC} vs. F_{OUT}

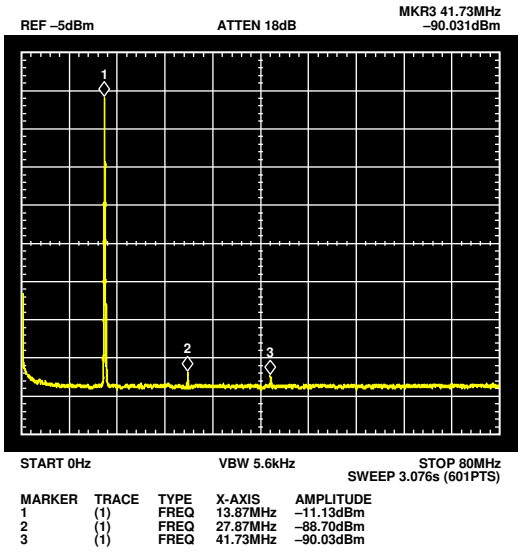

Figure 9. Output Spectrum F_{OUT} = 13.87 MHz

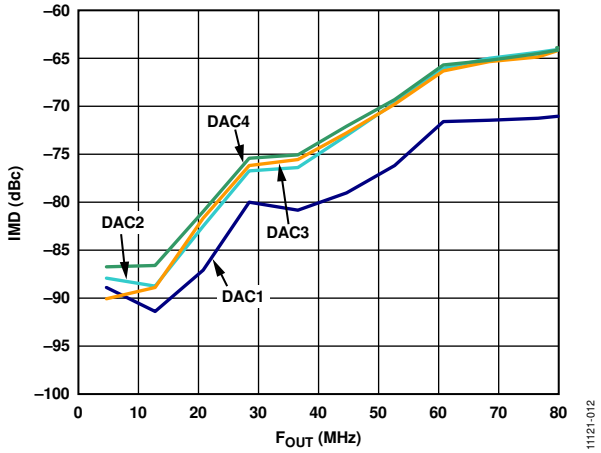

Figure 12. IMD vs. F_{OUT}, All Four DACs

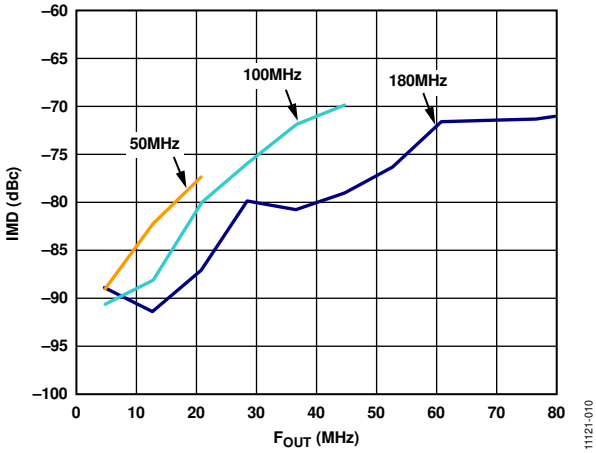

Figure 10. IMD vs. F_{OUT}, Three F_{DAC} Values

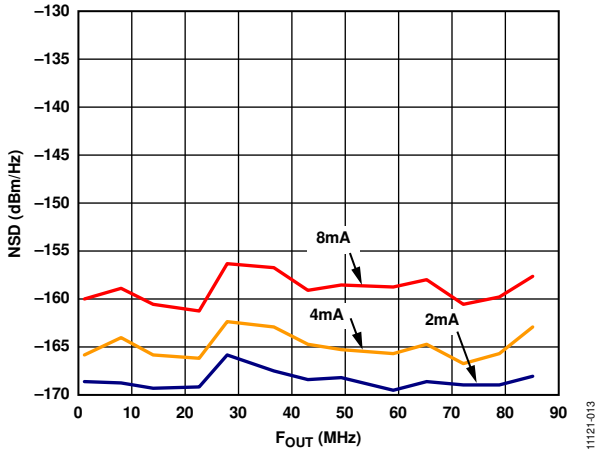

Figure 13. NSD vs. F_{OUT}, Three I_{OUTFS} Values

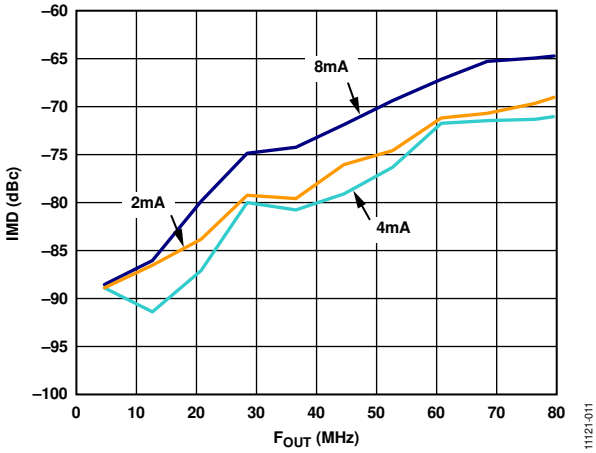

Figure 11. IMD vs. F_{OUT}, Three I_{OUTFS} Values

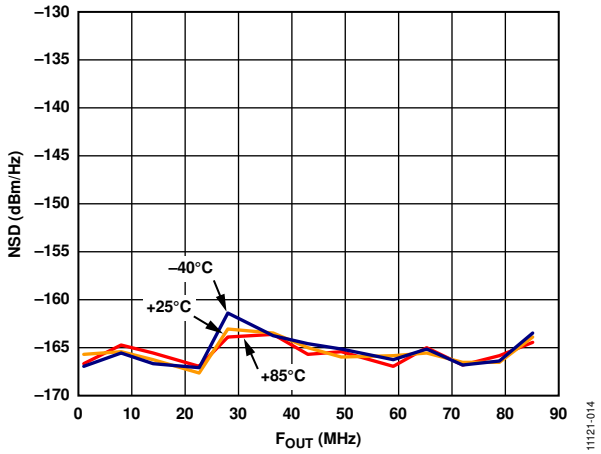

Figure 14. NSD vs. F_{OUT} at Three Temperatures

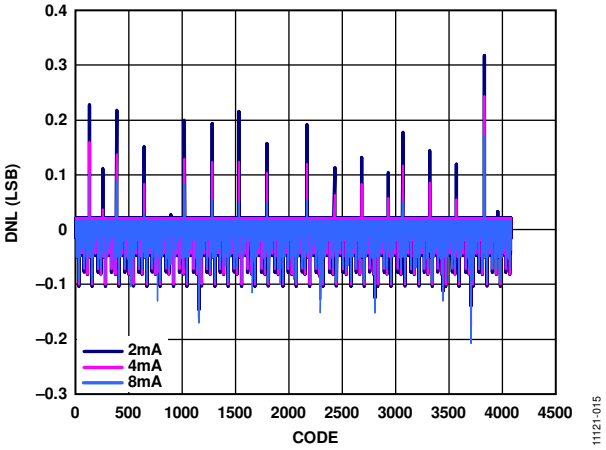

Figure 15. DNL, Three I_{OUTFS} Values

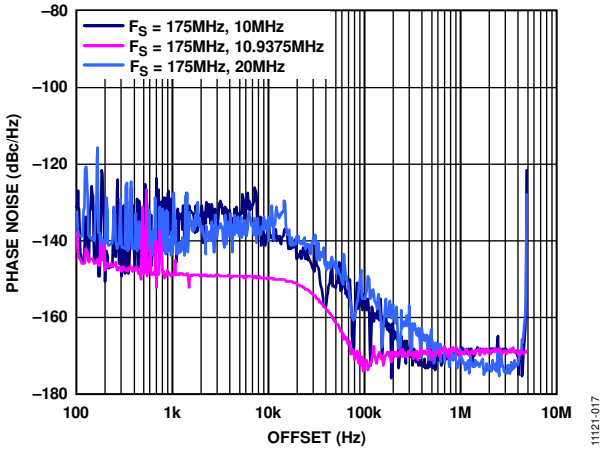

Figure 17. Phase Noise

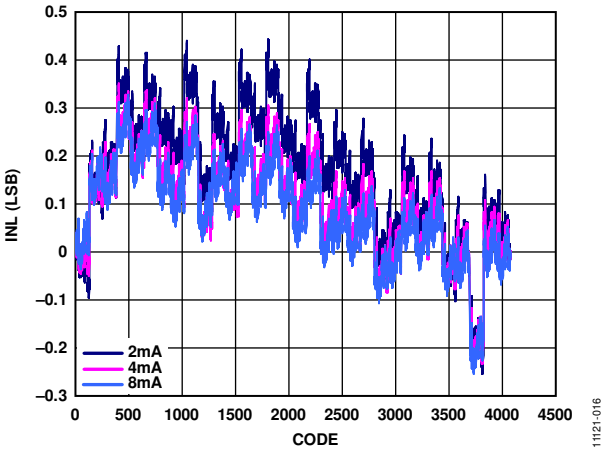

Figure 16. INL, Three I_{OUTFS} Values

AVDD = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V.

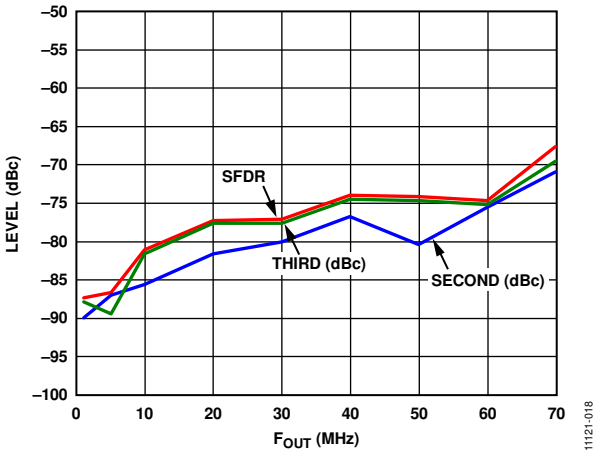

Figure 18. SFDR, 2nd and 3rd Harmonics at I_{OUTFS} = 4 mA vs. F_{OUT}

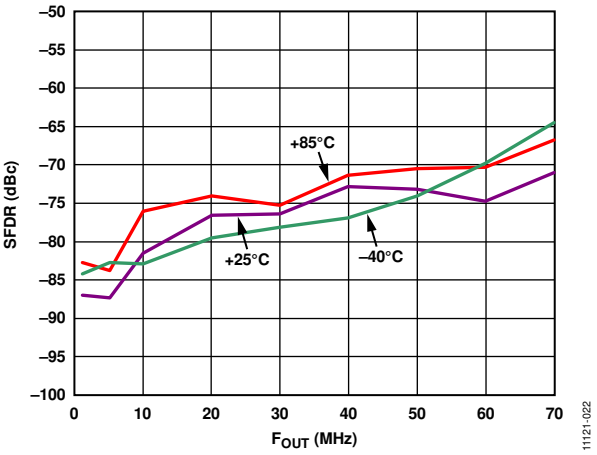

Figure 21. SFDR at Three Temperatures vs. F_{OUT}

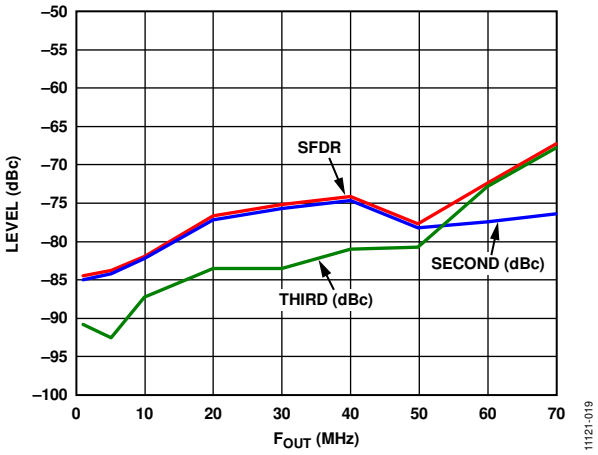

Figure 19. SFDR, 2nd and 3rd Harmonics at I_{OUTFS} = 2 mA vs. F_{OUT}

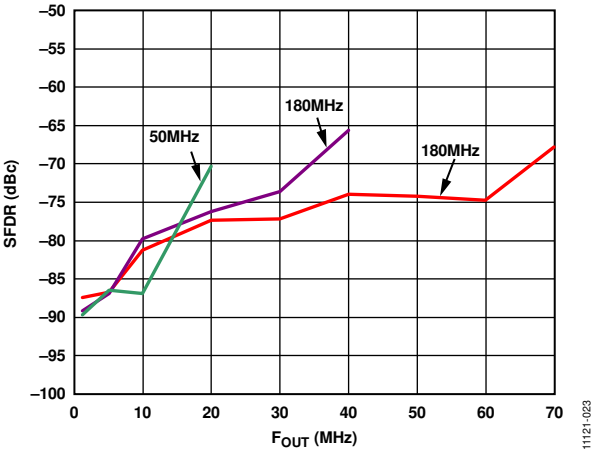

Figure 22. SFDR at Three F_{DAC} vs. F_{OUT}

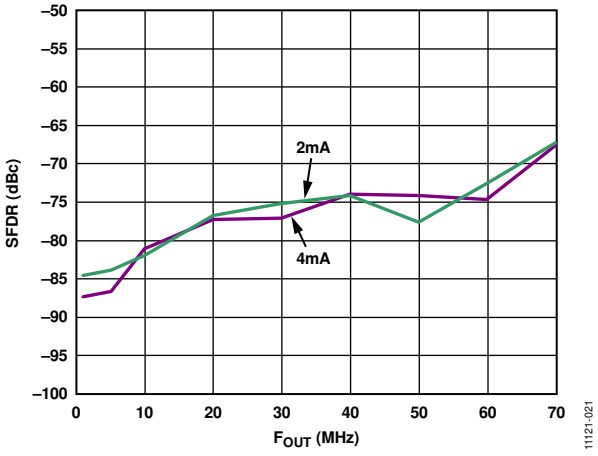

Figure 20. SFDR at Two I_{OUTFS} vs. F_{OUT}

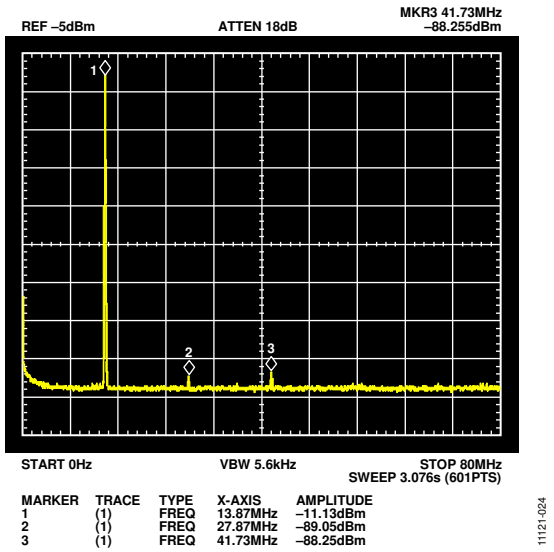

Figure 23. Output Spectrum F_{OUT} = 13.87 MHz

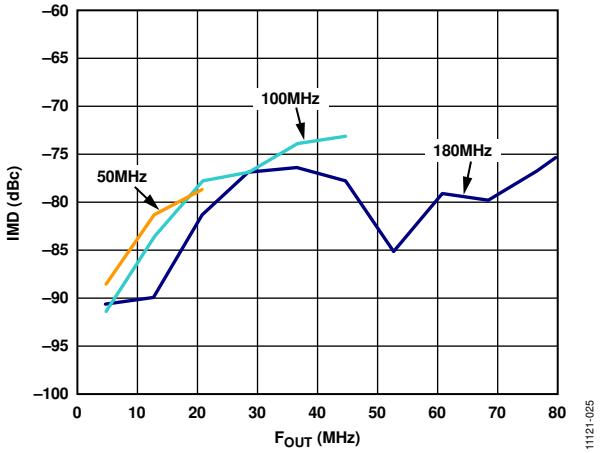

Figure 24. IMD vs. F_{OUT}, Three F_{OUT} Values

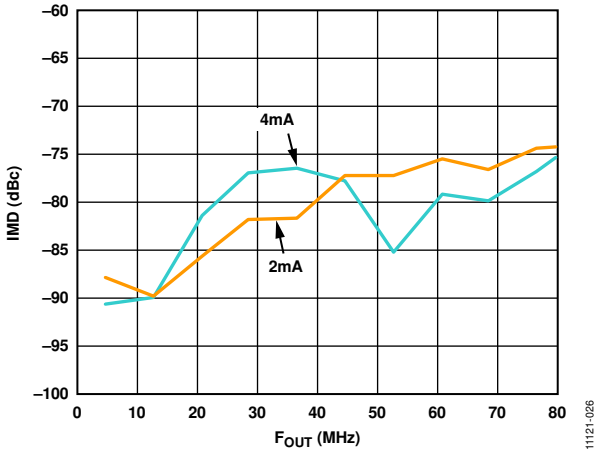

Figure 25. IMD vs. F_{OUT}, Two I_{OUTFS} Values

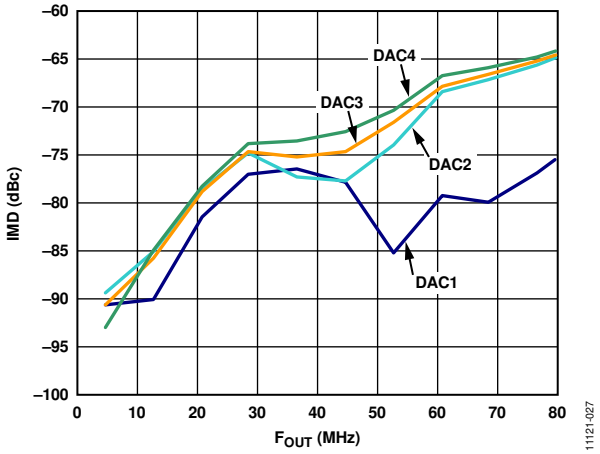

Figure 26. IMD vs. F_{OUT}, All Four DACs

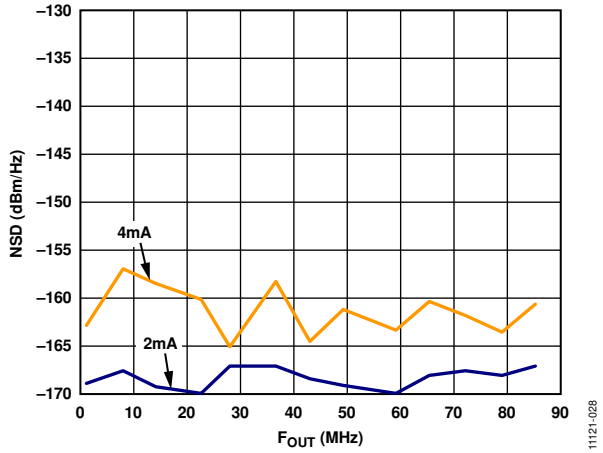

Figure 27. NSD vs. F_{OUT}, Two I_{OUTFS} Values

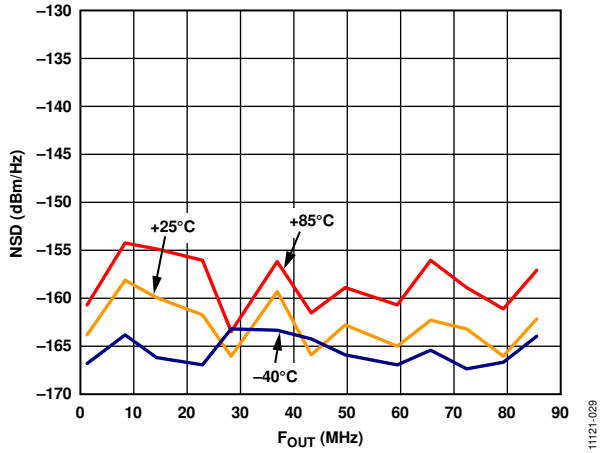

Figure 28. NSD vs. F_{OUT} at Three Temperatures

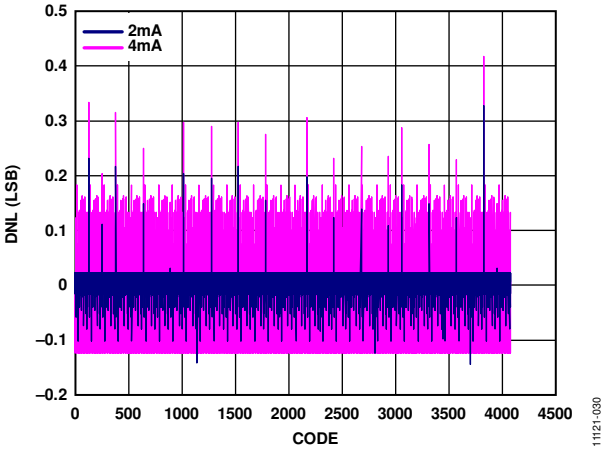

Figure 29. DNL, Three I_{OUTFS} Values

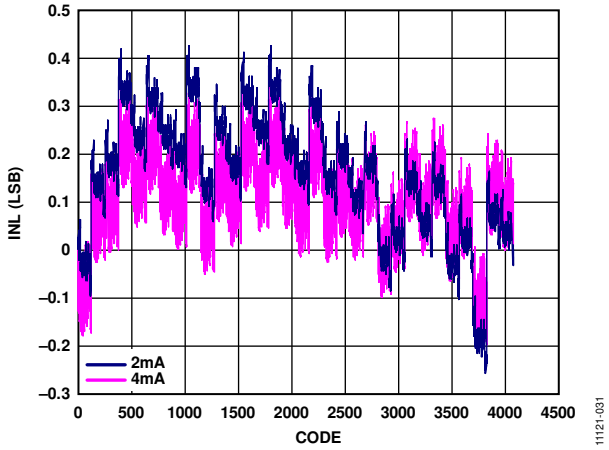

Figure 30. INL, Two I_{OUTFS} Values

TERMINOLOGY

Linearity Error (Integral Nonlinearity or INL)
INL is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A digital-to-analog converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
Offset error is the deviation of the output current from the ideal of zero. For IOUTPx, 0 mA output is expected when the inputs are all 0s. For IOUTNz, 0 mA output is expected when all inputs are set to 1.

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1, minus the output when all inputs are set to 0. The ideal gain is calculated using the measured VREF. Therefore, the gain error does not include effects of the reference.

Output Compliance Voltage
Output compliance voltage is the range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection
Power supply rejection is the maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in picovolt-seconds (pV-s).

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Noise Spectral Density (NSD)
Noise spectral density is the average noise power normalized to a 1 Hz bandwidth, with the DAC converting and producing an output tone.

THEORY OF OPERATION

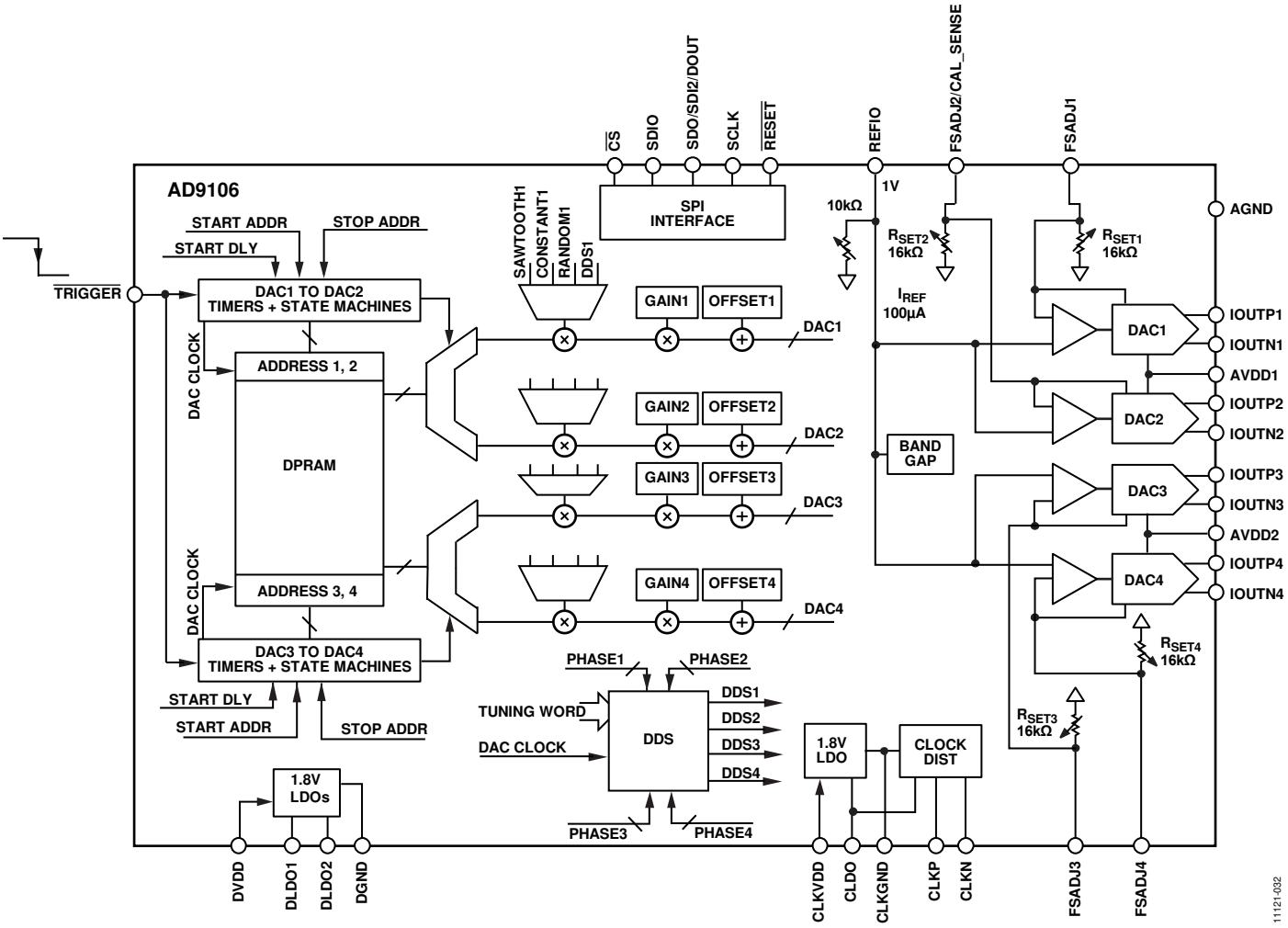

Figure 31. AD9106 Block Diagram

Figure 31 is a block diagram of the AD9106. The AD9106 has four 12-bit current output DACs.

The DACs use a single common voltage reference. An on-chip band gap reference is provided. Optionally, an off-chip voltage reference may be used. Full-scale DAC output current, also known as gain, is governed by the current, I_{REF}. I_{REF} is the current that flows through each I_{REF} resistor. Each DAC has its own I_{REF} set resistor. These resistors may be on or off chip at the discretion of the user. When on-chip R_{SET} resistors are in use DAC gain accuracy can be improved by employing the product's built in automatic gain calibration capability. Automatic calibration may be used with the on-chip reference or an external REFIO voltage. A procedure for automatic gain calibration is presented in this section.

The power supply rails for the AD9106 are AVDD for analog circuits, CLKVDD/CLDO for clock input receiver and DVDD/DLDO1/DLDO2 for digital I/O and for the on-chip digital data path. AVDD, DVDD, and CLKVDD can range from 1.8 V to 3.3 V nominal. DLDO1, DLDO2, and CLDO run at 1.8 V. If DVDD = 1.8 V, then DLDO1 and DLDO2 should both be connected to DVDD, with the on-chip LDOs disabled. All three supplies are provided externally in this case. This also applies to CLKVDD and CLDO if CLKVDD = 1.8 V.

Digital signals input to the four DACs are generated by on-chip digital waveform generation resources. Twelve-bit samples are input to each DAC at the CLKP/CLKN sample rate from a dedicated digital data path. Each DAC's data path includes gain and offset corrections and a digital waveform source selection multiplexer. Waveform sources are SRAM, direct digital synthesizer (DDS), DDS output amplitude modulated by SRAM data, a sawtooth generator, dc constant, and a pseudo-random sequence generator. The waveforms output by the source selection multiplexer have programmable pattern characteristics. The waveforms can be set up to be continuous, continuous pulsed (fixed pattern period and start delay within each pattern period), or finite pulsed (a set number of pattern periods are output, then the pattern stops).

Pulsed waveforms (finite or continuous) have a programmed pattern period and start delay. The waveform is present in each

pulse period following the global (applies to all four DACs) programmed pattern period start and each DAC's start delay.

An SPI port enables loading of data into SRAM and programming of all the control registers inside the device.

SPI PORT

The AD9106 provides a flexible, synchronous serial communications (SPI) port that allows easy interfacing to ASICs, FPGAs, and industry standard microcontrollers. The interface allows read/write access to all registers that configure the AD9106 and to the on-chip SRAM. Its data rate can be up to the SCLK clock speed shown in Table 3 and Table 4.

The SPI interface operates as a standard synchronous serial communication port. $\overline{CS}$ is a low true chip select. When $\overline{CS}$ goes true, SPI address and data transfer begins. The first bit coming from the SPI master on SDIO is a read/write indicator (high for read, low for write). The next 15-bits are the initial register address. The SPI port automatically increments the register address if $\overline{CS}$ stays low beyond the first data word allowing writes to or reads from a set of contiguous addresses.

Table 12. Command Word

MSB							LSB
DB15	**DB14**	**DB13**	**DB12**	**…**	**DB2**	**DB1**	**DB0**
$\overline{RW}$	A14	A13	A12	…	A2	A1	A0

When the first bit of this command byte is a logic low ($\overline{RW}$ bit = 0), the SPI command is a write operation. In this case, SDIO remains an input (see Figure 32).

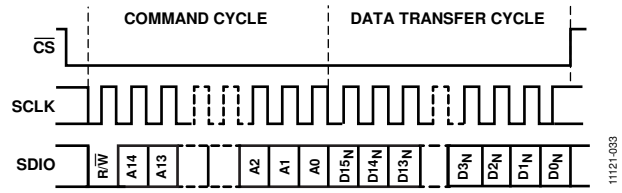

Figure 32. Serial Register Interface Timing, MSB First Write, 3-Wire SPI

When the first bit of this command byte is a logic high ($\overline{RW}$ bit = 1), the SPI command is a read operation. In this case, data is driven out of the SPI port as shown in Figure 33 and Figure 34. The SPI communication finishes after the $\overline{CS}$ pin goes high.

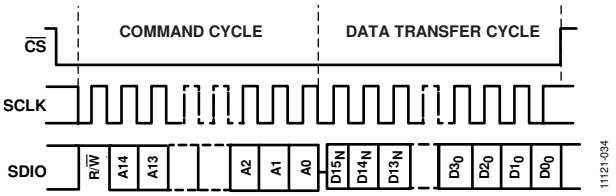

Figure 33. Serial Register Interface Timing, MSB First Read, 3-Wire SPI

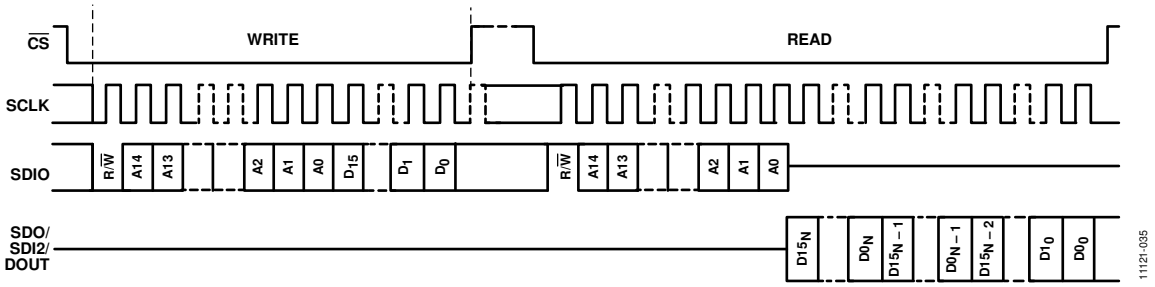

Figure 34. Serial Register Interface Timing, MSB First Read, 4-Wire SPI

Writing to On-Chip SRAM

The AD9106 includes an internal 4096 × 12 SRAM. The SRAM address space is 0x6000 to 0x6FFF of the AD9106 SPI address map.

Double SPI for Write for SRAM

The time to write data to the entire SRAM can be halved using the SPI access mode shown in Figure 35. The SDO/SDI2/DOUT line becomes a second serial data input line, doubling the achievable update rate of the on-chip SRAM. SDO/SDI2/DOUT is write-only in this mode. The entire SRAM can be written in $(2 + 2 \times 4096) \times 8/(2 \times F_{SCLK})$ seconds.

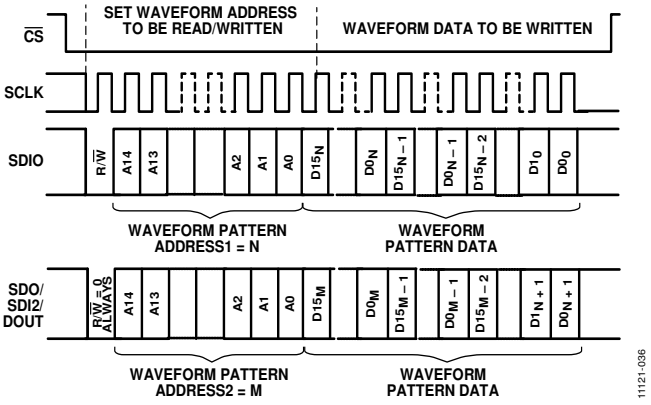

Figure 35. Double SPI Write of SRAM Data

Configuration Register Update Procedure

Most SPI accessible registers are double buffered. An active register set controls operation of the AD9106 during pattern generation. A set of shadow registers stores updated register values. Register updates can be written at any time and when the configuration update is complete, a 1 is written to the UPDATE bit in the RAMUPDATE register. The UPDATE bit arms the register set for transfer from shadow registers to active registers. The AD9106 will perform this transfer automatically the next time the pattern generator is off. This procedure does not apply to the 4K × 12 SRAM. Refer to the SRAM section for the SRAM update procedure.

DAC TRANSFER FUNCTION

The AD9106 DACs provide four differential current outputs: IOUTP1/IOUTN1, IOUTP2/IOUTN2, IOUTP3/IOUTN3, and IOUTP4/IOUTN4.

The DAC output current equations are as follows:

$$IOUTPx = I_{OUTFSx} \times xDAC\ INPUT\ CODE/2^{12} \quad (1)$$

$$IOUTNx = I_{OUTFSx} \times ((2^{12} - 1) - xDAC\ INPUT\ CODE)/2^{12} \quad (2)$$

where:
xDAC INPUT CODE = 0 to $2^{12} - 1$.
I_{OUTFSx} = full-scale current or DAC gain set independently for each DAC.

$$I_{OUTFSx} = 32 \times I_{IREFx} \quad (3)$$

where:

$$I_{REFx} = V_{REFIO}/xR_{SET} \quad (4)$$

I_{REFx} is the current that flows through each I_{REFx} resistor. Each DAC has its own I_{REF} set resistor. I_{REF} resistors may be on or off chip at the users' discretion. When on-chip xR_{SET} resistors are in use, DAC gain accuracy can be improved by employing the product's built in automatic gain calibration capability.

ANALOG CURRENT OUTPUTS

Optimum linearity and noise performance of DAC outputs can be achieved when they are connected differentially to an amplifier or a transformer. In these configurations, common-mode signals at the DAC outputs are rejected.

The output compliance voltage specifications shown in Table 1 and Table 2 must be adhered to for the performance specifications in these tables to be met.

SETTING I_{OUTFSx}, DAC GAIN

As expressed in Equation 3 and Equation 4, DAC gain (I_{OUTFSx}) is a function of the reference voltage at the REFIO terminal and xR_{SET} for each DAC.

Voltage Reference

The AD9106 contains an internal 1.0 V nominal band gap reference. The internal reference may be used. Alternatively, it can be replaced by a more accurate off-chip reference. An external reference can provide tighter reference voltage tolerances and/or lower temperature drift than the on-chip band gap.

By default, the on-chip reference is powered up and ready to be used. When using the on-chip reference, the REFIO terminal needs to be decoupled to AGND using a 0.1 µF capacitor as shown in Figure 36.

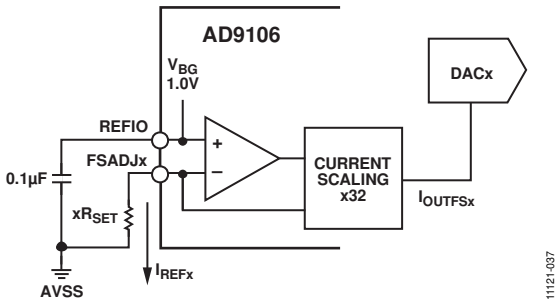

Figure 36. On-Chip Reference with External xR_{SET} Resistor

Table 13 summarizes reference connections and programming.

Table 13. Reference Operation

Reference Mode	REFIO Pin
Internal	Connect 0.1 µF capacitor
External	Connect off-chip reference

Programming Internal V_{REFIO}

The internal REFIO voltage level is programmable.

When the internal voltage reference is in use, the BGDR field in the lower six bits in Register 0x03 adjusts the V_{REFIO} level. This adds or subtracts up to 20% from the nominal band gap voltage on REFIO. The voltage across the FSADJx resistors tracks this change. As a result, I_{REFx} varies by the same amount. Figure 37 shows V_{REFIO} vs. BGDR code for an on-chip reference with a default voltage (BGDR = 0x00) of 1.04 V.

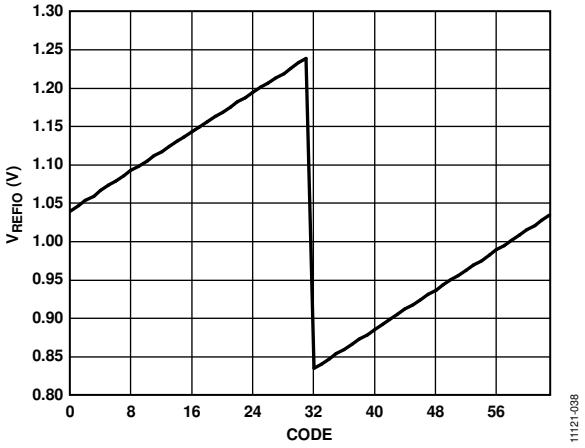

Figure 37. Typical V_{REF} Voltage vs. BGDR

xR_{SET} Resistors

xR_{SET} in Equation 4 for each DAC can be an internal resistor or a board level resistor of the users choosing connected to the appropriate FSADJx terminal.

To make use of on-chip xR_{SET} resistors, Bit15 of Register 0x0C, Register 0x0B, Register 0x0A, and Register 0x09 for DAC1, DAC2, DAC3, and DAC4, respectively, are set to Logic 1. Bits[4:0] of Register 0x0C, Register 0x0B, Register 0x0A, and Register 0x09 are used to manually program values for the on-chip xR_{SET} associated with DAC1, DAC2, DAC3, and DAC4, respectively.

AUTOMATIC I_{OUTFSX} CALIBRATION

Many applications require tight DAC gain control. The AD9106 provides an automatic I_{OUTFSx} calibration procedure used with on-chip xR_{SET} resistors only. The voltage reference V_{REFIO} can be the on-chip reference or an off-chip reference. The automatic calibration procedure does a fine adjustment of each internal xR_{SET} value and each current I_{REFx}.

When using automatic calibration the following board-level connections are required:

1. Connect FSADJ1 and FSADJ2/CAL_SENSE together.
2. A resistor should be installed between FSADJ2/CAL_SENSE and ground. The value of this resistor should be $R_{CAL\_SENSE} = 32 \times V_{REFIO}/I_{OUTFS}$ where I_{OUTFS} is the target full-scale current for all four DACs.

Automatic calibration uses an internal clock. This calibration clock is equal to the DAC clock divided by the division factor chosen by the CAL_CLK_DIV bits of Register 0x0D. Each calibration cycle is between 4 and 512 DAC clock cycles, depending on the value of CAL_CLK_DIV[2:0]. The frequency of the calibration clock should be less than 500 kHz.

To perform an automatic calibration, follow these steps:

1. Set the calibration ranges in Registers 0x08[7:0] and 0x0D[5:4] to their minimum values to allow best calibration.
2. Enable the calibration clock bit, CAL_CLK_EN, in Register 0x0D.
3. Set the divider ratio for the calibration clock by setting CAL_CLK_DIV[2:0] bits in Register 0x0D. The default is 512.
4. Set the CAL_MODE_EN bit in Register 0x0D to Logic 1.
5. Set the START_CAL bit in Register 0x000E to Logic 1. This begins the calibration of the comparator, xR_{SET} and gain.
6. The CAL_MODE flag in Register 0x000D will go to Logic 1 while the part is calibrating. The CAL_FIN flag in Register 0x0E will go to Logic 1 when the calibration is complete.
7. Set the START_CAL bit in Register 0x0E to Logic 0.
8. After calibration, verify that the overflow and underflow flags in Register 0x0D are not set (Bits[14:8]). If they are, change the corresponding calibration range to the next larger range and begin again at Step 5.
9. If no flag is set, read the DACx_RSET_CAL and DACx_AGAIN_CAL values in the DACxRSET[12:8] and DACxGAIN[14:8] registers, respectively, and write them into their corresponding DACxRSET and DACxAGAIN registers.
10. Reset the CAL_MODE_EN bit and the calibration clock bit CAL_CLK_EN in Register 0x0D to Logic 0 to disable the calibration clock.
11. Set the CAL_MODE_EN bit in Register 0x0D to Logic 0. This sets the RSET and gain control muxes towards the regular registers.
12. Disable the calibration clock bit, CAL_CLK_EN, in Register 0x0D.

To reset the calibration, pulse the CAL_RESET bit in Register 0x0D to Logic 1 and Logic 0, pulse the $\overline{\text{RESET}}$ pin, or pulse the RESET bit in the SPICONFIG register.

CLOCK INPUT

For optimum DAC performance, the AD9106 clock input signal pair (CLKP/CLKN) should be a very low jitter, fast rise time differential signal. The clock receiver generates its own common-mode voltage requiring these two inputs to be ac-coupled.

Figure 38 shows the recommended interface to a number of Analog Devices, Inc., LVDS clock drivers that work well with the AD9106. A 100 Ω termination resistor and two 0.1 µF coupling capacitors are used. Figure 40 shows an interface to an Analog Devices differential PECL driver. Figure 41 shows a single-ended-to-differential converter using a balun driving CLKP/CLKN, the preferred methods for clocking the AD9106.

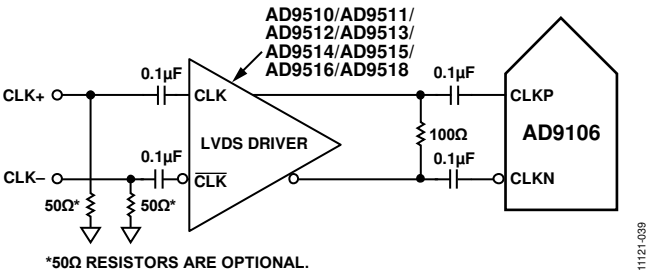

Figure 38. Differential LVDS Clock Input

In applications where the analog output signals are at low frequencies, it is acceptable to drive the AD9106 clock input with a single-ended CMOS signal. Figure 39 shows such an interface. CLKP is driven directly from a CMOS gate, and the CLKN pin is bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor. The optional resistor is a series termination.

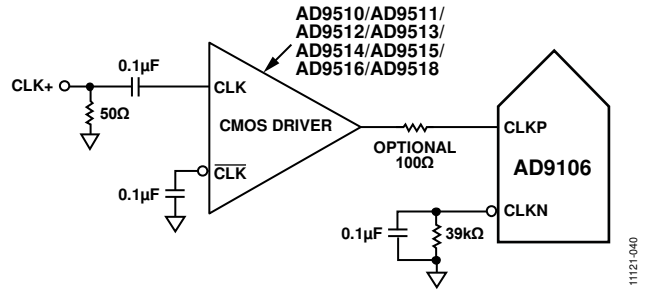

Figure 39. Single-Ended 1.8 V CMOS Sample Clock

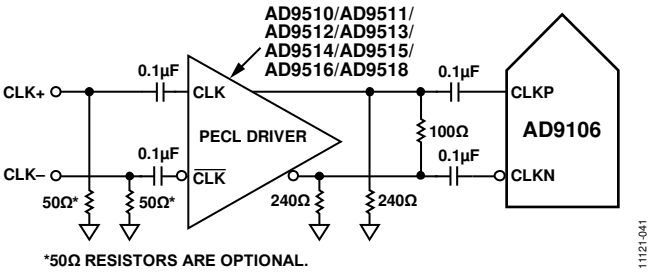

Figure 40. Differential PECL Sample Clock

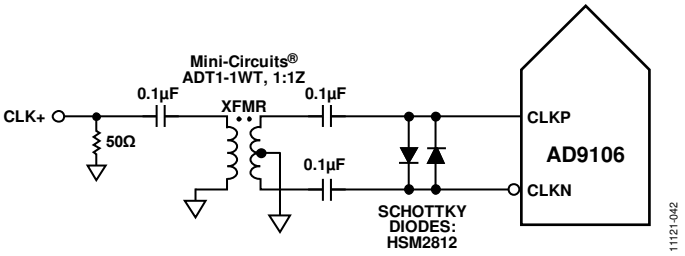

Figure 41. Transformer Coupled Clock

DAC OUTPUT CLOCK EDGE

Each of the four DACs can be configured independently to output samples on the rising or falling edge of the CLKP/CLKN clock input by configuring the DACx_INV_CLK bits in the CLOCKCONFIG register. This functionality sets the DAC output timing resolution at $1/(2 \times F_{CLKP/CLKN})$.

GENERATING SIGNAL PATTERNS

The AD9106 can generate three types of signal patterns under control of its programmable pattern generator.

- Continuous waveforms
- Periodic pulse train waveforms that repeat indefinitely
- Periodic pulse train waveforms that repeat a finite number of times

Run Bit

Setting the RUN bit in the PAT_STATUS register to 1 arms the AD9106 for pattern generation. Clearing this bit shuts down the pattern generator as shown in Figure 45.

Trigger Terminal

A falling edge on the trigger terminal starts the generation of a pattern. If RUN is set, the falling edge of trigger starts pattern generation. As shown in Figure 43, the pattern generator state goes to "pattern on" a number of CLKP/CLKN clock cycles following the falling edge of trigger. This delay is programmed in the PATTERN_DELAY bit field.

The rising edge on the trigger terminal is a request for the termination of pattern generation (see Figure 44).

Pattern Bit (Read Only)

The read-only PATTERN bit in the PAT_STATUS register indicates, when set to 1, that the pattern generator is in the "pattern on" state. A 0 indicates that the pattern generator is in the "pattern off" state.