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TOSHIBA Field Effect Transistor Silicon P Channel MOS Type(π-MOSVI)

SSM6P16FE

High Speed Switching Applications

Analog Switch Applications

- Small package
- Low on-resistance : $R_{DS(ON)} = 8 \Omega$ (max) (@ $V_{GS} = -4$ V)
: $R_{DS(ON)} = 12 \Omega$ (max) (@ $V_{GS} = -2.5$ V)
: $R_{DS(ON)} = 45 \Omega$ (max) (@ $V_{GS} = -1.5$ V)

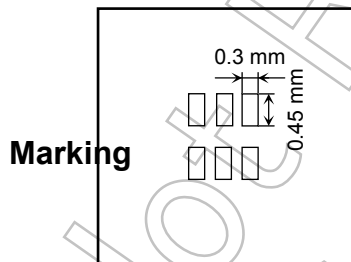
Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$) (Q1, Q2 Common)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	-20	V
Gate-Source voltage		V_{GSS}	± 10	V
Drain current	DC	I_D	-100	mA
	Pulse	I_{DP}	-200	
Power dissipation		P_D (Note 1)	150	mW
Channel temperature		T_{ch}	150	$^\circ\text{C}$
Storage temperature range		T_{stg}	-55 to 150	$^\circ\text{C}$

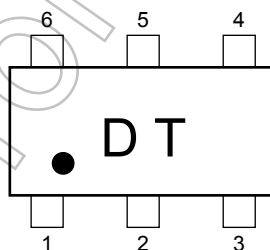
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

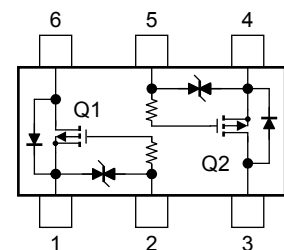
Note 1: Total rating, mounted on FR4 board
(25.4 mm \times 25.4 mm \times 1.6 mm, Cu Pad: 0.135 mm² \times 6)



Marking



Equivalent Circuit (top view)

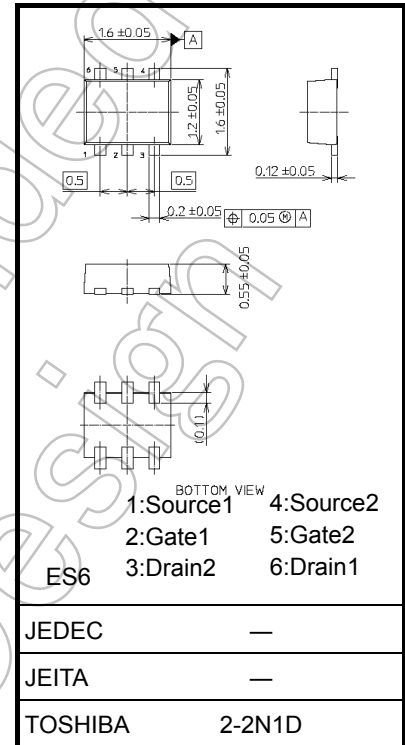


Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Start of commercial production
2002-01

Unit: mm



Weight: 3.0 mg (typ.)

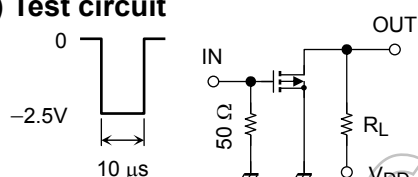
Electrical Characteristics (Ta = 25°C) (Q1, Q2 common)

Characteristic		Symbol	Test Condition	MIN.	TYP.	MAX.	UNIT
Gate leakage current		I_{GSS}	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0$	—	—	± 1	μA
Drain-Source breakdown voltage		$V_{(BR) DSS}$	$I_D = -0.1 \text{ mA}, V_{GS} = 0$	-20	—	—	V
Drain cut-off current		I_{DSS}	$V_{DS} = -20 \text{ V}, V_{GS} = 0$	—	—	-1	μA
Gate threshold voltage		V_{th}	$V_{DS} = -3 \text{ V}, I_D = -0.1 \text{ mA}$	-0.6	—	-1.1	V
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = -3 \text{ V}, I_D = -10 \text{ mA}$ (Note2)	25	—	—	mS
Drain-Source on-resistance		$R_{DS(ON)}$	$I_D = -10 \text{ mA}, V_{GS} = -4 \text{ V}$ (Note2)	—	6	8	Ω
			$I_D = -10 \text{ mA}, V_{GS} = -2.5 \text{ V}$ (Note2)	—	8	12	
			$I_D = -1 \text{ mA}, V_{GS} = -1.5 \text{ V}$ (Note2)	—	18	45	
Input capacitance		C_{iss}	$V_{DS} = -3 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	11	—	pF
Reverse transfer capacitance		C_{rss}		—	3.7	—	pF
Output capacitance		C_{oss}		—	10	—	pF
Switching time	Turn-on time	t_{on}	$V_{DD} = -3 \text{ V}, I_D = -10 \text{ mA},$ $V_{GS} = 0 \text{ to } -2.5 \text{ V}$	—	130	—	ns
	Turn-off time	t_{off}		—	190	—	

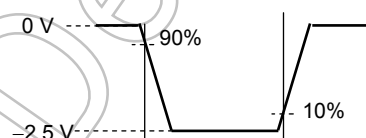
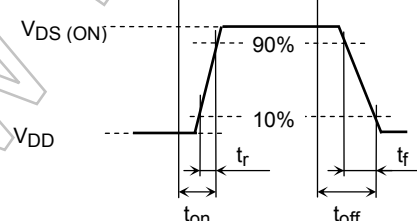
Note2: Pulse test

Switching Time Test Circuit

(a) Test circuit



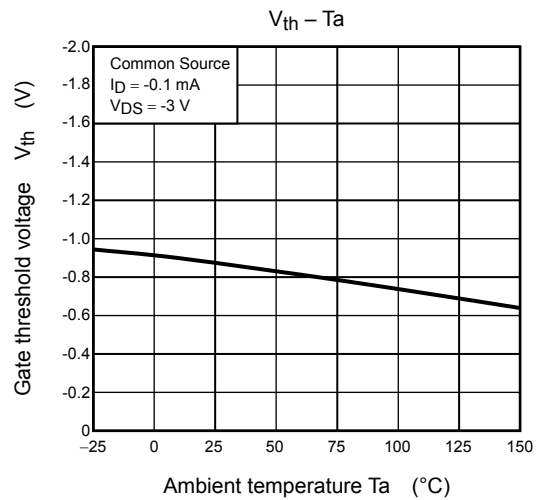
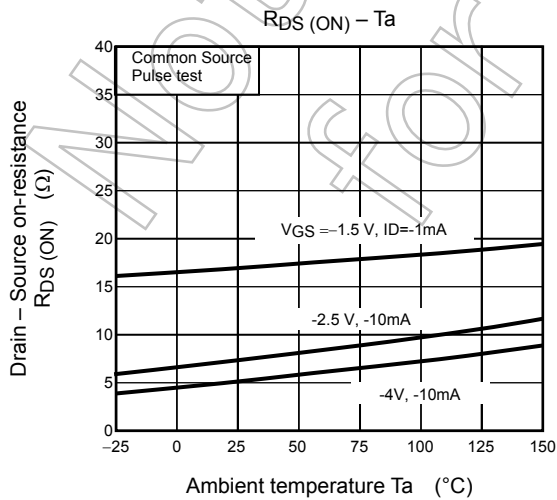
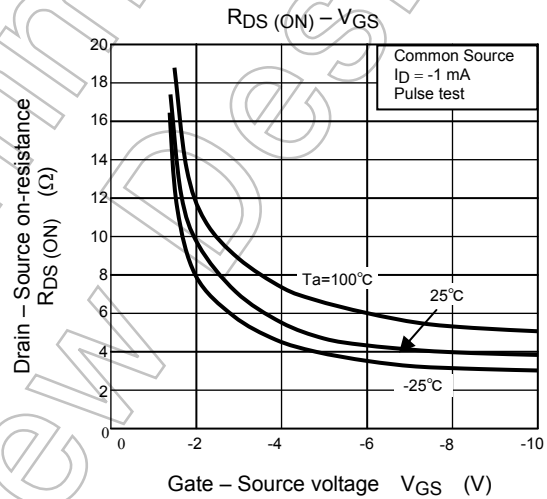
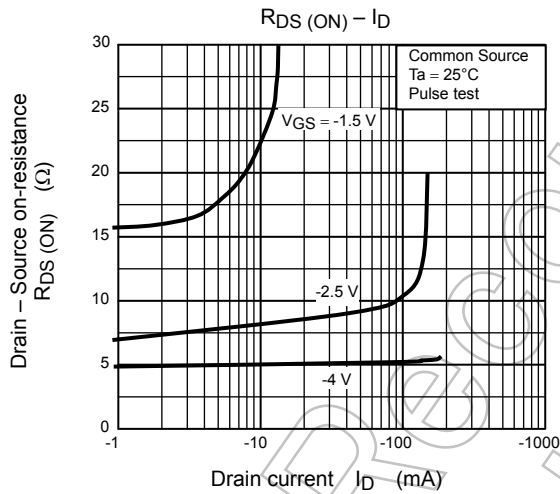
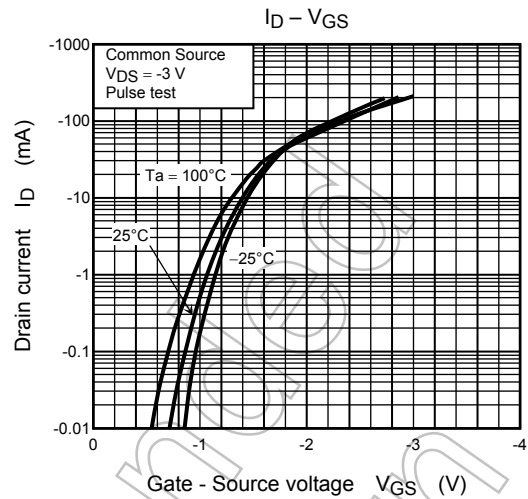
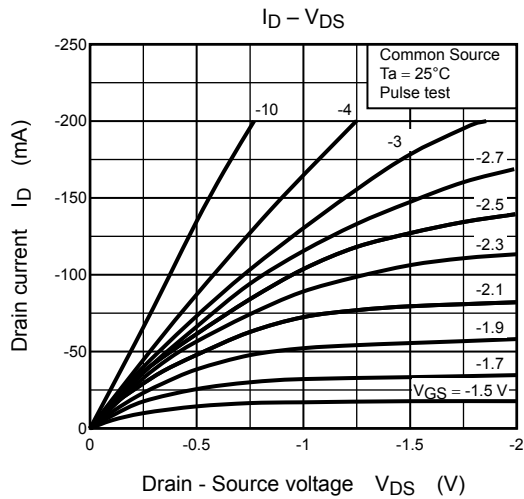
$V_{DD} = -3 \text{ V}$
 Duty $\leq 1\%$
 V_{IN} : $t_r, t_f < 5 \text{ ns}$
 $(Z_{out} = 50 \Omega)$
 Common Source
 $T_a = 25^\circ\text{C}$

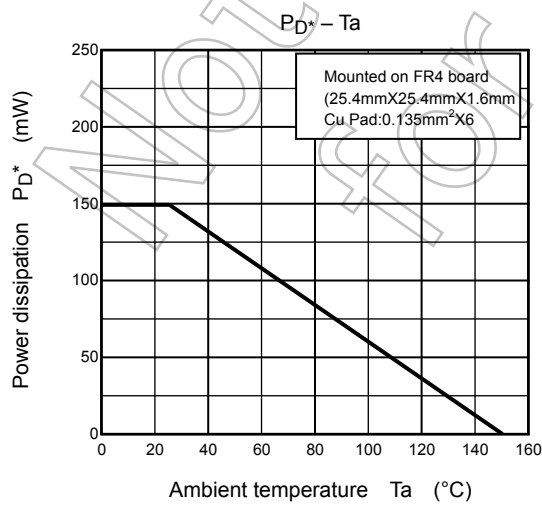
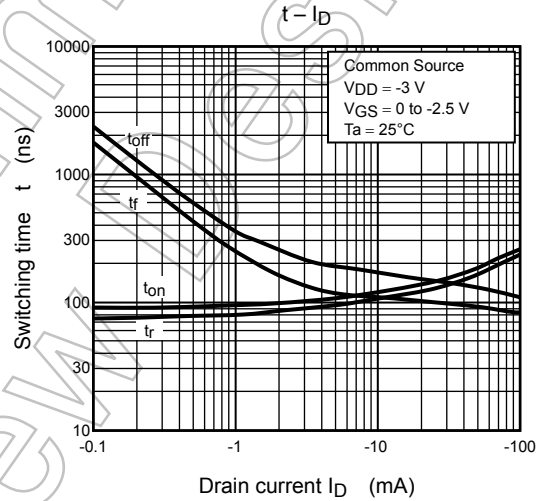
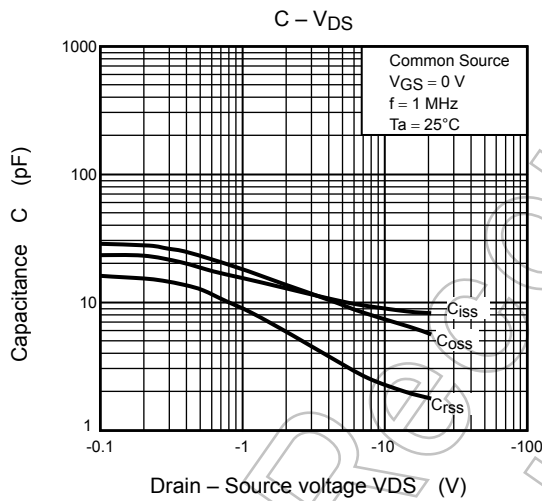
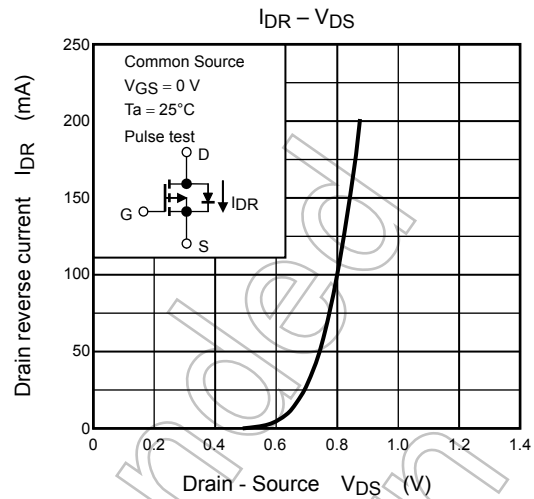
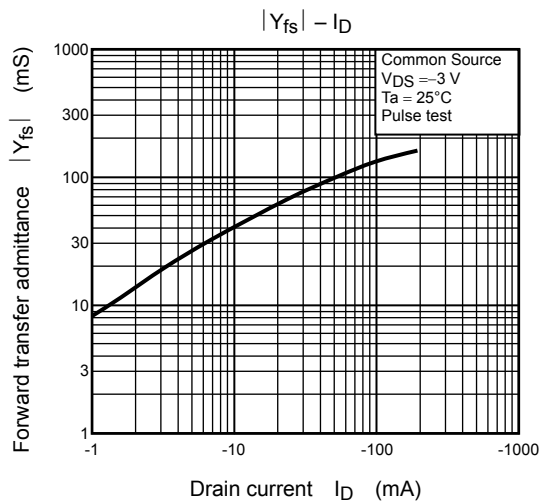
(b) V_{IN} (c) V_{OUT} 

Precaution

V_{th} can be expressed as the voltage between the gate and source when the low operating current value is $I_D = -0.1 \text{ mA}$ for this product. For normal switching operation, $V_{GS(on)}$ requires a higher voltage than V_{th} and $V_{GS(off)}$ requires a lower voltage than V_{th} . (The relationship can be established as follows: $V_{GS(off)} < V_{th} < V_{GS(on)}$.)

Be sure to take this into consideration when using the device.





*:Total rating

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