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Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# MB96640 Series

# F²MC-16FX 16-Bit Microcontroller

MB96640 series is based on Cypress advanced F²MC-16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established F²MC-16LX family thus allowing for easy migration of F²MC-16LX Software to the new F²MC-16FX products.
F²MC-16FX product improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For high processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 32MHz operation frequency from an external 4MHz to 8MHz resonator. The result is a minimum instruction cycle time of 31.2ns going together with excellent EMI behavior. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows selecting suitable operation frequencies for peripheral resources independent of the CPU speed.

## Features

- Technology
  - 0.18µm CMOS
- CPU
  - F²MC-16FX CPU
  - Optimized instruction set for controller applications (bit, byte, word and long-word data types, 23 different addressing modes, barrel shift, variety of pointers)
  - 8-byte instruction queue
  - Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available
- System clock
  - On-chip PLL clock multiplier (×1 to ×8, ×1 when PLL stop)
  - 4MHz to 8MHz crystal oscillator (maximum frequency when using ceramic resonator depends on Q-factor)
  - Up to 8MHz external clock for devices with fast clock input feature
  - 32.768kHz subsystem quartz clock
  - 100kHz/2MHz internal RC clock for quick and safe startup, clock stop detection function, watchdog
  - Clock source selectable from mainclock oscillator, subclock oscillator and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals
  - The subclock oscillator is enabled by the Boot ROM program controlled by a configuration marker after a Power or External reset
  - Low Power Consumption - 13 operating modes (different Run, Sleep, Timer, Stop modes)
- On-chip voltage regulator

  Internal voltage regulator supports a wide MCU supply voltage range (Min=2.7V), offering low power consumption
- Low voltage detection function

  Reset is generated when supply voltage falls below programmable reference voltage
- Code Security

  Protects Flash Memory content from unintended read-out
- DMA

  Automatic transfer function independent of CPU, can be assigned freely to resources
- Interrupts
  - Fast Interrupt processing
  - 8 programmable priority levels
  - Non-Maskable Interrupt (NMI)
- CAN
  - Supports CAN protocol version 2.0 part A and B
  - ISO16845 certified
  - Bit rates up to 1Mbps
  - 32 message objects
  - Each message object has its own identifier mask
  - Programmable FIFO mode (concatenation of message objects)
  - Maskable interrupt
  - Disabled Automatic Retransmission mode for Time Triggered CAN applications
  - Programmable loop-back mode for self-test operation
- USART
  - Full duplex USARTs (SCI/LIN)
  - Wide range of baud rate settings using a dedicated reload timer
  - Special synchronous options for adapting to different synchronous serial protocols
  - LIN functionality working either as master or slave LIN device
  - Extended support for LIN-Protocol to reduce interrupt load
- I²C
  - Up to 400kbps
  - Master and Slave functionality, 7-bit and 10-bit addressing
- A/D converter
  - SAR-type
  - 8/10-bit resolution
  - Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
  - Range Comparator Function
  - Scan Disable Function
- Source Clock Timers

  Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)

- Hardware Watchdog Timer
  - Hardware watchdog timer is active after reset
  - Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval
- Reload Timers
  - 16-bit wide
  - Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
  - Event count function
- Free-Running Timers
  - Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
  - Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency
- Input Capture Units
  - 16-bit wide
  - Signals an interrupt upon external event
  - Rising edge, Falling edge or Both (rising & falling) edges sensitive
- Output Compare Units
  - 16-bit wide
  - Signals an interrupt when a match with Free-running Timer occurs
  - A pair of compare registers can be used to generate an output signal
- Programmable Pulse Generator
  - 16-bit down counter, cycle and duty setting registers
  - Can be used as 2 × 8-bit PPG
  - Interrupt at trigger, counter borrow and/or duty match
  - PWM operation and one-shot operation
  - Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock or of selected Reload timer underflow as clock input
  - Can be triggered by software or reload timer
  - Can trigger ADC conversion
  - Timing point capture
  - Start delay
- Quadrature Position/Revolution Counter (QPRC)
  - Up/down count mode, Phase difference count mode, Count mode with direction
  - 16-bit position counter
  - 16-bit revolution counter
  - Two 16-bit compare registers with interrupt
  - Detection edge of the three external event input pins AIN, BIN and ZIN is configurable
- Real Time Clock
  - Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
  - Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
  - Read/write accessible second/minute/hour registers
  - Can signal interrupts every half second/second/minute/hour/day
  - Internal clock divider and prescaler provide exact 1s clock
- External Interrupts
  - Edge or Level sensitive
  - Interrupt mask bit per channel
  - Each available CAN channel RX has an external interrupt for wake-up
  - Selected USART channels SIN have an external interrupt for wake-up
- Non Maskable Interrupt
  - Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
  - Once enabled, cannot be disabled other than by reset
  - High or Low level sensitive
  - Pin shared with external interrupt 0
- I/O Ports
  - Most of the external pins can be used as general purpose I/O
  - All push-pull outputs (except when used as $I^2C$ SDA/SCL line)
  - Bit-wise programmable as input/output or peripheral signal
  - Bit-wise programmable input enable
  - One input level per GPIO-pin (either Automotive or CMOS hysteresis)
  - Bit-wise programmable pull-up resistor
- Built-in On Chip Debugger (OCD)
  - One-wire debug tool interface
  - Break function:
    - Hardware break: 6 points (shared with code event)
    - Software break: 4096 points
  - Event function
    - Code event: 6 points (shared with hardware break)
    - Data event: 6 points
    - Event sequencer: 2 levels + reset
  - Execution time measurement function
  - Trace function: 42 branches
  - Security function
- Flash Memory
  - Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
  - Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
  - Supports automatic programming, Embedded Algorithm
  - Write/Erase/Erase-Suspend/Resume commands
  - A flag indicating completion of the automatic algorithm
  - Erase can be performed on each sector individually
  - Sector protection
  - Flash Security feature to protect the content of the Flash
  - Low voltage detection during Flash erases or writes

## Contents

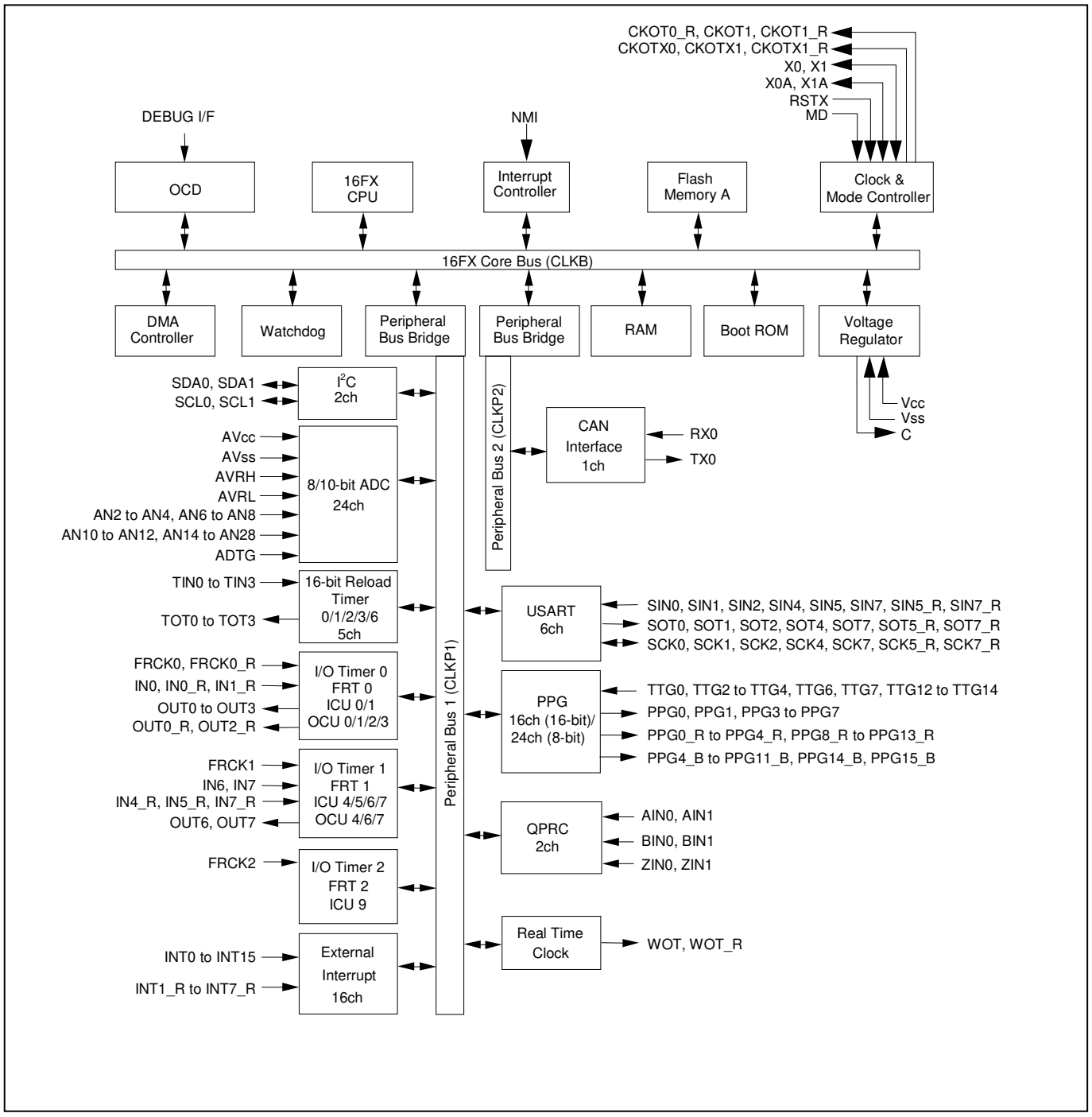
# 1. Product Lineup

| Features | | MB96640 | Remark |
|---|---|---|---|
| Product Type | | Flash Memory Product | |
| Subclock | | Subclock can be set by software | |
| Dual Operation Flash Memory | RAM | - | |
| 64.5KB + 32KB | 10KB | MB96F643R, MB96F643A | Product Options<br>R: MCU with CAN<br>A: MCU without CAN |
| 128.5KB + 32KB | 16KB | MB96F645R, MB96F645A | |
| 256.5KB + 32KB | 24KB | MB96F646R | |
| 384.5KB + 32KB | 28KB | MB96F647R | |
| Package | | LQFP-100<br>FPT-100P-M20 | |
| DMA | | 4ch | |
| USART | | 6ch | LIN-USART 0 to 2/4/5/7 |
| | with automatic LIN-Header transmission/reception | Yes (only 1ch) | LIN-USART 0 |
| | with 16 byte RX- and TX-FIFO | No | |
| $I^2C$ | | 2ch | $I^2C$ 0/1 |
| 8/10-bit A/D Converter | | 24ch | AN 2 to 4/6 to 8/10 to 12/14 to 28 |
| | with Data Buffer | No | |
| | with Range Comparator | Yes | |
| | with Scan Disable | Yes | |
| | with ADC Pulse Detection | No | |
| 16-bit Reload Timer (RLT) | | 5ch | RLT 0 to 3/6 |
| 16-bit Free-Running Timer (FRT) | | 3ch | FRT 0 to 2 |
| 16-bit Input Capture Unit (ICU) | | 7ch<br>(1 channel for LIN-USART) | ICU 0/1/4 to 7/9<br>(ICU 9 for LIN-USART) |
| 16-bit Output Compare Unit (OCU) | | 7ch | OCU 0 to 4/6/7<br>(OCU 4 for FRT clear) |
| 8/16-bit Programmable Pulse Generator (PPG) | | 16ch (16-bit) / 24ch (8-bit) | PPG 0 to 15 |
| | with Timing point capture | Yes | |
| | with Start delay | Yes | |
| | with Ramp | No | |
| Quadrature Position/Revolution Counter (QPRC) | | 2ch | QPRC 0/1 |
| CAN Interface | | 1ch | CAN 0<br>32 Message Buffers |
| External Interrupts (INT) | | 16ch | INT 0 to 15 |
| Non-Maskable Interrupt (NMI) | | 1ch | |
| Real Time Clock (RTC) | | 1ch | |
| I/O Ports | | 79 (Dual clock mode)<br>81 (Single clock mode) | |
| Clock Calibration Unit (CAL) | | 1ch | |
| Clock Output Function | | 2ch | |
| Low Voltage Detection Function | | Yes | Low voltage detection function can be disabled by software |
| Hardware Watchdog Timer | | Yes | |
| On-chip RC-oscillator | | Yes | |
| On-chip Debugger | | Yes | |

**Note:**

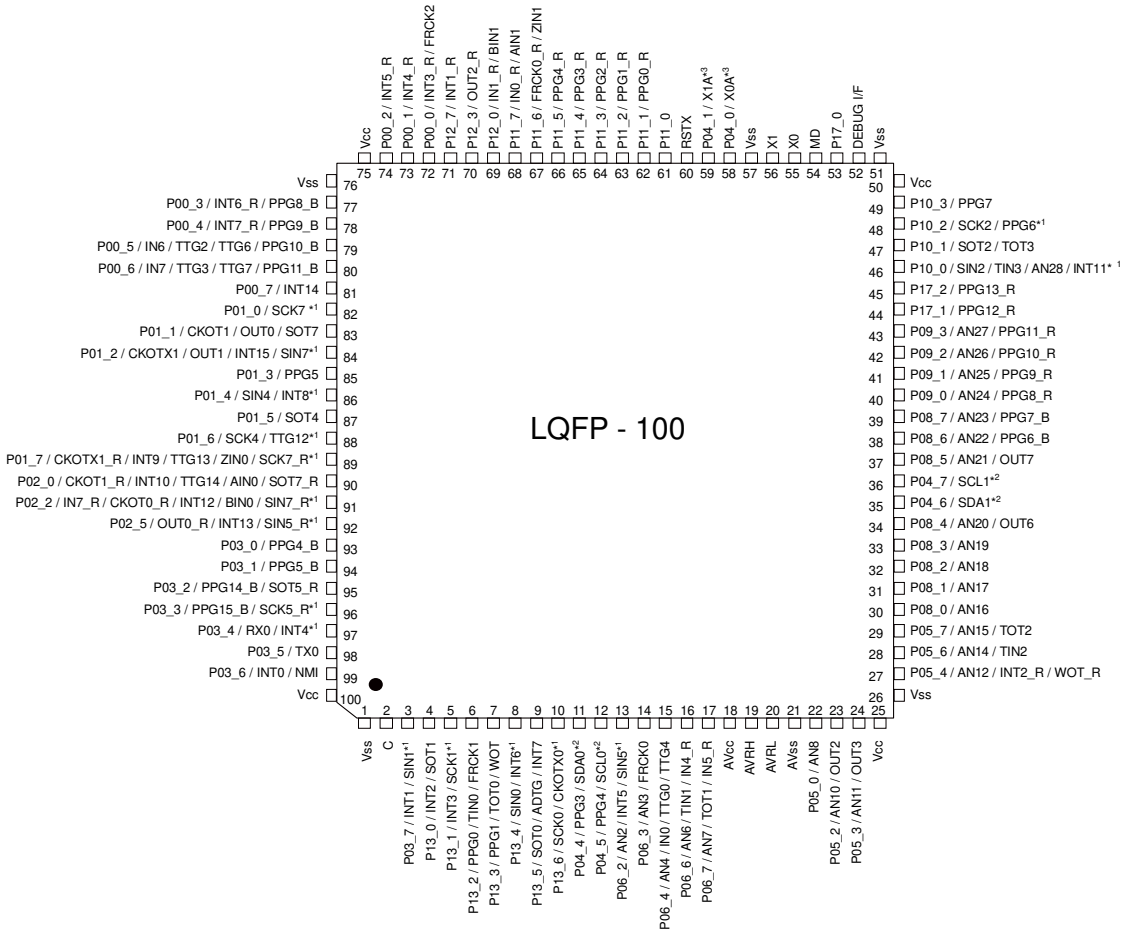
All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.
It is necessary to use the port relocate function of the general I/O port according to your function use.

## 2. Block Diagram



## 3. Pin Assignment

(Top view)




(FPT-100P-M20)

*1: CMOS input level only

*2: CMOS input level only for $I^2C$

*3: Please set ROM Configuration Block (RCB) to use the subclock.

Other than those above, general-purpose pins have only automotive input level.

## 4. Pin Description

| Pin name | Feature | Description |
|---|---|---|
| ADTG | ADC | A/D converter trigger input pin |
| AINn | QPRC | Quadrature Position/Revolution Counter Unit n input pin |
| ANn | ADC | A/D converter channel n input pin |
| AVcc | Supply | Analog circuits power supply pin |
| AVRH | ADC | A/D converter high reference voltage input pin |
| AVRL | ADC | A/D converter low reference voltage input pin |
| AVss | Supply | Analog circuits power supply pin |
| BINn | QPRC | Quadrature Position/Revolution Counter Unit n input pin |
| C | Voltage regulator | Internally regulated power supply stabilization capacitor pin |
| CKOTn | Clock Output function | Clock Output function n output pin |
| CKOTn_R | Clock Output function | Relocated Clock Output function n output pin |
| CKOTXn | Clock Output function | Clock Output function n inverted output pin |
| CKOTXn_R | Clock Output function | Relocated Clock Output function n inverted output pin |
| DEBUG I/F | OCD | On Chip Debugger input/output pin |
| FRCKn | Free-Running Timer | Free-Running Timer n input pin |
| FRCKn_R | Free-Running Timer | Relocated Free-Running Timer n input pin |
| INn | ICU | Input Capture Unit n input pin |
| INn_R | ICU | Relocated Input Capture Unit n input pin |
| INTn | External Interrupt | External Interrupt n input pin |
| INTn_R | External Interrupt | Relocated External Interrupt n input pin |
| MD | Core | Input pin for specifying the operating mode |
| NMI | External Interrupt | Non-Maskable Interrupt input pin |
| OUTn | OCU | Output Compare Unit n waveform output pin |
| OUTn_R | OCU | Relocated Output Compare Unit n waveform output pin |
| Pnn_m | GPIO | General purpose I/O pin |
| PPGn | PPG | Programmable Pulse Generator n output pin (16bit/8bit) |
| PPGn_R | PPG | Relocated Programmable Pulse Generator n output pin (16bit/8bit) |
| PPGn_B | PPG | Programmable Pulse Generator n output pin (16bit/8bit) |
| RSTX | Core | Reset input pin |
| RXn | CAN | CAN interface n RX input pin |
| SCKn | USART | USART n serial clock input/output pin |
| SCKn_R | USART | Relocated USART n serial clock input/output pin |
| SCLn | $I^2C$ | $I^2C$ interface n clock I/O input/output pin |
| SDAn | $I^2C$ | $I^2C$ interface n serial data I/O input/output pin |
| SINn | USART | USART n serial data input pin |
| SINn_R | USART | Relocated USART n serial data input pin |
| SOTn | USART | USART n serial data output pin |
| SOTn_R | USART | Relocated USART n serial data output pin |
| TINn | Reload Timer | Reload Timer n event input pin |
| TOTn | Reload Timer | Reload Timer n output pin |

| Pin name | Feature | Description |
|---|---|---|
| TTGn | PPG | Programmable Pulse Generator n trigger input pin |
| TXn | CAN | CAN interface n TX output pin |
| Vcc | Supply | Power supply pin |
| Vss | Supply | Power supply pin |
| WOT | RTC | Real Time clock output pin |
| WOT_R | RTC | Relocated Real Time clock output pin |
| X0 | Clock | Oscillator input pin |
| X0A | Clock | Subclock Oscillator input pin |
| X1 | Clock | Oscillator output pin |
| X1A | Clock | Subclock Oscillator output pin |
| ZINn | QPRC | Quadrature Position/Revolution Counter Unit n input pin |

## 5. Pin Circuit Type

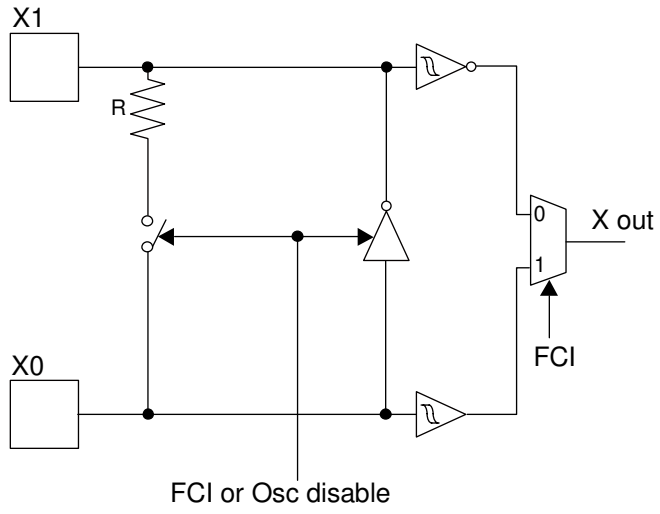
| Pin no. | I/O circuit type* | Pin name |
|---|---|---|
| 1 | Supply | Vss |
| 2 | F | C |
| 3 | M | P03_7 / INT1 / SIN1 |
| 4 | H | P13_0 / INT2 / SOT1 |
| 5 | M | P13_1 / INT3 / SCK1 |
| 6 | H | P13_2 / PPG0 / TIN0 / FRCK1 |
| 7 | H | P13_3 / PPG1 / TOT0 / WOT |
| 8 | M | P13_4 / SIN0 / INT6 |
| 9 | H | P13_5 / SOT0 / ADTG / INT7 |
| 10 | M | P13_6 / SCK0 / CKOTX0 |
| 11 | N | P04_4 / PPG3 / SDA0 |
| 12 | N | P04_5 / PPG4 / SCL0 |
| 13 | I | P06_2 / AN2 / INT5 / SIN5 |
| 14 | K | P06_3 / AN3 / FRCK0 |
| 15 | K | P06_4 / AN4 / IN0 / TTG0 / TTG4 |
| 16 | K | P06_6 / AN6 / TIN1 / IN4_R |
| 17 | K | P06_7 / AN7 / TOT1 / IN5_R |
| 18 | Supply | AVcc |
| 19 | G | AVRH |
| 20 | G | AVRL |
| 21 | Supply | AVss |
| 22 | K | P05_0 / AN8 |
| 23 | K | P05_2 / AN10 / OUT2 |
| 24 | K | P05_3 / AN11 / OUT3 |
| 25 | Supply | Vcc |
| 26 | Supply | Vss |
| 27 | K | P05_4 / AN12 / INT2_R / WOT_R |
| 28 | K | P05_6 / AN14 / TIN2 |
| 29 | K | P05_7 / AN15 / TOT2 |
| 30 | K | P08_0 / AN16 |
| 31 | K | P08_1 / AN17 |
| 32 | K | P08_2 / AN18 |
| 33 | K | P08_3 / AN19 |
| 34 | K | P08_4 / AN20 / OUT6 |
| 35 | N | P04_6 / SDA1 |
| 36 | N | P04_7 / SCL1 |
| 37 | K | P08_5 / AN21 / OUT7 |
| 38 | K | P08_6 / AN22 / PPG6_B |

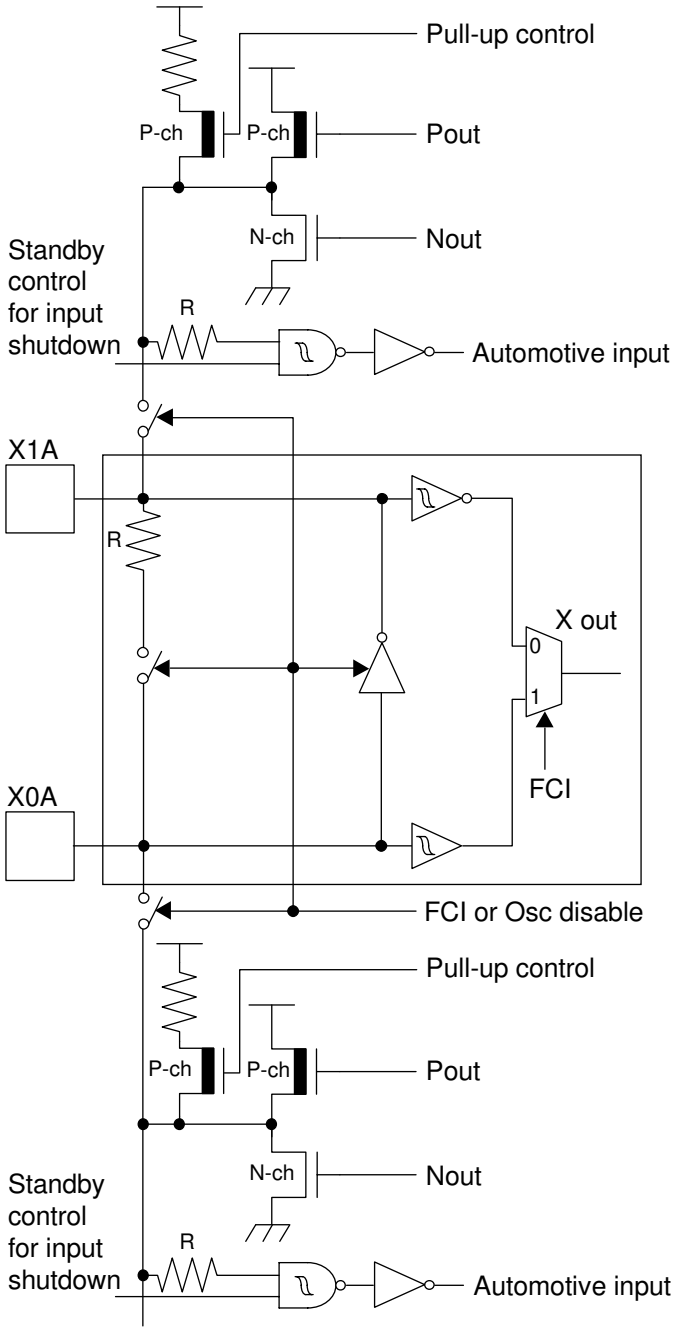
| Pin no. | I/O circuit type* | Pin name |
|---|---|---|
| 39 | K | P08_7 / AN23 / PPG7_B |
| 40 | K | P09_0 / AN24 / PPG8_R |
| 41 | K | P09_1 / AN25 / PPG9_R |
| 42 | K | P09_2 / AN26 / PPG10_R |
| 43 | K | P09_3 / AN27 / PPG11_R |
| 44 | H | P17_1 / PPG12_R |
| 45 | H | P17_2 / PPG13_R |
| 46 | I | P10_0 / SIN2 / TIN3 / AN28 / INT11 |
| 47 | H | P10_1 / SOT2 / TOT3 |
| 48 | M | P10_2 / SCK2 / PPG6 |
| 49 | H | P10_3 / PPG7 |
| 50 | Supply | Vcc |
| 51 | Supply | Vss |
| 52 | O | DEBUG I/F |
| 53 | H | P17_0 |
| 54 | C | MD |
| 55 | A | X0 |
| 56 | A | X1 |
| 57 | Supply | Vss |
| 58 | B | P04_0 / X0A |
| 59 | B | P04_1 / X1A |
| 60 | C | RSTX |
| 61 | H | P11_0 |
| 62 | H | P11_1 / PPG0_R |
| 63 | H | P11_2 / PPG1_R |
| 64 | H | P11_3 / PPG2_R |
| 65 | H | P11_4 / PPG3_R |
| 66 | H | P11_5 / PPG4_R |
| 67 | H | P11_6 / FRCK0_R / ZIN1 |
| 68 | H | P11_7 / IN0_R / AIN1 |
| 69 | H | P12_0 / IN1_R / BIN1 |
| 70 | H | P12_3 / OUT2_R |
| 71 | H | P12_7 / INT1_R |
| 72 | H | P00_0 / INT3_R / FRCK2 |
| 73 | H | P00_1 / INT4_R |
| 74 | H | P00_2 / INT5_R |
| 75 | Supply | Vcc |
| 76 | Supply | Vss |
| 77 | H | P00_3 / INT6_R / PPG8_B |

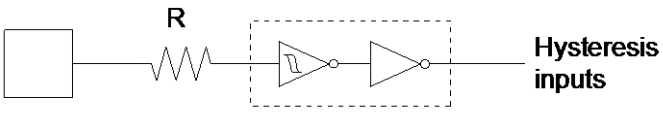
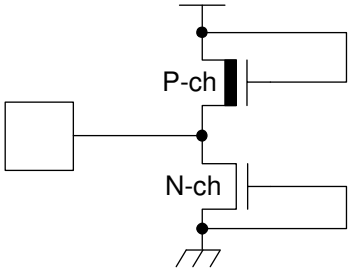
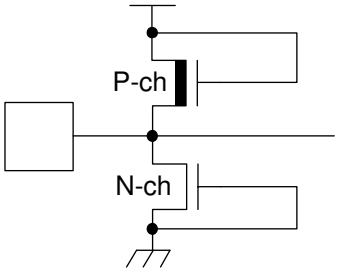
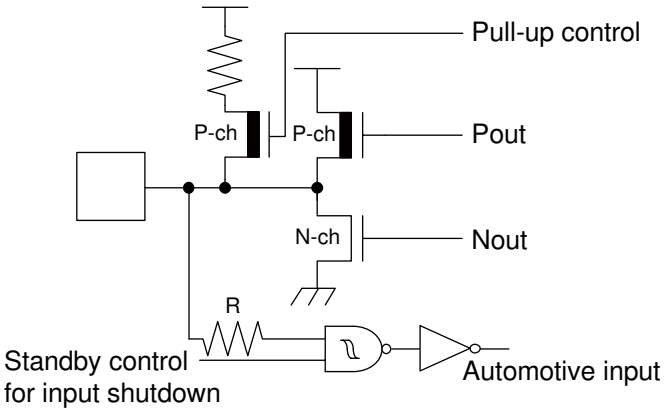
| Pin no. | I/O circuit type* | Pin name |
|---|---|---|
| 78 | H | P00_4 / INT7_R / PPG9_B |
| 79 | H | P00_5 / IN6 / TTG2 / TTG6 / PPG10_B |
| 80 | H | P00_6 / IN7 / TTG3 / TTG7 / PPG11_B |
| 81 | H | P00_7 / INT14 |
| 82 | M | P01_0 / SCK7 |
| 83 | H | P01_1 / CKOT1 / OUT0 / SOT7 |
| 84 | M | P01_2 / CKOTX1 / OUT1 / INT15 / SIN7 |
| 85 | H | P01_3 / PPG5 |
| 86 | M | P01_4 / SIN4 / INT8 |
| 87 | H | P01_5 / SOT4 |
| 88 | M | P01_6 / SCK4 / TTG12 |
| 89 | M | P01_7 / CKOTX1_R / INT9 / TTG13 / ZIN0 / SCK7_R |
| 90 | H | P02_0 / CKOT1_R / INT10 / TTG14 / AIN0 / SOT7_R |
| 91 | M | P02_2 / IN7_R / CKOT0_R / INT12 / BIN0 / SIN7_R |
| 92 | M | P02_5 / OUT0_R / INT13 / SIN5_R |
| 93 | H | P03_0 / PPG4_B |
| 94 | H | P03_1 / PPG5_B |
| 95 | H | P03_2 / PPG14_B / SOT5_R |
| 96 | M | P03_3 / PPG15_B / SCK5_R |
| 97 | M | P03_4 / RX0 / INT4 |
| 98 | H | P03_5 / TX0 |
| 99 | H | P03_6 / INT0 / NMI |
| 100 | Supply | Vcc |

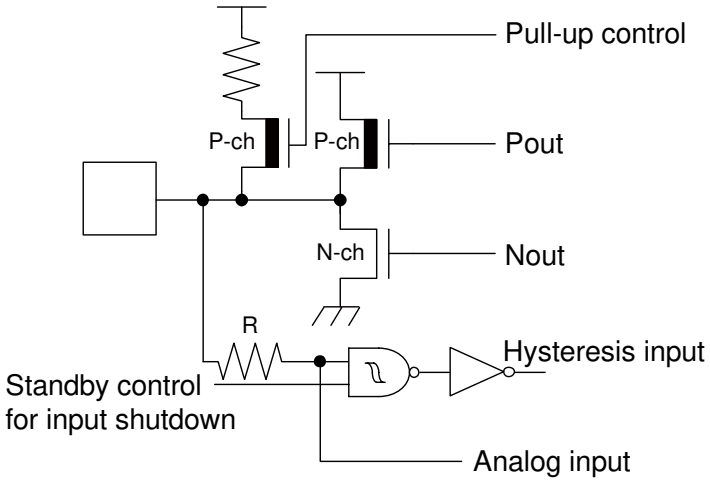
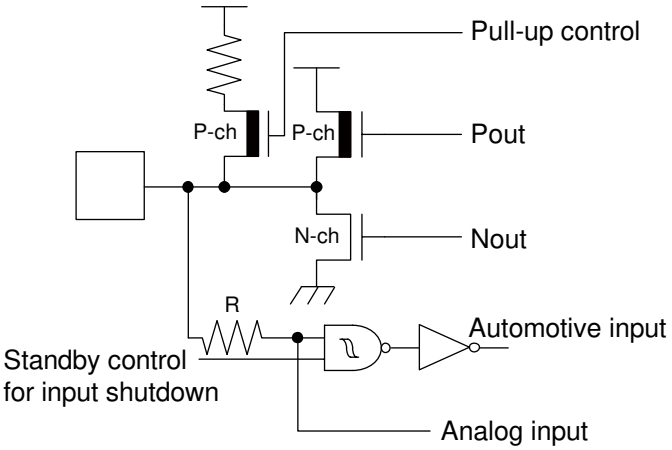
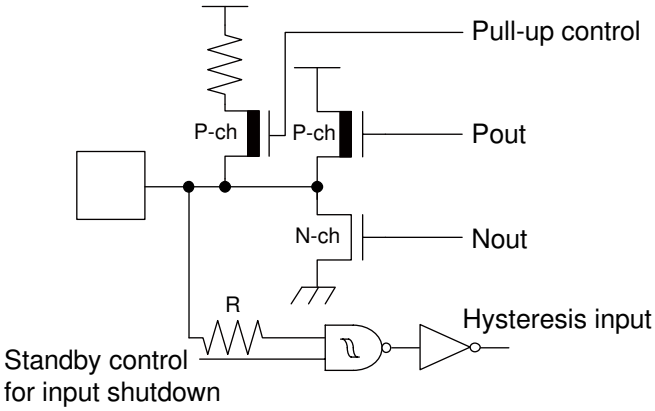
*: See “I/O Circuit Type” for details on the I/O circuit types.

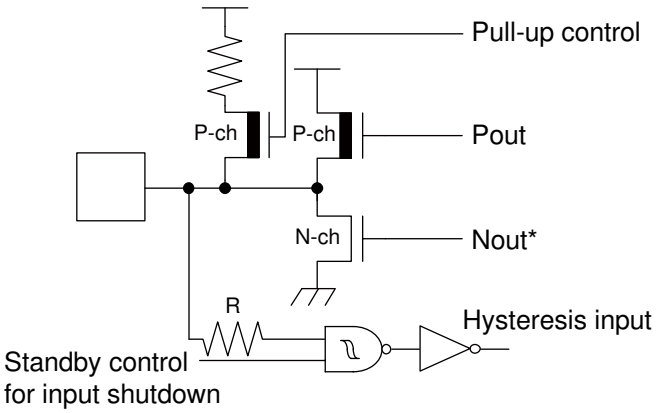
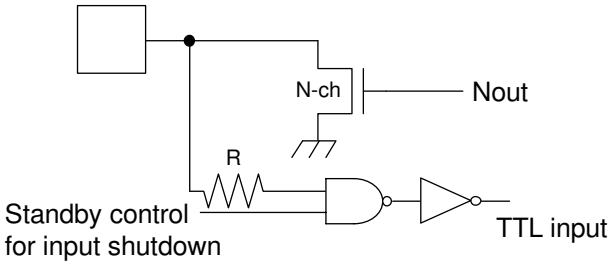
## 6. I/O Circuit Type

| Type | Circuit | Remarks |
|---|---|---|
| A |  | High-speed oscillation circuit:<br>• Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin)<br>• Feedback resistor = approx. 1.0MΩ<br>• The amplitude: 1.8V±0.15V to operate by the internal supply voltage |

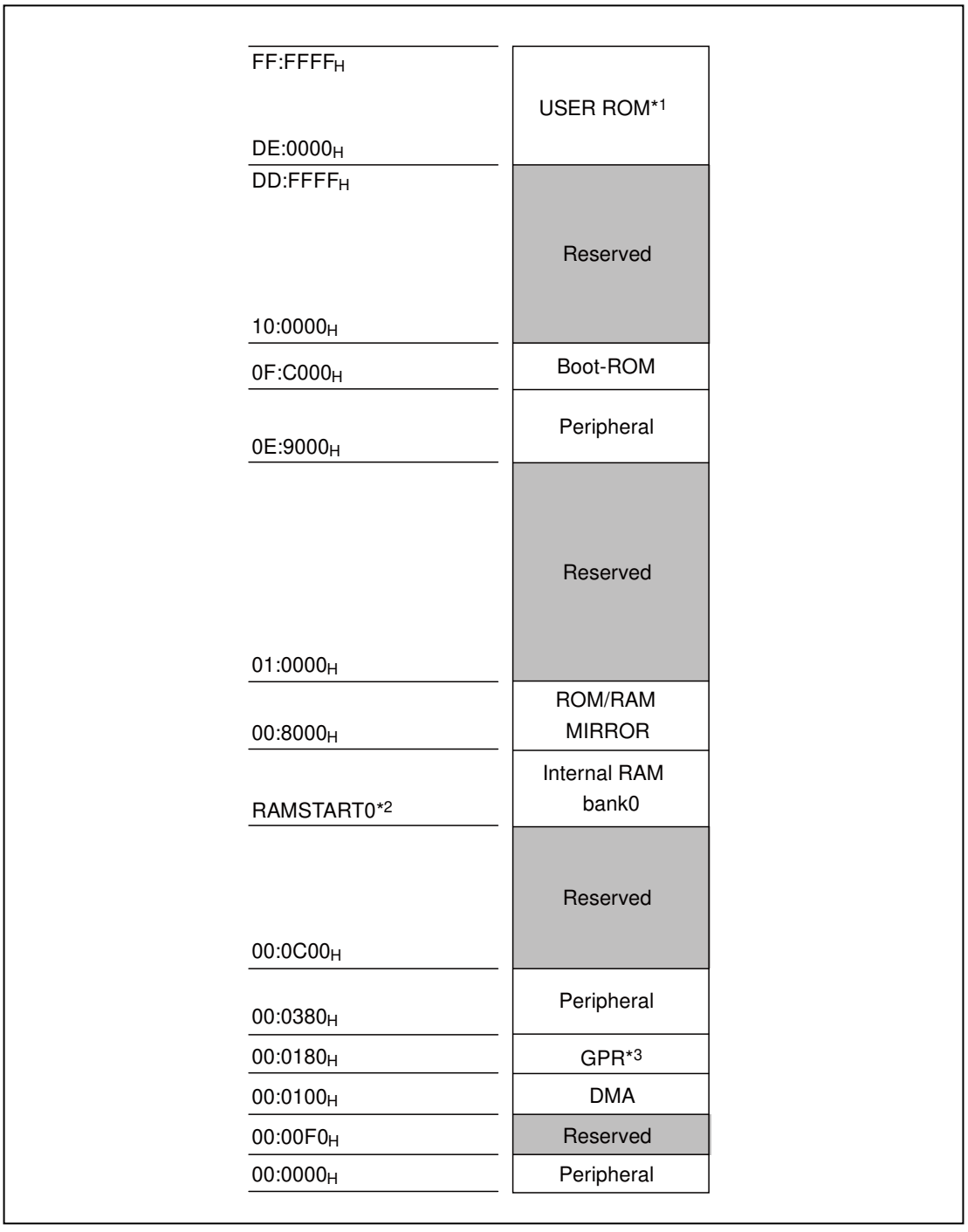
| Type | Circuit | Remarks |
|---|---|---|
| B |  | Low-speed oscillation circuit shared with GPIO functionality:<br>• Feedback resistor = approx. 5.0MΩ<br>• GPIO functionality selectable (CMOS level output ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA), Automotive input with input shutdown function and programmable pull-up resistor) |

| Type | Circuit | Remarks |
|---|---|---|
| C |  | CMOS hysteresis input pin |
| F |  | Power supply input protection circuit |
| G |  | • A/D converter ref+ (AVRH)/ ref- (AVRL) power supply input pin with protection circuit<br>• Without protection circuit against $V_{CC}$ for pins AVRH/AVRL |
| H |  | • CMOS level output ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA)<br>• Automotive input with input shutdown function<br>• Programmable pull-up resistor |

| Type | Circuit | Remarks |
|---|---|---|
| I |  | • CMOS level output ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA)<br>• CMOS hysteresis input with input shutdown function<br>• Programmable pull-up resistor<br>• Analog input |
| K |  | • CMOS level output ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA)<br>• Automotive input with input shutdown function<br>• Programmable pull-up resistor<br>• Analog input |
| M |  | • CMOS level output ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA)<br>• CMOS hysteresis input with input shutdown function<br>• Programmable pull-up resistor |

| Type | Circuit | Remarks |
|---|---|---|
| N |  | • CMOS level output ($I_{OL}$ = 3mA, $I_{OH}$ = -3mA)<br>• CMOS hysteresis input with input shutdown function<br>• Programmable pull-up resistor<br>*: N-channel transistor has slew rate control according to $I^2C$ spec, irrespective of usage. |
| O |  | • Open-drain I/O<br>• Output 25mA, Vcc = 2.7V<br>• TTL input |

## 7. Memory Map




*1: For details about USER ROM area, see “User Rom Memory Map For Flash Devices” on the following pages.

*2: For RAMSTART Addresses, see the table on the next page.

*3: Unused GPR banks can be used as RAM area.

GPR: General-Purpose Register

The DMA area is only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

## 8. RAMSTART Addresses

| Devices | Bank 0 RAM size | RAMSTART0 |
|---|---|---|
| MB96F643 | 10KB | $00:5A00_H$ |
| MB96F645 | 16KB | $00:4200_H$ |
| MB96F646 | 24KB | $00:2200_H$ |
| MB96F647 | 28KB | $00:1200_H$ |

## 9. User Rom Memory Map For Flash Devices

| CPU mode address | Flash memory mode address | MB96F643 Flash size 64.5KB + 32KB | MB96F645 Flash size 128.5KB + 32KB | MB96F646 Flash size 256.5KB + 32KB | MB96F647 Flash size 384.5KB + 32KB | |
|---|---|---|---|---|---|---|
| $FF:FFFF_H$ | $3F:FFFF_H$ | SA39 - 64KB | SA39 - 64KB | SA39 - 64KB | SA39 - 64KB | Bank A of Flash A |
| $FF:0000_H$ | $3F:0000_H$ | | | | | |
| $FE:FFFF_H$ | $3E:FFFF_H$ | Reserved | SA38 - 64KB | SA38 - 64KB | SA38 - 64KB | |
| $FE:0000_H$ | $3E:0000_H$ | | | | | |
| $FD:FFFF_H$ | $3D:FFFF_H$ | | Reserved | SA37 - 64KB | SA37 - 64KB | |
| $FD:0000_H$ | $3D:0000_H$ | | | | | |
| $FC:FFFF_H$ | $3C:FFFF_H$ | | | SA36 - 64KB | SA36 - 64KB | |
| $FC:0000_H$ | $3C:0000_H$ | | | | | |
| $FB:FFFF_H$ | $3B:FFFF_H$ | | | Reserved | SA35 - 64KB | |
| $FB:0000_H$ | $3B:0000_H$ | | | | | |
| $FA:FFFF_H$ | $3A:FFFF_H$ | | | | SA34 - 64KB | |
| $FA:0000_H$ | $3A:0000_H$ | | | | | |
| $F9:FFFF_H$ | | | | | Reserved | |
| $DF:A000_H$ | | | | | | |
| $DF:9FFF_H$ | $1F:9FFF_H$ | SA4 - 8KB | SA4 - 8KB | SA4 - 8KB | SA4 - 8KB | Bank B of Flash A |
| $DF:8000_H$ | $1F:8000_H$ | | | | | |
| $DF:7FFF_H$ | $1F:7FFF_H$ | SA3 - 8KB | SA3 - 8KB | SA3 - 8KB | SA3 - 8KB | |
| $DF:6000_H$ | $1F:6000_H$ | | | | | |
| $DF:5FFF_H$ | $1F:5FFF_H$ | SA2 - 8KB | SA2 - 8KB | SA2 - 8KB | SA2 - 8KB | |
| $DF:4000_H$ | $1F:4000_H$ | | | | | |
| $DF:3FFF_H$ | $1F:3FFF_H$ | SA1 - 8KB | SA1 - 8KB | SA1 - 8KB | SA1 - 8KB | |
| $DF:2000_H$ | $1F:2000_H$ | | | | | |
| $DF:1FFF_H$ | $1F:1FFF_H$ | SAS - 512B* | SAS - 512B* | SAS - 512B* | SAS - 512B* | Bank A of Flash A |
| $DF:0000_H$ | $1F:0000_H$ | | | | | |
| $DE:FFFF_H$ | | Reserved | Reserved | Reserved | Reserved | |
| $DE:0000_H$ | | | | | | |

*: Physical address area of SAS-512B is from DF: $0000_H$ to DF:$01FF_H$.
Others (from DF:$0200_H$ to DF:$1FFF_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF: $0000_H$ -DF: $01FF_H$.
SAS cannot be used for $E^2$PROM emulation.

## 10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

| MB96640 | | |
|---|---|---|
| **Pin Number** | **USART Number** | **Normal Function** |
| 8 | USART0 | SIN0 |
| 9 | | SOT0 |
| 10 | | SCK0 |
| 3 | USART1 | SIN1 |
| 4 | | SOT1 |
| 5 | | SCK1 |
| 46 | USART2 | SIN2 |
| 47 | | SOT2 |
| 48 | | SCK2 |
| 86 | USART4 | SIN4 |
| 87 | | SOT4 |
| 88 | | SCK4 |

## 11. Interrupt Vector Table

| Vector number | Offset in vector table | Vector name | Cleared by DMA | Index in ICR to program | Description |
|---|---|---|---|---|---|
| 0 | $3FC_H$ | CALLV0 | No | - | CALLV instruction |
| 1 | $3F8_H$ | CALLV1 | No | - | CALLV instruction |
| 2 | $3F4_H$ | CALLV2 | No | - | CALLV instruction |
| 3 | $3F0_H$ | CALLV3 | No | - | CALLV instruction |
| 4 | $3EC_H$ | CALLV4 | No | - | CALLV instruction |
| 5 | $3E8_H$ | CALLV5 | No | - | CALLV instruction |
| 6 | $3E4_H$ | CALLV6 | No | - | CALLV instruction |
| 7 | $3E0_H$ | CALLV7 | No | - | CALLV instruction |
| 8 | $3DC_H$ | RESET | No | - | Reset vector |
| 9 | $3D8_H$ | INT9 | No | - | INT9 instruction |
| 10 | $3D4_H$ | EXCEPTION | No | - | Undefined instruction execution |
| 11 | $3D0_H$ | NMI | No | - | Non-Maskable Interrupt |
| 12 | $3CC_H$ | DLY | No | 12 | Delayed Interrupt |
| 13 | $3C8_H$ | RC_TIMER | No | 13 | RC Clock Timer |
| 14 | $3C4_H$ | MC_TIMER | No | 14 | Main Clock Timer |
| 15 | $3C0_H$ | SC_TIMER | No | 15 | Sub Clock Timer |
| 16 | $3BC_H$ | LVDI | No | 16 | Low Voltage Detector |
| 17 | $3B8_H$ | EXTINT0 | Yes | 17 | External Interrupt 0 |
| 18 | $3B4_H$ | EXTINT1 | Yes | 18 | External Interrupt 1 |
| 19 | $3B0_H$ | EXTINT2 | Yes | 19 | External Interrupt 2 |
| 20 | $3AC_H$ | EXTINT3 | Yes | 20 | External Interrupt 3 |
| 21 | $3A8_H$ | EXTINT4 | Yes | 21 | External Interrupt 4 |
| 22 | $3A4_H$ | EXTINT5 | Yes | 22 | External Interrupt 5 |
| 23 | $3A0_H$ | EXTINT6 | Yes | 23 | External Interrupt 6 |
| 24 | $39C_H$ | EXTINT7 | Yes | 24 | External Interrupt 7 |
| 25 | $398_H$ | EXTINT8 | Yes | 25 | External Interrupt 8 |
| 26 | $394_H$ | EXTINT9 | Yes | 26 | External Interrupt 9 |
| 27 | $390_H$ | EXTINT10 | Yes | 27 | External Interrupt 10 |
| 28 | $38C_H$ | EXTINT11 | Yes | 28 | External Interrupt 11 |
| 29 | $388_H$ | EXTINT12 | Yes | 29 | External Interrupt 12 |
| 30 | $384_H$ | EXTINT13 | Yes | 30 | External Interrupt 13 |
| 31 | $380_H$ | EXTINT14 | Yes | 31 | External Interrupt 14 |
| 32 | $37C_H$ | EXTINT15 | Yes | 32 | External Interrupt 15 |
| 33 | $378_H$ | CAN0 | No | 33 | CAN Controller 0 |
| 34 | $374_H$ | - | - | 34 | Reserved |
| 35 | $370_H$ | - | - | 35 | Reserved |
| 36 | $36C_H$ | - | - | 36 | Reserved |
| 37 | $368_H$ | - | - | 37 | Reserved |
| 38 | $364_H$ | PPG0 | Yes | 38 | Programmable Pulse Generator 0 |
| 39 | $360_H$ | PPG1 | Yes | 39 | Programmable Pulse Generator 1 |

| Vector number | Offset in vector table | Vector name | Cleared by DMA | Index in ICR to program | Description |
|---|---|---|---|---|---|
| 40 | $35C_H$ | PPG2 | Yes | 40 | Programmable Pulse Generator 2 |
| 41 | $358_H$ | PPG3 | Yes | 41 | Programmable Pulse Generator 3 |
| 42 | $354_H$ | PPG4 | Yes | 42 | Programmable Pulse Generator 4 |
| 43 | $350_H$ | PPG5 | Yes | 43 | Programmable Pulse Generator 5 |
| 44 | $34C_H$ | PPG6 | Yes | 44 | Programmable Pulse Generator 6 |
| 45 | $348_H$ | PPG7 | Yes | 45 | Programmable Pulse Generator 7 |
| 46 | $344_H$ | PPG8 | Yes | 46 | Programmable Pulse Generator 8 |
| 47 | $340_H$ | PPG9 | Yes | 47 | Programmable Pulse Generator 9 |
| 48 | $33C_H$ | PPG10 | Yes | 48 | Programmable Pulse Generator 10 |
| 49 | $338_H$ | PPG11 | Yes | 49 | Programmable Pulse Generator 11 |
| 50 | $334_H$ | PPG12 | Yes | 50 | Programmable Pulse Generator 12 |
| 51 | $330_H$ | PPG13 | Yes | 51 | Programmable Pulse Generator 13 |
| 52 | $32C_H$ | PPG14 | Yes | 52 | Programmable Pulse Generator 14 |
| 53 | $328_H$ | PPG15 | Yes | 53 | Programmable Pulse Generator 15 |
| 54 | $324_H$ | - | - | 54 | Reserved |
| 55 | $320_H$ | - | - | 55 | Reserved |
| 56 | $31C_H$ | - | - | 56 | Reserved |
| 57 | $318_H$ | - | - | 57 | Reserved |
| 58 | $314_H$ | RLT0 | Yes | 58 | Reload Timer 0 |
| 59 | $310_H$ | RLT1 | Yes | 59 | Reload Timer 1 |
| 60 | $30C_H$ | RLT2 | Yes | 60 | Reload Timer 2 |
| 61 | $308_H$ | RLT3 | Yes | 61 | Reload Timer 3 |
| 62 | $304_H$ | - | - | 62 | Reserved |
| 63 | $300_H$ | - | - | 63 | Reserved |
| 64 | $2FC_H$ | RLT6 | Yes | 64 | Reload Timer 6 |
| 65 | $2F8_H$ | ICU0 | Yes | 65 | Input Capture Unit 0 |
| 66 | $2F4_H$ | ICU1 | Yes | 66 | Input Capture Unit 1 |
| 67 | $2F0_H$ | - | - | 67 | Reserved |
| 68 | $2EC_H$ | - | - | 68 | Reserved |
| 69 | $2E8_H$ | ICU4 | Yes | 69 | Input Capture Unit 4 |
| 70 | $2E4_H$ | ICU5 | Yes | 70 | Input Capture Unit 5 |
| 71 | $2E0_H$ | ICU6 | Yes | 71 | Input Capture Unit 6 |
| 72 | $2DC_H$ | ICU7 | Yes | 72 | Input Capture Unit 7 |
| 73 | $2D8_H$ | - | - | 73 | Reserved |
| 74 | $2D4_H$ | ICU9 | Yes | 74 | Input Capture Unit 9 |
| 75 | $2D0_H$ | - | - | 75 | Reserved |
| 76 | $2CC_H$ | - | - | 76 | Reserved |
| 77 | $2C8_H$ | OCU0 | Yes | 77 | Output Compare Unit 0 |
| 78 | $2C4_H$ | OCU1 | Yes | 78 | Output Compare Unit 1 |
| 79 | $2C0_H$ | OCU2 | Yes | 79 | Output Compare Unit 2 |
| 80 | $2BC_H$ | OCU3 | Yes | 80 | Output Compare Unit 3 |
| 81 | $2B8_H$ | OCU4 | Yes | 81 | Output Compare Unit 4 |

| Vector number | Offset in vector table | Vector name | Cleared by DMA | Index in ICR to program | Description |
|---|---|---|---|---|---|
| 82 | $2B4_H$ | - | - | 82 | Reserved |
| 83 | $2B0_H$ | OCU6 | Yes | 83 | Output Compare Unit 6 |
| 84 | $2AC_H$ | OCU7 | Yes | 84 | Output Compare Unit 7 |
| 85 | $2A8_H$ | - | - | 85 | Reserved |
| 86 | $2A4_H$ | - | - | 86 | Reserved |
| 87 | $2A0_H$ | - | - | 87 | Reserved |
| 88 | $29C_H$ | - | - | 88 | Reserved |
| 89 | $298_H$ | FRT0 | Yes | 89 | Free-Running Timer 0 |
| 90 | $294_H$ | FRT1 | Yes | 90 | Free-Running Timer 1 |
| 91 | $290_H$ | FRT2 | Yes | 91 | Free-Running Timer 2 |
| 92 | $28C_H$ | - | - | 92 | Reserved |
| 93 | $288_H$ | RTC0 | No | 93 | Real Time Clock |
| 94 | $284_H$ | CAL0 | No | 94 | Clock Calibration Unit |
| 95 | $280_H$ | - | - | 95 | Reserved |
| 96 | $27C_H$ | IIC0 | Yes | 96 | $I^2C$ interface 0 |
| 97 | $278_H$ | IIC1 | Yes | 97 | $I^2C$ interface 1 |
| 98 | $274_H$ | ADC0 | Yes | 98 | A/D Converter 0 |
| 99 | $270_H$ | - | - | 99 | Reserved |
| 100 | $26C_H$ | - | - | 100 | Reserved |
| 101 | $268_H$ | LINR0 | Yes | 101 | LIN USART 0 RX |
| 102 | $264_H$ | LINT0 | Yes | 102 | LIN USART 0 TX |
| 103 | $260_H$ | LINR1 | Yes | 103 | LIN USART 1 RX |
| 104 | $25C_H$ | LINT1 | Yes | 104 | LIN USART 1 TX |
| 105 | $258_H$ | LINR2 | Yes | 105 | LIN USART 2 RX |
| 106 | $254_H$ | LINT2 | Yes | 106 | LIN USART 2 TX |
| 107 | $250_H$ | - | - | 107 | Reserved |
| 108 | $24C_H$ | - | - | 108 | Reserved |
| 109 | $248_H$ | LINR4 | Yes | 109 | LIN USART 4 RX |
| 110 | $244_H$ | LINT4 | Yes | 110 | LIN USART 4 TX |
| 111 | $240_H$ | LINR5 | Yes | 111 | LIN USART 5 RX |
| 112 | $23C_H$ | LINT5 | Yes | 112 | LIN USART 5 TX |
| 113 | $238_H$ | - | - | 113 | Reserved |
| 114 | $234_H$ | - | - | 114 | Reserved |
| 115 | $230_H$ | LINR7 | Yes | 115 | LIN USART 7 RX |
| 116 | $22C_H$ | LINT7 | Yes | 116 | LIN USART 7 TX |
| 117 | $228_H$ | - | - | 117 | Reserved |
| 118 | $224_H$ | - | - | 118 | Reserved |
| 119 | $220_H$ | - | - | 119 | Reserved |
| 120 | $21C_H$ | - | - | 120 | Reserved |

| Vector number | Offset in vector table | Vector name | Cleared by DMA | Index in ICR to program | Description |
|---|---|---|---|---|---|
| 121 | $218_H$ | - | - | 121 | Reserved |
| 122 | $214_H$ | - | - | 122 | Reserved |
| 123 | $210_H$ | - | - | 123 | Reserved |
| 124 | $20C_H$ | - | - | 124 | Reserved |
| 125 | $208_H$ | - | - | 125 | Reserved |
| 126 | $204_H$ | - | - | 126 | Reserved |
| 127 | $200_H$ | - | - | 127 | Reserved |
| 128 | $1FC_H$ | - | - | 128 | Reserved |
| 129 | $1F8_H$ | - | - | 129 | Reserved |
| 130 | $1F4_H$ | - | - | 130 | Reserved |
| 131 | $1F0_H$ | - | - | 131 | Reserved |
| 132 | $1EC_H$ | - | - | 132 | Reserved |
| 133 | $1E8_H$ | FLASHA | Yes | 133 | Flash memory A interrupt |
| 134 | $1E4_H$ | - | - | 134 | Reserved |
| 135 | $1E0_H$ | - | - | 135 | Reserved |
| 136 | $1DC_H$ | - | - | 136 | Reserved |
| 137 | $1D8_H$ | QPRC0 | Yes | 137 | Quad Position/Revolution counter 0 |
| 138 | $1D4_H$ | QPRC1 | Yes | 138 | Quad Position/Revolution counter 1 |
| 139 | $1D0_H$ | ADCRC0 | No | 139 | A/D Converter 0 - Range Comparator |
| 140 | $1CC_H$ | - | - | 140 | Reserved |
| 141 | $1C8_H$ | - | - | 141 | Reserved |
| 142 | $1C4_H$ | - | - | 142 | Reserved |
| 143 | $1C0_H$ | - | - | 143 | Reserved |