Isolated, Synchronous Forward Controller with Active Clamp and *i*Coupler

Data Sheet

ADP1074

FEATURES

- Current mode controller for active clamp forward topology
- Integrated 5 kV (wide body SOIC package) or 3.0 kV (LGA package) rated dielectric isolation voltage with Analog Devices, Inc., patented *i*Coupler technology
- Wide voltage supply range
  - Primary V_{IN}: up to 60 V
  - Secondary V_{DD2}: up to 36 V
- Integrated 1 A primary side MOSFET driver for power switch and active clamp reset switch
- Integrated 1 A secondary side MOSFET drivers for synchronous rectification
- Integrated error amplifier and <1% accurate reference voltage
- Programmable slope compensation
- Programmable frequency range: 50 kHz to 600 kHz typical
- Frequency synchronization
- Programmable maximum duty cycle limit
- Programmable soft start
- Smooth soft start from precharged load
- Programmable dead time
- Power saving light load mode using MODE pin
- Protection features such as short circuit, output overvoltage, and overtemperature protection
  - Cycle-by-cycle input overcurrent protection
- Precision enable UVLO with hysteresis
- PGOOD pin for system flagging
- Tracking function from secondary side
- Remote (secondary side) shutdown/reset function
- Safety and regulatory approvals (pending)
  - UL recognition
    - 5000 V rms for 1 minute per UL 1577 (for wide body SOIC package)
    - 3000 V rms for 1 minute per UL 1577 (for LGA package)
  - CSA component acceptance notice 5A
  - VDE certificate of conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 849 V peak (for wide body SOIC package)
    - V_{IORM} = 560 V peak (for LGA package)
  - CQC certification per GB4943.1-2011
- Available in 24-lead SOIC_W package and 24-terminal LGA package

APPLICATIONS

- Isolated dc-to-dc power conversion
- Intermediate bus voltage generation
- Telecom, industrial
- Base station and antenna RF power
- Small cell
  - PoE powered device
- Enterprise switches/routers
- Core/edge/metro/optical routing
- Power modules

SIMPLIFIED BLOCK DIAGRAM

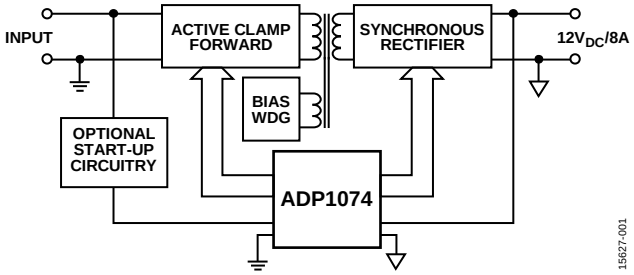

Figure 1.

GENERAL DESCRIPTION

The ADP1074 is a current mode, fixed frequency, active clamp, synchronous forward controller designed for isolated dc to dc power supplies. Analog Devices proprietary *i*Couplers® are integrated in the ADP1074 to eliminate the bulky signal transformers and optocouplers that transmit signals over the isolation boundary. Integrating the *i*Couplers reduces system design complexity, cost, and component count and improves overall system reliability. With the integrated isolators and metal-oxide semiconductor field effect transistor (MOSFET) drivers on both the primary and the secondary side, the ADP1074 offers a compact system level design and yields a higher efficiency than a non-synchronous forward converter at heavy loads.

The primary side pins provide functions for programming the switching frequency, maximum duty cycle, external frequency synchronization, and slope compensation.

The secondary side pins provide functions for differential output voltage sensing, overvoltage, power good, tracking, and programmable light load mode setting.

The feedback signal and timing of synchronous rectifier pulse-width modulations (PWMs) are transmitted from primary to secondary or from secondary to primary sides through the *i*Couplers using a proprietary transmission scheme.

The ADP1074 also offers features such as input current protection, undervoltage lockout (UVLO), precision enable with adjustable hysteresis, overtemperature protection (OTP), and power saving light load mode (LLM).

Rev. A

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10/2017—Revision 0: Initial Version

SPECIFICATIONS

VIN = 24 V, VDD2 = 12 V, T_J = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY (PRIMARY)						
Supply Voltage	V_{IN}	4.7 µF capacitor from VIN to PGND1, 1 µF capacitor from VREG1 to PGND1	4.7	24	60	V
Quiescent Supply Current	I_{VIN}	VIN > VIN UVLO, NGATE and PGATE unloaded				
		At 100 kHz		5.3		mA
		At 300 kHz		5.8		mA
		At 600 kHz		6.8		mA
		VIN > VIN UVLO, NGATE and PGATE loaded with 2.2 nF and 410 pF, respectively				
		At 100 kHz		7.5		mA
		At 300 kHz		12		mA
		At 600 kHz		19.5		mA
VIN Shutdown Current		EN pin voltage (V_{EN}) < 1.2 V, VREG1 = 0 V, VIN = 60 V			55	µA
(VIN + VREG1) Start-Up Current	$I_{VIN\_STARTUP}$	V_{EN} < 1.2 V, VREG1 = 12 V, VIN = 12 V			160	µA
VIN UVLO		VIN rising			4.7	V
		VIN falling	4.0			V
UVLO Hysteresis				0.19		V
Time from EN High to PGATE Output Switching		V_{EN} > 1.2 V, 1 µF capacitor on VREG1			1	ms
Time from EN Low to SR1/SR2 Output Stops Switching		V_{EN} < 1.0 V, 1 µF capacitor on VREG1			1	µs
SUPPLY (SECONDARY)						
Supply Voltage	V_{DD2}	4.7 µF capacitor from VDD2 to PGND2, 1 µF capacitor from VREG2 to PGND2	4.5	12	36	V
Quiescent Supply Current	I_{DD}	SR1 and SR2 unloaded				
		At 100 kHz		6.5		mA
		At 300 kHz		6.7		mA
		At 600 kHz		7		mA
	I_{DD2}	SR1 and SR2 loaded with 2.2 nF				
		At 100 kHz		8.3		mA
		At 300 kHz		12		mA
		At 600 kHz		18		mA
VDD2 UVLO Threshold		VDD2 rising			3.55	V
		VDD2 falling	3.0			V
UVLO Hysteresis				0.145		V
Secondary UVLO Hiccup Time				200		ms
OSCILLATOR						
Switching Frequency (f_S)		RT resistance (R_{RT}) = 480 kΩ (±1%)	50 − 10%	50	50 + 10%	kHz
		R_{RT} = 240 kΩ (±1%)	100 − 10%	100	100 + 10%	kHz
		R_{RT} = 120 kΩ (±1%)	200 − 10%	200	200 + 10%	kHz
		R_{RT} = 80 kΩ (±1%)	300 − 10%	300	300 + 10%	kHz
		R_{RT} = 60 kΩ (±1%)	400 − 10%	400	400 + 10%	kHz
		R_{RT} = 40 kΩ (±1%)	600 − 10%	600	600 + 10%	kHz
VREG1 PIN						
VREG1 Voltage Clamp		VREG1 current (I_{VREG1}) = 3 mA, V_{EN} < 1.2 V	13.5	14.3	15.2	V
VREG1 Clamp Series Resistance		VREG1 forced current of 5 mA and 15 mA		16		Ω

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
GATE DRIVERS (PRIMARY)						
NGATE and PGATE High Voltage		I_{VREG1} = 20 mA, VIN > 9 V	7.8	8	8.2	V
Gate Short-Circuit Peak Current[1]		8 V on VREG1		1.0		A
Rise Time		10% to 90%				
NGATE		C_{NGATE} = 2.2 nF		18		ns
PGATE		C_{PGATE} = 410 pF		8		ns
Fall Time		90% to 10%				
NGATE		C_{NGATE} = 2.2 nF		16		ns
PGATE		C_{PGATE} = 410 pF		7		ns
Source Resistance	R_{ON_SOURCE}	Source 100 mA				
NGATE				4		Ω
PGATE				6.5		Ω
Sink Resistance	R_{ON_SINK}	Sink 100 mA				
NGATE				3		Ω
PGATE				3.5		Ω
NGATE Maximum Duty Cycle	D_{MAX}	Divider bottom resistor (R_{BOT}) = 0 Ω	45	50	55	%
		Divider top resistor (R_{TOP}) = R_{BOT}, 1% resistors		75		%
NGATE Minimum On Time		Includes propagation delay and CS comparator blanking time		170		ns
PGATE Source Resistance	R_{ON_SOURCE}	Source 100 mA		6.5		Ω
PGATE Sink Resistance	R_{ON_SINK}	Sink 100 mA		3.5		Ω
SRx DRIVERS (SECONDARY)						
SR1 and SR2 High Voltage		I_{VREG2} = 15 mA, VDD2 > 5.5 V	4.9	5	5.1	V
Gate Short-Circuit Peak Current[1]		5 V on VREG2		1.0		A
SRx Time		C_{SRx} = 2.2 nF				
Rise		10% to 90%		14		ns
Fall		90% to 10%		11		ns
Minimum On		Includes blanking time		230		ns
SRx Resistance						
Source	$R_{ON\_SR\_SOURCE}$	Source 100 mA		3.5		Ω
Sink	$R_{ON\_SR\_SINK}$	Sink 100 mA		2		Ω
DELAYS						
Gate Delay (SR1 Rising to NGATE Rising)				35		ns
Delay Between NGATE Falling Edge and SR1 Falling Edge	*i*Coupler delay			21		ns
SR DEAD TIME (PGATE RISING TO SR2 FALLING)		Resistor (±5%) at NGATE				
		Dead time resistor (R_{DT}) = 10 kΩ		154		ns
		R_{DT} = 22 kΩ		109		ns
		R_{DT} = 47 kΩ		72		ns
		R_{DT} is open		42		ns
SR1 and SR2 Dead Time		Dead time between SR1 and SR2		25		ns
CURRENT-LIMIT SENSE (PRIMARY)						
CS Limit Threshold	V_{CS_LIM}	Over current sense limit threshold		120		mV
CS Leading Edge Blanking Time				150		ns
Current Source di/dt for Slope Compensation		Switching period (t_S) = 1/f_S		20		µA per t_S

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Overcurrent Protection (OCP) Comparator Delay				40		ns
Time in OCP Before Entering Hiccup Mode				1.5		ms
OCP Hiccup Time		When FB > 0.3 V and if VDD2 is powered from auxiliary winding on secondary side.		40		ms
FB PIN AND ERROR AMPLIFIER						
Feedback Accuracy Voltage	V_{FB}	T_J = −40°C to +85°C	1.2 − 0.85%	+1.2	1.2 + 0.85%	V
		T_J = −40°C to +125°C	1.2 − 1.25%	+1.2	1.2 + 1.25%	V
Temperature Coefficient					76	ppm/°C
FB Input Bias Current			−100	+1	+100	nA
Transconductance	gm		230	250	270	µA/V
Output Current Clamp						
Minimum				−57		µA
Maximum				43		µA
COMP Clamp Voltage						
Minimum		20 µA sinking current from COMP pin		0.7		V
Maximum		20 µA sourcing current to COMP pin		2.52		V
Open-Loop Gain				80		dB
Output Shunt Resistance				5		GΩ
Gain Bandwidth Product				1		MHz
PRECISION ENABLE THRESHOLD						
EN Threshold	V_{EN}	EN rising	1.14	1.2	1.26	V
EN Hysteresis		V_{EN} < 1.2 V		4		µA
		V_{EN} > 1.2 V		1		µA
EN Hysteresis Current				3		µA
MODE PIN						
Light Load Mode Current Source		Connect a resistor from MODE to AGND2	6	6.5	7	µA
Hysteresis			24	40	60	mV
TEMPERATURE						
Thermal Shutdown				155		°C
Hysteresis				−15		°C
SOFT START SS1 AND SS2 PINS						
Primary Side SS1 Current Source		During soft start only		9.1		µA
Secondary Side SS2 Current Source		During soft start only, post handover		20		µA
SS2 Discharging Current		During a fault condition or soft stop		30		µA
SYNC PIN						
Synchronization Range			100		600	kHz
Input Pulse Width			100			ns
Number of Cycles Before Synchronization				7		Cycles
Input Voltage						
Low					0.4	V
High			3			V
Leakage Current					1	µA
*i*COUPLER DELAY						
COMP Signal Delay Through *i*Coupler				600		ns

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FB, OVP, AND $\overline{\text{PGOOD}}$ THRESHOLDS		Overvoltage (OV) threshold for $\overline{\text{PGOOD}}$ to toggle for FB and OVP pin	1.3	1.36	1.42	V
FB Pin OV Hysteresis				36		mV
OVP Pin Hysteresis				36		mV
FB Pin UV Threshold		Undervoltage (UV) threshold for $\overline{\text{PGOOD}}$ to toggle	1.04	1.11	1.16	V
FB Pin UV Hysteresis				36		mV
OVP Comparator Delay (Includes *i*Coupler Delay)				320		ns
Time from Fault Condition to $\overline{\text{PGOOD}}$ Toggling		OVP pin fault to $\overline{\text{PGOOD}}$ toggling		90		ns
		FB pin OV/UV to $\overline{\text{PGOOD}}$ toggling		5		µs
OVP Pin Leakage Current					1	µA
$\overline{\text{PGOOD}}$ Pin Leakage Current					1	µA
OVP Hiccup		Time in OVP before entering OVP hiccup mode		200		µs
		Hiccup time triggered by OVP event		200		ms

[1] Short-circuit duration less than 1 µs. Average power must conform to the limit shown in the Absolute Maximum Ratings section.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
WIDE BODY SOIC						
*i*Coupler						
Rated Dielectric Insulation Voltage		1 minute duration		5		kV
Minimum External Air Gap (Clearance)		Measured from input terminals to output terminals, shortest distance through air	7.6			mm
Minimum External Air Gap (Creepage)		Measured from input terminals to output terminals, shortest distance path along body	7.6			mm
Minimum Internal Gap (Internal Clearance)		Insulation distance through insulation		0.030		mm
Tracking Resistance (Comparative Tracking Index)	CTI			>400		V
Isolation Group		Material Group II (DIN VDE 0110, 1/89, Table 1)				
LAND GRID ARRAY (LGA)						
*i*Coupler						
Rated Dielectric Insulation Voltage		1 minute duration		2.5		kV
Minimum External Air Gap (Clearance)		Measured from input terminals to output terminals, shortest distance through air	4			mm
Minimum External Air Gap (Creepage)		Measured from input terminals to output terminals, shortest distance path along body	4			mm
Minimum Internal Gap (Internal Clearance)		Insulation distance through insulation		0.030		mm
Tracking Resistance (Comparative Tracking Index)	CTI			>400		V
Isolation Group		Material Group I (DIN VDE 0110, 1/89, Table 1)				

REGULATORY INFORMATION

See Table 3, Table 4, and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table 3. Regulatory Information for Wide Body SOIC Package

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
Recognized Under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]	Certified by CQC11-471543-2012, GB4943.1-2011:
Single Protection, 5000 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2 and IEC62368:	Reinforced insulation, maximum working insulation voltage (V_{IORM}) = 849 V peak, highest allowable overvoltage (V_{IOTM}) = 8000 V peak	Basic insulation at 780 V rms (1103 V peak)
	Basic insulation at 780 V rms (1103 V peak)		Reinforced insulation at 389 V rms (552 V peak), tropical climate, altitude ≤5000 meters
	Reinforced insulation at 390 V rms (552 V peak)		
	IEC 60601-1 Edition 3.1:		
	Basic insulation (1 means of patient protection (1 MOPP)), 490 V rms (686 V peak)		
	Reinforced insulation (2 MOPP), 238 V rms (325 V peak)		
	CSA 61010-1-12 and IEC 61010-1 third edition:		
	Basic insulation at 300 V rms mains, 780 V secondary (1103 V peak)		
File (pending)	File (pending)	File (pending)	File (pending)

[1] In accordance with UL 1577, each product is proof tested by applying an insulation test voltage ≥6000 V rms for 1 sec.
[2] In accordance with DIN V VDE V 0884-10, each product is proof tested by applying an insulation test voltage ≥1592 V peak for 1 sec (partial discharge detection limit = 5 pC). Note that the asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

Table 4. Regulatory Information for LGA Package

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
Recognized Under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]	Certified by CQC11-471543-2012, GB4943.1-2011:
Single Protection, 3000V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2 and IEC62368:	Reinforced insulation, V_{IORM} = 565 V peak, V_{IOTM} = 4242 V peak impulse voltage = 4242 V peak	Basic insulation at 400 V rms (565 V peak)
	Basic insulation at 400 V rms (565 V peak)		Reinforced insulation at 200 V rms (283 V peak), tropical climate, altitude ≤5000 meters
	Reinforced insulation at 200 V rms (283 V peak)		
	IEC 60601-1 Edition 3.1:		
	Basic insulation (1 means of patient protection (1 MOPP)), 250 V rms (354 V peak)		
	CSA 61010-1-12 and IEC 61010-1 third edition:		
	Basic insulation at 300 V rms mains, 400 V secondary (565 V peak)		
File (pending)	File (pending)	File (pending)	File (pending)

[1] In accordance with UL 1577, each product is proof tested by applying an insulation test voltage ≥3000 V rms for 1 sec.
[2] In accordance with DIN V VDE V 0884-10, each product is proof tested by applying an insulation test voltage ≥1059 V peak for 1 sec (partial discharge detection limit = 5 pC). Note that the asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation within the safety limit data only. Maintenance of the safety data is ensured by protective circuits. Note that the asterisk (*) marked on the package denotes DIN V VDE V 0884-10 approval for a 560 V peak working voltage.

Table 5. DIN V VDE V 0884-10 (VDE V 0884-10) Insulation Characteristics for Wide Body SOIC Package

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	565	V_{PEAK}
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	V_{PR}	1060	V_{PEAK}
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC	V_{PR}		
After Environmental Tests Subgroup 1			905	V_{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		679	V_{PEAK}
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 seconds	V_{IOTM}	7071	V_{PEAK}
Surge Isolation Voltage Reinforced	V_{PEAK} = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6000	V_{PEAK}
Safety-Limiting Values	Maximum value allowed in the event of a failure; see Figure 2			
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	160	mA
Side 2 Current		I_{S2}	170	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

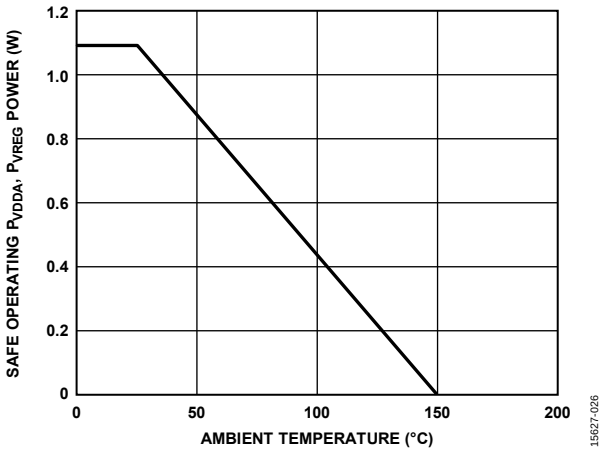

Figure 2. Thermal Derative Curve, Dependence of Safety Limiting Values with Ambient Temperature per DINV VDE V 0884-10

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation within the safety limit data only. Maintenance of the safety data is ensured by protective circuits. Note that the asterisk (*) marked on the package denotes DIN V VDE V 0884-10 approval for a 560 V peak working voltage.

Table 6. DIN V VDE V 0884-10 (VDE V 0884-10) Insulation Characteristics for LGA Package

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	565	V_{PEAK}
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	V_{PR}	1060	V_{PEAK}
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC	V_{PR}		
After Environmental Tests Subgroup 1			905	V_{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		679	V_{PEAK}
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 seconds	V_{TR}	4242	V_{PEAK}
Surge Isolation Voltage Reinforced	V_{PEAK} = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6000	V_{PEAK}
Safety-Limiting Values	Maximum value allowed in the event of a failure; see Figure 3			
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	160	mA
Side 2 Current		I_{S2}	170	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

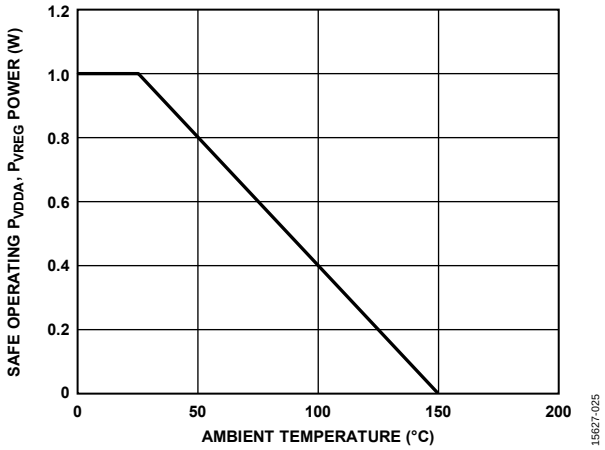

Figure 3. Thermal Derative Curve, Dependence of Safety Limiting Values with Ambient Temperature per DINV VDE V 0884-10

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
VIN, EN	−0.3 V to +66 V
VDD2	−0.3 V to +42 V
VREG1	−0.3 V to +16 V
VREG2	−0.3 V to +6 V
NGATE, PGATE	−0.3 V to +16 V
RT, CS, SYNC, SS1, SS2, $\overline{\text{PGOOD}}$, FB, COMP, OVP, MODE, DMAX, SR1, SR2	−0.3 V to +6 V
AGND1, PGND1, AGND2, PGND2	±0.3 V
Common-Mode Transients[1]	±25 kV/µs
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS Compliant Assemblies (20 sec to 40 sec)	260°C
Electrostatic Discharge (ESD)	
Charged Device Model (CDM)	±1250 V
Human Body Model (HBM)	±2 kV

[1] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 8. Thermal Resistance[1]

Package Type	θ_{JA}	θ_{JC}	Unit
RW-24 (Wide Body SOIC)	65.4	43.8	°C/W
CC-24-6 (LGA)	62.1	43	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board. See JEDEC JESD-51.

Table 9. Maximum Continuous Working Voltage, Wide Body SOIC[1]

Waveform	Maximum Voltage (V_{PEAK})	Constraint
AC Voltage		
Bipolar	565	50-year minimum lifetime
Unipolar	1131	50-year minimum lifetime
DC Voltage	1131	50-year minimum lifetime

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

Table 10. Maximum Continuous Working Voltage, LGA[1]

Waveform	Maximum Voltage (V_{PEAK})	Constraint
AC Voltage		
Bipolar	565	50-year minimum lifetime
Unipolar	909	Limited by creepage
DC Voltage	565	Limited by creepage

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

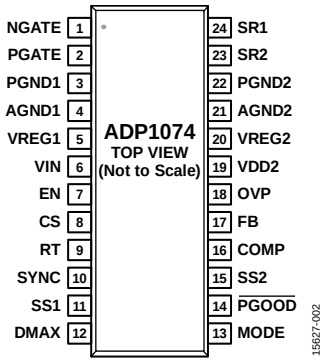

Figure 4. 24-Lead SOIC_W Pin Configuration

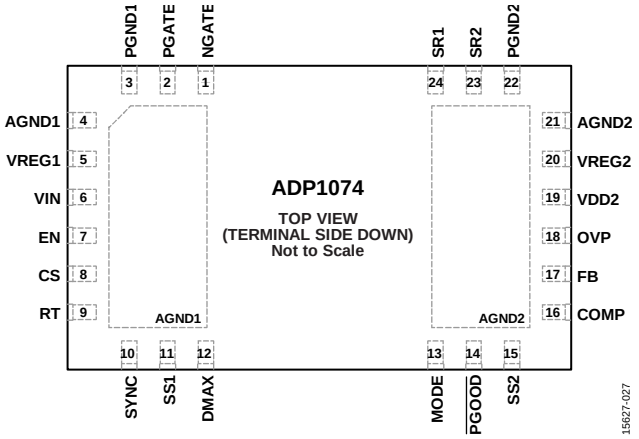

Figure 5. 24-Terminal LGA Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NGATE	Driver Output for the Main Power MOSFET on the Primary Side. Multiple function pin. Connect a resistor from NGATE to PGND1 to set up the predetermined dead time between PGATE and SR2.
2	PGATE	Driver for the Active Clamp MOSFET of the Forward Topology. This pin is referenced to PGND1.
3	PGND1	Power Ground on the Primary Side. Star connect this pin to AGND1.
4	AGND1	Analog Ground on the Primary Side. Star connect this pin to PGND1. Use this pin to differentially sense the primary current sensed with the sense resistor between the CS and AGND1 pins.
5	VREG1	8 V Output for the MOSFET Drivers. Connect 1 µF or greater at this pin. Do not put an external load on this pin. Reference this pin to PGND1.
6	VIN	Input Voltage. Connect a 4.7 µF capacitor to this pin. The size of this capacitor can be reduced if the input voltage to this pin is guaranteed stable. Reference this pin to PGND1.
7	EN	Precision Enable Input. The controller is enabled when the voltage at the EN pin is above the EN threshold voltage. Soft stop is enabled when EN drops below the EN threshold voltage. This pin also has a programmable EN hysteresis. Reference this pin to AGND1.
8	CS	Input Current Sensing. This pin senses the input pulse width modulated current. Place a current sense resistor between the source terminal of the power MOSFET and PGND1. This current sense resistor sets up the input current limit. This pin is also used for an external slope compensator. Connect a resistor from CS to the current sense resistor to generate a voltage ramp for the slope compensation. Reference this pin to AGND1. Connect a 33 pF to 100 pF capacitor to this pin to act as a resistor capacitor (RC) filter along with the slope compensation resistor in noisy environments.
9	RT	Switching Period Resistor. Connect two resistors in series that sum up to the appropriate resistor from RT to AGND1 to set the switching frequency. See the DMAX pin for more information. Also see the Frequency Setting (RT Pin) section and the Maximum Duty Cycle section for the relevant equations.
10	SYNC	Frequency Synchronization. Connect an external clock to the SYNC pin to synchronize the internal oscillator to this external clock frequency. Connect SYNC to AGND1 if this feature is not used. It is recommended that the SYNC frequency be within 10% of the frequency set by the RT pin.
11	SS1	Soft Start 1. Connect a capacitor at this pin to set up the open-loop soft start time. Reference this pin to AGND1.
12	DMAX	Maximum Duty Cycle Control. Connect DMAX to the center tap of the resistive divider at the RT pin to set up the maximum duty cycle. See the Frequency Setting (RT Pin) section and the Maximum Duty Cycle section for the relevant equations.
13	MODE	Light Load Mode Setting. Connect MODE to AGND2 to disable discontinuous conduction mode (DCM) operation, or to a high logic (2.5 V or higher, such as the VREG2 pin) to force LLM operation, or to a resistor to set up a fixed LLM threshold voltage.
14	$\overline{\text{PGOOD}}$	Power Good Pin. Open-drain output. Connect a pull-up resistor from $\overline{\text{PGOOD}}$ to VREG2.
15	SS2	Soft Start on the Secondary Side. Connect a capacitor from SS2 to AGND2 to set up the soft start time on the secondary side.

Pin No.	Mnemonic	Description
16	COMP	Compensation Node on the Secondary Side. This pin is the output of the transconductance (gm) amplifier. This pin is referenced to AGND2.
17	FB	Feedback Node on the Secondary Side. Set up the resistive divider from the output voltage such that the nominal voltage, when the power supply is in regulation, is 1.2 V. Reference this pin to AGND2.
18	OVP	Output Overvoltage Protection (OVP). The OVP threshold is set at 1.36 V. Connect a resistive divider from OVP to the output and AGND2.
19	VDD2	Input Supply on the Secondary Side. Connect VDD2 to the output voltage of the power supply for a self driven configuration. Connect a 4.7 µF capacitor from VDD2 to AGND2. The size of this capacitor can be reduced if the input voltage to VDD2 is guaranteed stable.
20	VREG2	5 V Regulated Low Dropout (LDO) Output for Internal Bias and Powering of the Drivers of the Synchronous Rectifiers. Do not use VREG2 as a reference or load. Connect a 1 µF capacitor from VREG2 to AGND2.
21	AGND2	Analog Ground on the Secondary Side. Star connect AGND2 to PGND2. Use AGND2 for differential sensing of the output voltage between the FB pin and AGND2.
22	PGND2	Power Ground on the Secondary Side. Star connect PGND2 to AGND2.
23	SR2	MOSFET Driver Output 2 for the Synchronous Rectifier MOSFET. This PWM controls the freewheeling switch.
24	SR1	MOSFET Driver Output 1 for the Synchronous Rectifier MOSFET. This PWM is in phase with NGATE.

TYPICAL PERFORMANCE CHARACTERISTICS

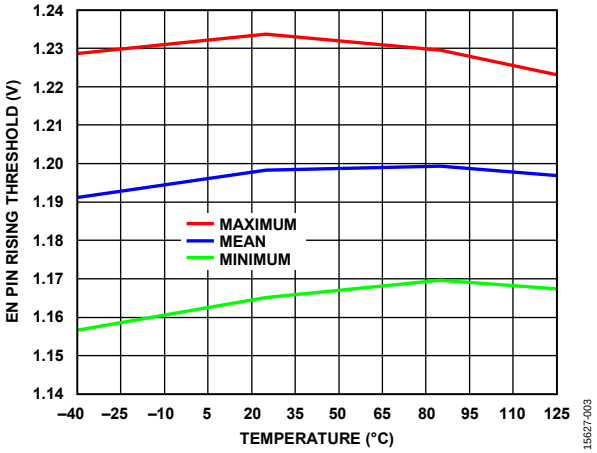

Figure 6. EN Pin Rising Threshold vs. Temperature

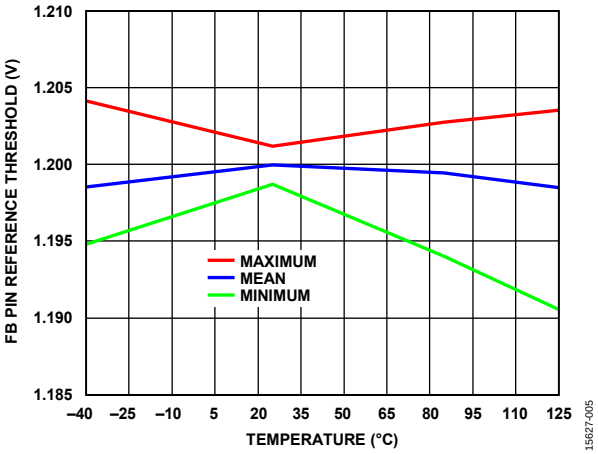

Figure 8. FB Pin Reference Threshold vs. Temperature

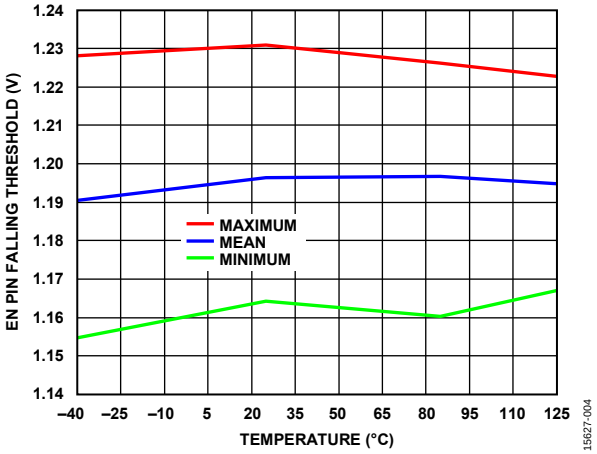

Figure 7. EN Pin Falling Threshold vs. Temperature

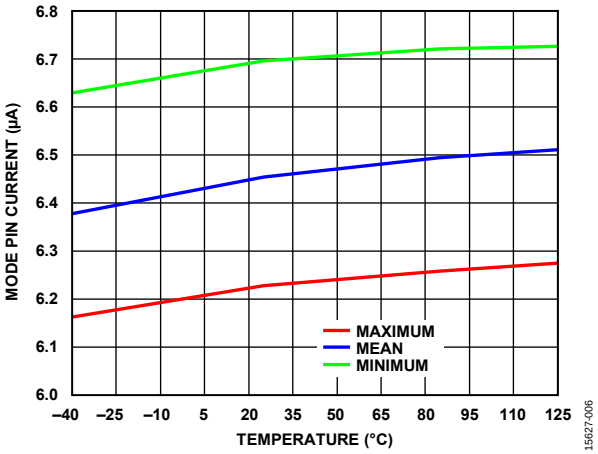

Figure 9. MODE Pin Current vs. Temperature

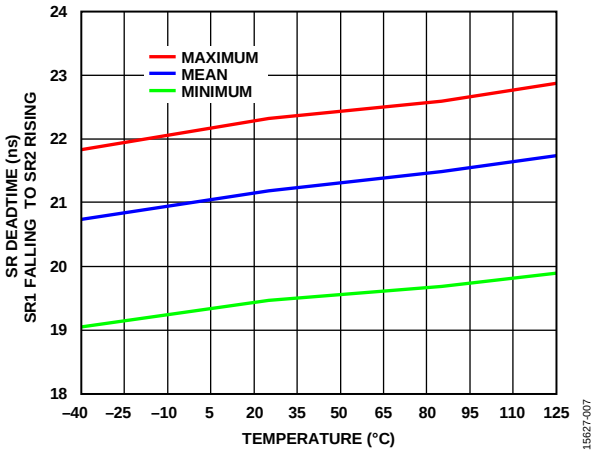

Figure 10. SR Dead Time (SR1 Falling to SR2 Rising) vs. Temperature

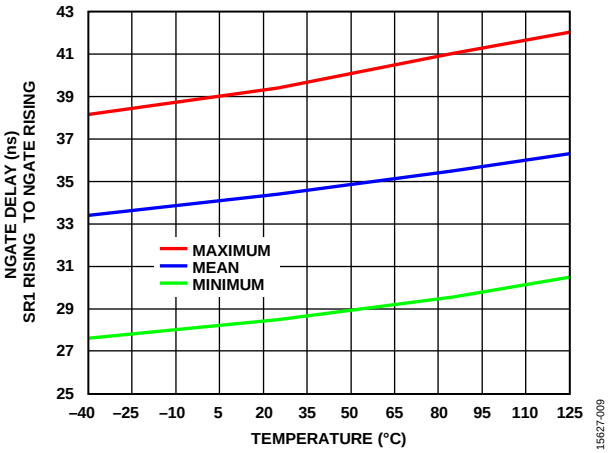

Figure 12. NGATE Delay (SR1 Rising to NGATE Rising) vs. Temperature

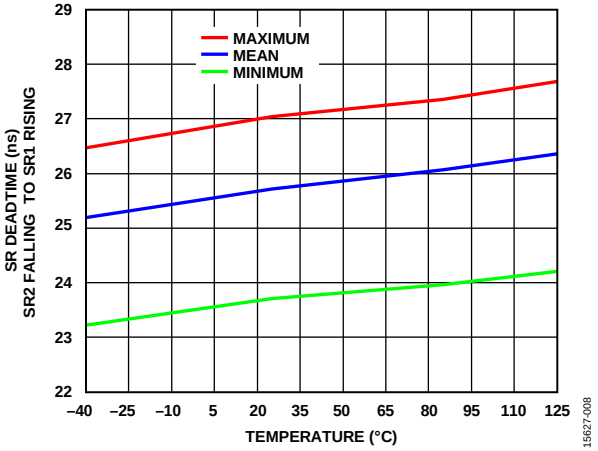

Figure 11. SR Dead Time (SR2 Falling to SR1 Rising) vs. Temperature

THEORY OF OPERATION

The ADP1074 is a current mode, fixed frequency, active clamp, synchronous forward controller designed for isolated dc to dc power supplies. Analog Devices proprietary *i*Couplers are integrated in the ADP1074 to eliminate the bulky signal transformers and optocouplers that transmit signals over the isolation boundary. Integrating the *i*Couplers reduces system design complexity, cost, and component count and improves overall system reliability. With the integrated isolators and MOSFET drivers on both the primary and the secondary side, the ADP1074 offers a compact system level design and yields a higher efficiency than a nonsynchronous forward converter at heavy loads.

Traditionally in a forward or flyback converter, a discrete optocoupler is used in the feedback path to transmit the signal from the secondary to the primary side, and an external transformer is used for transmitting the PWM signal from the primary to the secondary side for synchronous rectification. However, the current transfer ratio (CTR) of the optocouplers degrades over time and over temperature and so the optocoupler must be replaced every five to ten years, depending on the manufacturing quality and optocoupler grade that determines the initial CTR. The ADP1074 eliminates the use of optocouplers and signal transformers, thus reducing system cost, PCB area, and complexity while improving system reliability, without the issue of CTR degradation of the optocouplers.

The ADP1074 controller offers a complete solution for an isolated dc to dc power supply by integrating the 5 kV isolators and the primary and secondary control circuitries in one package.

The PWM controls are performed on the primary side by sensing the input peak current cycle by cycle with a sense resistor at the source of the main switching MOSFET. The output of the converter is sensed by the secondary circuitry, which sends the feedback and PWM signals to the primary side via the 5 kV integrated isolators for a complete control loop solution.

The primary circuitry in the ADP1074 includes an 8 V LDO, input current sensing, bias circuit, and MOSFET drivers including an active clamp reset driver, slope compensation, external frequency synchronization, PWM generator, and a programmable maximum duty cycle setting. The primary side also has pins for differential sensing of the current sense signal.

The secondary circuitry includes the feedback compensation, a 5 V LDO regulator, an internal reference, two MOSFET drivers for synchronous rectification, and a dedicated pin for overvoltage protection. Additionally, the secondary side features differential output voltage sensing and power good pins, and a programmable light load mode setting.

The integrated *i*Couplers carry out the communications between the primary and secondary sides by transmitting the feedback signal and the PWMs over the isolation barrier.

The feedback signal and timing of synchronous rectifier PWMs are transmitted between the primary and the secondary sides, or between the secondary and primary sides, through the *i*Couplers using a proprietary transmission scheme.

The ADP1074 also offers features such as input current protection, UVLO, precision enable with adjustable hysteresis, OTP, LLM, and tracking.

DETAILED BLOCK DIAGRAM

Figure 13 shows a detailed block diagram of the ADP1074.

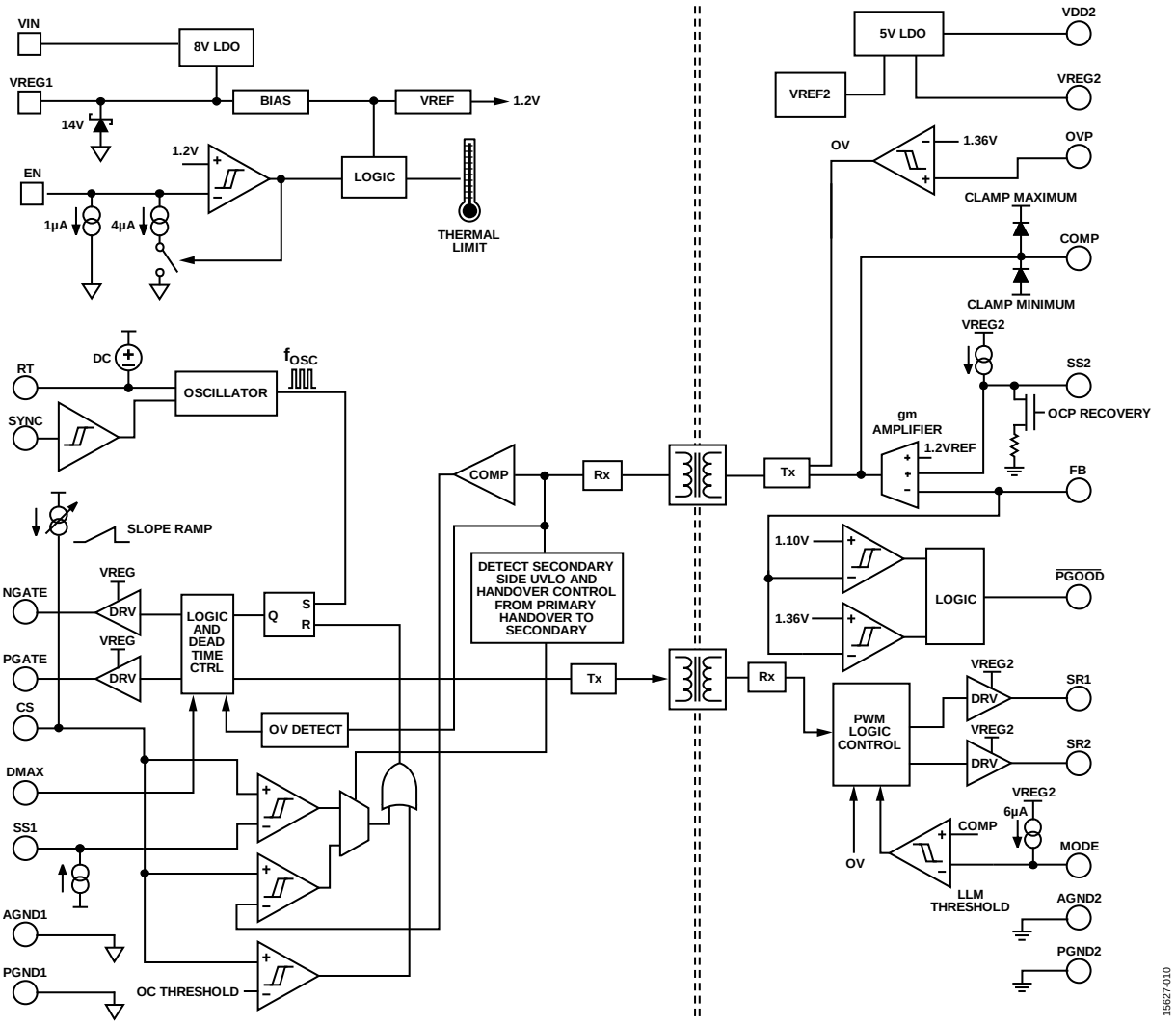

Figure 13. Detailed Block Diagram

PRIMARY SIDE SUPPLY, INPUT VOLTAGE, AND LDO

Two pins on the primary side are supply pins: VIN and VREG1. A high voltage LDO regulator connected to VIN has a regulated output of 8 V at the VREG1 pin. This LDO regulator provides power to the internal bias circuitry, primary side *i*Couplers and housekeeping circuits, and the primary MOSFET drivers at the NGATE and PGATE pins.

To reduce power consumption in the LDO for input voltages higher than approximately 30 V, an auxiliary winding on the transformer of the active clamp forward topology can be used to power VREG1. This auxiliary supply voltage must be higher than the regulated output at VREG1 so that the LDO shuts off during normal operation. The recommended auxiliary voltage is ≥8.5 V and ≤13 V because an internal 14 V Zener diode is connected at VREG1.

For a high input voltage application to avoid losses in the LDO, connect the VIN and VREG1 pins together and apply an auxiliary voltage of 8 V to 10 V, which exceeds the VIN pin UVLO of typically 4.5 V. Take care that this voltage does not exceed the internal Zener clamp voltage of 14 V (typical). The typical value is 10 V.

SECONDARY SIDE SUPPLY AND LDO

Two pins on the secondary side are supply pins: VDD2 and VREG2.

The secondary side is typically powered by the output rail of the converter by connecting it to the VDD2 pin. The UVLO for the secondary side is typically 3.5 V, at which the secondary side starts up. For output voltages less than the secondary UVLO voltage, a third winding is required to generate an auxiliary voltage to power the secondary circuitry. The internal 5 V LDO regulator at the VREG2 pin powers the MOSFET drivers, secondary side *i*Couplers, and housekeeping circuits. When VDD2 is less than 5 V, the LDO regulator operates in dropout mode.

For output voltages higher than 24 V, connecting the output voltage directly to VDD2 can result in significant power dissipation in the LDO. For instance, at 24 V and with the total driver current at 10 mA, the power dissipated in the LDO is 0.19 W (10 mA × 19 V). It is recommended to power VDD2 with an auxiliary voltage in the 8 V to 12 V range.

PRECISION ENABLE

The enable threshold at the EN pin is precision voltage referenced at 1.2 V. Assuming VIN is above the UVLO voltage (typically 4.5 V), the ADP1074 is enabled when the voltage at EN rises above 1.2 V. The crossing of the voltage, such that V_{EN} > 1.2 V, enables the internal 8 V LDO regulator on the VREG1 pin, and, after the internal biasing is finished, a soft start procedure is initiated.

Connect a resistive divider between EN and VIN to set up the input start-up voltage (see Figure 14.) An internal current source at EN allows the user to program the UVLO start-up voltage with a desirable hysteresis. To calculate the start-up voltage with hysteresis, use the superposition theorem or nodal analysis to obtain the EN pin voltage, as follows:

$$V_{EN} = V_{IN} \times \frac{R2}{R1 + R2} - I_{EN} \times (R1 \,||\, R2 + RH)$$

where:

V_{EN} is the EN pin voltage.

I_{EN} is the current source at the EN pin (1 µA for turn on and 4 µA for turn off).

The user can adjust the R1, R2, and RH resistors such that $V_{EN} \geq 1.2$ V and obtain the desired hysteresis.

An internal 1 µA pull-down current is always on, and the 3 µA current is active only when the V_{EN} is below the EN threshold and becomes inactive when V_{EN} is above the EN threshold.

In general, a higher input voltage requires a larger hysteresis. It is recommended to keep a capacitor on the EN pin to AGND1 to provide a low impedance path that prevents any noise, which toggles the EN pin when the input voltage hovers at the threshold.

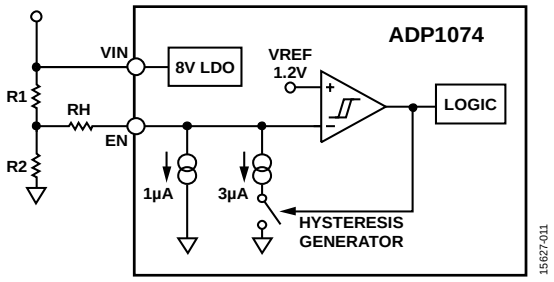

Figure 14. Precision EN with Adjustable Hysteresis

When the EN pin is less than the EN threshold, the system enables the soft stop procedure. SR1 and SR2 take up to a maximum of two switching periods to terminate. See the Soft Start Procedure section for more details.

SOFT START PROCEDURE

The following procedure assumes that the VDD2 pin is powered directly from the output voltage of the power supply.

To ensure a smooth output voltage ramp during startup, the soft start sequence is controlled by two soft start control circuits, one in the primary (for open-loop soft start, using the SS1 pin) and the other in the secondary (for closed-loop soft start, using the SS2 pin). Proper handshaking between the primary side and the secondary side is needed prior to the secondary side taking control.

The open-loop soft start time is determined by the capacitor on the SS1 pin. This pin sources a 9.1 µA constant current that builds up a voltage on the SS1 pin. The voltage on the SS1 pin is proportional to the peak primary current limit where 0 V and 1.5 V correspond to a peak current of 0 A and 120 mV/R_{SENSE}, respectively. This rate is the open-loop soft start. During this time, the ADP1074 starts firing the PWM pulses, and the output voltage continues to build up slowly if the average inductor current limit exceeds the load current. Because the ADP1074 is a current mode controller, the output capacitor

starts charging only when the primary current limit exceeds the load current requirement.

The rate at which the SS1 pin voltage rises to the maximum current limit is given by

$$dt = C_{SS1} \times 1.5/(9.1\ \mu A)$$

The handshaking process is as follows.

When VDD2 reaches the UVLO of approximately 3.5 V, the internal circuitry on the secondary side is activated and the ADP1074 initiates the following process:

1. The ADP1074 makes the voltage on the SS2 pin equal to the value on the FB pin, with an SS2 pin current, at ten times the nominal current source of 20 µA on the SS2 pin.
2. Simultaneously, the current limit on the primary (which is the voltage on SS1) is transferred over to the secondary side, and the voltage on the COMP pin is made equal to the instantaneous SS1 voltage ± 100 mV. There is a timeout for this process, which is 1.5 ms after the VDD2 UVLO threshold is crossed.

When this process is satisfied, the transmission of the COMP signal occurs from the secondary to the primary side. The ADP1074 transmits the COMP signal by continuously sampling the analog signal at the COMP pin. The sampled value is then transmitted using a proprietary scheme to the primary side where the instantaneous value of the CS pin is compared to the COMP level to determine the falling edge of the NGATE pulse. The COMP signal is, therefore, a representation of the primary current limit.

After COMP transmission begins, the primary side receives the signal and control is completely handed over to the secondary side when either the received level of COMP on the primary side is within ±100 mV, or up to 128 switching periods (typically 8) have passed, starting from the first pulse being transmitted to the primary side.

Then, the control is handed over to the secondary side and the closed-loop soft start begins, where the SS2 capacitor is charged at a nominal rate of 20 µA. The output voltage then rises to the regulation voltage based on the SS2 pin voltage. The voltage on the SS2 pin continues to rise to 1.2 V, that is, the steady state voltage on the FB pin. At this stage, the power supply is in regulation, and the output voltage is at its target value.

At the end of the soft start process, the voltage on the SS2 pin continues to rise to approximately 1.4 V. The instant that the handover takes place, SS1 is discharged to 0 V. In steady state, the FB pin (that is, the reference voltage) is 1.2 V.

The SR1 and SR2 synchronous drivers begin to pulse after VDD2 crosses the UVLO threshold.

If the voltage at the VDD2 pin is greater than the UVLO voltage, such as a soft start from the precharged output, or if the VDD2 pin is powered by an external supply, the secondary side assumes control from the moment the EN pin is enabled, and only SS2 is used for the soft start procedure.

When initiating a soft start from the precharged output, the SS2 pin tracks the FB pin and then initiates a soft start. This process eliminates any glitches in the output voltage.

When soft starting into a precharged output, the SRx gates are prevented from turning on until the SS2 voltage has reached the precharged voltage at the FB pin. This soft start scheme prevents the output from being discharged, and it prevents reverse current.

Under abnormal situations, such as a shorted load or a transient condition on the load during the soft start process, FB may not be able to track SS2 accurately. If this occurs before the VDD2 UVLO threshold is crossed, SS1 is in control. If it occurs after the VDD2 UVLO threshold is crossed, SS2 tracks the FB pin and then continues with the soft start process until the regulation voltage is reached. In all conditions, control is handed over to the secondary if FB ≥ 1.2 V.

When the secondary VDD2 is directly powered by the output of the converter, the minimum output voltage required is higher than the secondary UVLO voltage. For output voltages less than the secondary UVLO voltage, a third winding is needed to generate an auxiliary voltage to power the secondary side circuitry. Alternately, in most cases, a diode resistor capacitor combination from the switch node can provide the voltage to VDD2.

OUTPUT VOLTAGE SENSING AND FEEDBACK

The output voltage of the converter is set by a resistive divider to the FB pin. The resistive divider must be set in a manner such that the voltage at the FB pin is 1.2 V in steady state. The output voltage must be differentially sensed using the FB pin and the AGND2 pin.

LOOP COMPENSATION AND STEADY STATE OPERATION

The FB pin feeds into the negative terminal of a transconductance amplifier (or gm amplifier) with a gain of approximately 250 µA/V. The positive input terminal of the gm amplifier is connected to SS2, which provides the reference setpoint voltage. The output of the gm amplifier is connected to the COMP pin. The voltage on the COMP pin is representative of the current peak limit required to sustain regulation. This pin is continuously sampled, and the signal is transmitted to the primary side, where it is compared to the sensed primary current using a comparator. When the comparator trips, it causes NGATE to terminate.

Typically, an RC network in series is connected between the COMP pin and AGND2 for compensation. A high frequency pole in the form of a capacitor can also be added in parallel to the RC network.

The output of the gm amplifier is clamped to a minimum and maximum current of approximately −57 µA and +43 µA, respectively.

The COMP node is clamped to a lower and higher level of approximately 0.7 V and 2.52 V, respectively. This is representative of the CS range from 0 mV to 120 mV.

SLOPE COMPENSATION

For a peak current mode controller with duty cycle higher than 50%, slope compensation is necessary for a stable operation. To set up an external compensation in the ADP1074, connect the external R_{RAMP} resistor (see Figure 25) between CS and the current sense resistor, R_{SENSE}, to set up the slope voltage ramp for the control signal. It is important to sense the signal differentially. See the Layout Guidelines section for more details.

An internal ramp current starts from 0 µA at the minimum duty cycle (that is, the beginning of the switching period) and increases linearly toward a maximum of 20 µA at the end of the switching period. The slope of the voltage ramp is the ramp current times R_{RAMP}. R_{RAMP} is sized using the following equation:

$$R_{RAMP} \geq k \frac{V_{OUT}}{L} \times \frac{N2}{N1} \times \frac{R_{SENSE}}{20\,\mu A} \times t_S$$

where:
k = 0.5 for nominal cases and k = 1 for deadbeat control.
V_{OUT} is the desired output voltage.
L is the output inductor.
$N1$ and $N2$ are the primary and secondary turns of the transformer.
t_S is the switching period.

INPUT/OUTPUT CURRENT-LIMIT PROTECTION

There is no direct current-limit sensing circuit on the secondary; the output current limit is indirectly limited by the cycle-by-cycle primary side current limit of 120 mV on the CS pin.

The input peak current limit is set by connecting a sense resistor, R_{SENSE}, from the source of the main MOSFET to PGND1 (see Figure 25), and the sensed voltage appears at the CS pin. To generate the slope-comp ramp, insert the slope compensation resistor, R_{RAMP}, between CS and R_{SENSE}.

The CS current limit, V_{CSLIM}, is internally set to 120 mV. Calculate the R_{SENSE} value by

$$R_{SENSE} = \frac{V_{CSLIM} - R_{RAMP} \times 20\,\mu A}{I_{PKPRI}}$$

where:
V_{CSLIM} is the CS current limit.
I_{PKPRI} is the primary peak current.

When the sensed input peak current is above the CS limit threshold, the controller operates in the cycle-by-cycle constant current-limit mode for 1.5 ms. Then the controller immediately shuts down the primary and secondary drivers. The controller then goes into hiccup mode for the next 40 ms and restarts the soft start sequence after this timeout period.

The slope ramp can affect the accuracy of the current-limit threshold because the voltage drop across R_{RAMP} contributes to the inaccuracy of the peak current limit. For instance, if the added slope ramp voltage is 20% of the current-limit threshold, the actual input peak current limit can be off by as much as 20% depending on where the peak current-limit threshold is tripped during the on cycle. In the event of an output short circuit, the controller treats this condition as an overcurrent event and enters the 40 ms hiccup mode.

Under certain conditions, the ADP1074 exits OCP hiccup mode. In these conditions, the COMP pin is at the maximum clamp level, but the device does not enter hiccup mode. However, it is guaranteed that the PWMs are terminated whenever the CS maximum threshold is reached. The condition under which the ADP1074 skips entering hiccup mode is when VDD2 is powered through an auxiliary winding and an output short circuit occurs that results in the FB pin having a voltage that is <300 mV. This event is more prominent at high temperatures (>85°C), and can be exacerbated at higher temperatures.

The root cause of the device exiting hiccup mode is due to the effect that the OCP hiccup mode feature has on the SS2 pin. During OCP recovery, the SS2 pin tracks the FB pin and attempts a soft start from the precharge sequence. During the time when SS2 tracks the FB pin, the SS2 pin voltage can be less than the FB pin for a short interval, which causes the COMP pin (output of the gm amplifier) to momentarily dip below the maximum COMP pin clamp level. This event means that the current limit required for the next few switching periods is less than the maximum threshold and puts the device out of hiccup mode because the ADP1074 fails to register 1.25 ms worth of consecutive overcurrent cycles.

To guarantee OCP hiccup mode, the following circuits are recommended based on the configuration of the VDD2 power supply:

1. When VDD2 is powered directly from the output voltage, if a short circuit occurs on the output terminals of the load after steady state regulation is achieved, the voltage of the VDD2 pin is less than the UVLO, and the device enters hiccup mode for 200 ms, similar to the hiccup time described in the Remote System Reset section.
2. When VDD2 is powered through auxiliary winding or another configuration, when a short circuit occurs on the output terminals, the auxiliary winding is not shorted and maintains a positive voltage above the UVLO threshold of the VDD2 pin. To enter hiccup mode, it is recommended to use the circuit shown in Figure 15. The circuit operates as follows: when the output voltage goes low due to a short circuit, the D1 diode turns on, which pulls the base of the bipolar junction transistor low, shutting off VDD2. The system then enters hiccup mode, as described in the Remote System Reset section.

   R3 is sized to bias the Zener diode and R4 is sized such that $(V_{ZENER} - 1)/R4 > I_{ZENER}$, where V_{ZENER} is the voltage of the diode and I_{ZENER} is the biasing current of the diode. This sizing ensures that the impedance of the resistor is less than the impedance of the diode, which causes the voltage of the diode to drop, and allows VDD2 to enter UVLO.

If the output voltage is <5 V, the same procedure can be used to size the R4 resistor. If a discrete LDO is not used, a simple resistor and diode connector to the output voltage is sufficient. In this case, the R4 resistor is sized to limit the current through the D1 diode when the output voltage is 0 V during a short-circuit event. Because the bandwidth of the system is high, the ADP1074 is able to maintain voltage regulation at the proper voltage level, even if the auxiliary winding voltage is higher than the output voltage. The soft start and soft start from precharge conditions is met with the addition of this circuit due to the bandwidth of the overall system.

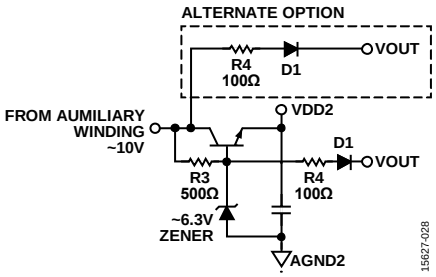

Figure 15. Recommended Circuit to Guarantee Hiccup Mode Showing Typical Values

TEMPERATURE SENSING

The ADP1074 has an internal temperature sensor that shuts down the controller when the internal temperature exceeds the OTP limit. At this time, the primary and secondary MOSFET drivers (PGATE, NGATE, SR1, and SR2) are held low. When the temperature drops below the OTP hysteresis level, the ADP1074 restarts with a soft start sequence.

FREQUENCY SETTING (RT PIN)

The switching frequency can be programmed in a range of 50 kHz to 600 kHz by connecting a resistor from RT to AGND1. A small current flows out of the RT pin and the voltage across it sets up the internal oscillator frequency. The value of this pin is approximately 1.224 V in steady state. Use the following equation to determine the resistor (in Ω) for a particular switching frequency (in kHz):

$$f_S(\text{kHz}) = \frac{1}{41.67 \times 10^{-12} \times (R_{TOP} + R_{BOT})} \times \frac{1}{1000}$$

where:
f_S is the switching frequency.
R_{TOP} is the top resistor of the divider.
R_{BOT} is the bottom resistor of the divider.

MAXIMUM DUTY CYCLE

To prevent the transformer core from saturating in the event of high current or extreme load transient and reduce voltage stress on the MOSFETs, a maximum duty cycle clamp can be set by connecting the DMAX pin to the center tap of the resistive divider that is connected from RT to AGND1, as shown in Figure 16.

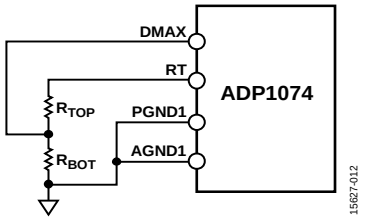

Figure 16. Setting the Maximum Duty Cycle, D_{MAX}

The maximum duty cycle is calculated by the following:

$$D_{MAX} = 50 + \frac{50 \times R_{BOT}}{(R_{TOP} + R_{BOT})}\%$$

where:
D_{MAX} is 50% when R_{BOT} is 0 Ω or when the DMAX pin is connected to AGND1. For example, when R_{TOP} is equal to R_{BOT}, D_{MAX} is 75%. D_{MAX} can reach 100% if R_{TOP} is 0 or when R_{BOT} becomes open circuit.
R_{BOT} is the bottom resistor of the divider.
R_{TOP} is the top resistor of the divider.

As an added protection feature to prevent open-loop conditions, the maximum duty cycle is also applicable during soft start. If the controller reaches DMAX during soft start for three consecutive switching periods, the 40 ms hiccup timer is initiated.

FREQUENCY SYNCHRONIZATION

The switching frequency of the ADP1074 can be synchronized to an external clock at the SYNC pin. When an external clock rising edge is first detected, it takes approximately seven to ten periods for the internal clock to lock in the SYNC clock frequency. In between the time that the SYNC clock is detected and the time that it is locked in, the controller continues to operate with the internal oscillator frequency.

The SYNC frequency must be within ±10% of the internal oscillator frequency set by the RT pin; otherwise, synchronization does not take place.

A clock signal can be applied to SYNC on the fly or prior to the soft start sequence. A dithered clock can also be applied to SYNC to reduce the peak electromagnetic interference (EMI) noise in the converter output and switch node. The internal clock is able to lock onto the dithered clock cycle by cycle.

It is recommended to connect the SYNC pin to AGND1 if this feature is not used.

SYNCHRONOUS RECTIFIER (SR) DRIVERS

There are two synchronous rectifier drivers on the secondary side for driving the synchronous switches. SR1 is the forward driver that is in phase with the primary side NGATE driver, and SR2 is the freewheeling driver. VDD2 is the front end of the LDO at VREG2. The 5 V internal LDO at VREG2 powers the SRx drivers and all internal circuits on the secondary side. The recommended power supply range at VDD2 is from 6 V to 36 V. However, at 36 V input to VDD2, the power dissipation in the LDO can be significant. If VDD2 is less than 5 V, the LDO

operates in the dropout region, where VREG2 and the driver output are less than 5 V. In this case, it is recommended to supply VDD2 with an auxiliary power supply greater than 5 V.

VDD2 can be directly connected to the converter output or an auxiliary power supply, which can be realized by using a third winding of the main transformer. For additional drive strength, SR1 and SR2 can be fed into an external MOSFET driver such as the ADP3624 or the ADP3654.

OUTPUT OVERVOLTAGE PROTECTION (OVP)

When the output voltage exceeds the OVP threshold of 1.36 V, the controller immediately shuts off the drivers (NGATE, PGATE, SR1, and SR2) on both the primary and secondary side. When the voltage at the OVP drops below the OV hysteresis level, the controller resumes switching in the next switching period with the primary drivers, followed by phasing in of the SR1 and SR2 PWMs. The OVP feature causes the system to enter hiccup for 200 ms if the voltage on the OVP pin exceeds 1.36 V for a sustained period of 200 µs.

ACTIVE CLAMP (PGATE)

In a forward converter, the magnetizing energy stored in the transformer core during the on cycle must be demagnetized or reset during the off cycle; otherwise, the transformer core saturates in subsequent switching cycles. To reset the transformer core, an active clamp switch is turned on during the off cycle, which enables the reset of the transformer. This process reduces power dissipation and increases overall efficiency. The active clamp switch can be a high-side or a low-side switch using the driver at the PGATE pin.

LEADING EDGE BLANKING

A leading edge blanking time is added after the rising edge of the NGATE signal to avoid picking up any unwanted noise or ringing at the CS pin at the start of the switching period.

GATE DELAY AND SR DEAD TIME

At high input voltages, the rise and fall times of the main MOSFET on the primary side are larger than at lower input voltages. It is important to have a programmable delay time between the PGATE rising and the NGATE rising to account for different input voltages, leakage inductances of the transformer, and MOSFET output capacitances. Also, a sufficient gate delay between PGATE and NGATE ensures zero volt switching (ZVS), which is important for reducing switching losses in the main MOSFET.

The total delay between the PGATE and NGATE rising edges can be programmed with a resistor connected to the NGATE pin. The resistor connected to NGATE is determined by the ADP1074 prior to soft start. The programmable delay between PGATE to NGATE has four discrete settings having typical values of 30 ns, 60 ns, 100 ns, and 150 ns. See Figure 17 for more details.

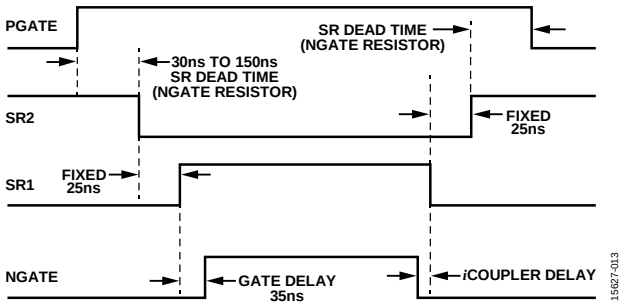

Figure 17. Gate Delay and SR Dead Time Settings

To maximize efficiency and avoid cross conduction between the primary NGATE and SR2 (freewheeling switch), it is necessary to have a delay time between SR2 and NGATE.

As shown in Figure 17, the NGATE falling edge and SR1 falling edge turn off simultaneously with an *i*Coupler delay.

In addition, a dead time between SR1 and SR2 is internally fixed to 25 ns (typical) to avoid shorting out the secondary transformer winding.

LIGHT LOAD MODE (LLM) AND SR PHASE IN

Add a resistor at the MODE pin to enable the ADP1074 power saving LLM feature. A current source from the MODE pin of 6.5 µA into this resistor sets up the LLM threshold voltage, which is compared to the COMP voltage. When the COMP voltage rises above the LLM threshold (that is, the MODE pin voltage), the SRx PWMs gradually increase (or phase in) from the duty cycle at light load to the steady state duty cycle at the SRx phase in rate. The SRx phase in rate moves the SRx edges every 1.5 ns per µs. Without the phase in sequence, a dip in the output voltage can occur if the SRx PWMs transition from zero to full duty cycle instantaneously.

In a load dump situation, for example, when the load is stepped from full load to light load, that is, from continuous conduction mode (CCM) to discontinuous conduction mode (DCM) operation, the duty cycles of the SRx PWMs gradually phase out at the SRx phase out rate, which has the same numerical value of the SRx phase in rate. The phase out sequence of the SRx PWMs prevents reverse current in the secondary, and at the same time, optimizes the dynamic performance of the output response. Note that the level of COMP is still above the minimum COMP clamp level at this point, and the ADP1074 outputs duty cycles with minimum on time.

If the load is further reduced and the COMP pin voltage becomes equal to the minimum COMP clamp level, the ADP1074 enters pulse skip mode.

The NGATE delay time settings shown in Figure 17 remain unchanged in LLM operation. Use the following formula to set up the light load mode threshold:

$$R_{MODE} = \frac{I_{PEAK\_LLM} \times CS_{GAIN} + 0.8}{I_{MODE}}$$

where:

I_{PEAK_LLM} is the peak primary current at the light load condition.
CS_{GAIN} = 12.5.
I_{MODE} is the current flowing out of the MODE pin.

For a forced CCM operation, connect MODE to AGND2. In this case, pulse skipping is disabled.

Note also that when the system enters light load mode, the synchronous rectifiers terminate at the falling edge of SR1. This termination facilitates the prevention of the PWM at a negative current, which can cause a spike in voltage that can damage the synchronous FET.

EXTERNAL START-UP CIRCUIT

For input voltages higher than 36 V, where the power dissipation in the internal 8 V LDO can be significant, the use of an external start-up circuit is recommended. (See Figure 18 for an example.) In this case, the VIN and VREG1 pins are shorted together and connect to the output of the start-up circuit. Because the input pre-enable bias current, the (VIN + VREG1) start-up current, is approximately 160 µA, the output of the start-up circuit must be able to provide this level of current to perform a soft start. The auxiliary winding then provides the bias voltage, shutting off the start-up circuit after soft start completes.

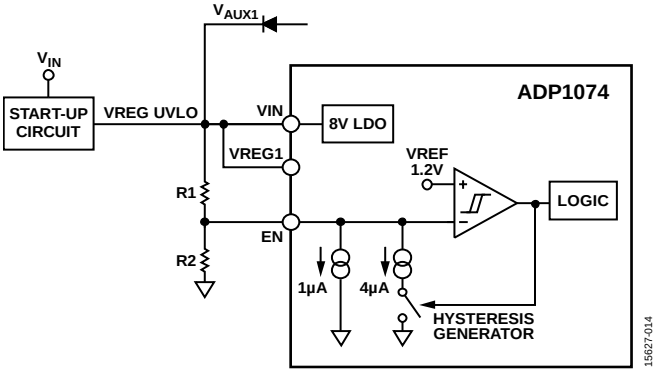

Figure 18. Precision EN Circuit Connection with an External Start-Up Circuit

A fast start-up circuit is shown in Figure 19. This circuit requires two components: a Zener diode, which sets up the start-up voltage at the VIN and VREG1 pin, and a negative-positive-negative (NPN) transistor, which sets up a fast current path for charging up the start-up capacitor, C1. The start-up current through R1 must be more than 160 µA, which is the minimum specified start-up current, and it is recommended that the start-up voltage at VREG1 and VIN be approximately 8 V to 13 V. The auxiliary winding then provides the bias voltage, shutting off the NPN transistor after soft start completes.

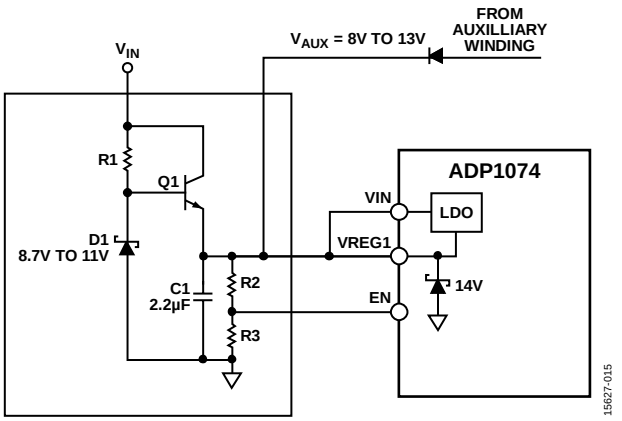

Figure 19. Fast Start-Up Circuit

SOFT STOP

The ADP1074 employs a soft stop feature that brings the output voltage gradually down to zero by using the SS2 pin as a reference. During the soft stop procedure, the SS2 pin is discharged to zero by a current sink of approximately 1.5 times the value during closed-loop soft start.

When the voltage at EN drops below the EN threshold, the SR1 and SR2 secondary drivers shut off immediately, and the primary NGATE pulse width gradually decreases the duty cycle from the last known condition to the minimum pulse width and down to zero, causing the output voltage to decrease. The soft stop feature prevents any reverse current when the controller is shut down.

When the output voltage decreases below the VDD2 UVLO threshold, there is no transmission of the COMP signal to the primary side. Therefore, the output voltage continues to decrease at the rate at which the load current discharges the output capacitor.

When the load is at a minimum or at no load, the output voltage does not discharge because any reduction in duty cycle or current limit does not discharge the output voltage linearly.

POWER GOOD

The $\overline{\text{PGOOD}}$ pin is an open-drain N-channel metal-oxide semiconductor (nMOS), which is off in fault conditions. Connect a pull-up resistor between $\overline{\text{PGOOD}}$ and VREG2 or to an external power supply less than 5.5 V.

To toggle $\overline{\text{PGOOD}}$, the fault voltage on the FB pin and the OVP pin must exceed the overvoltage threshold of 1.36 V. $\overline{\text{PGOOD}}$ also toggles if the FB pin voltage drops 100 mV below the nominal of 1.2 V, that is, to 1.1 V.

$\overline{\text{PGOOD}}$ toggles again after the output voltage crosses the $\overline{\text{PGOOD}}$ hysteresis voltage of 36 mV. $\overline{\text{PGOOD}}$ becomes active after a delay of 5 µs for an FB pin fault and after 90 ns for an OVP pin fault.

OCP/FEEDBACK RECOVERY

During steady state, the FB pin is at 1.2 V. At this time, the SS2 pin voltage is 1.4 V. Under abnormal situations, such as an overload condition, the output voltage can dip severely. In such an event, the current limit is at the maximum level, and the COMP pin voltage is at its clamp level. If the two conditions of the COMP pin voltage being clamped and V_{FB} < (1.2 V − 100 mV) are satisfied, the controller discharges the SS2 pin using a fast current sink (200 μA) to make the SS2 pin equal to the FB pin. The controller then attempts to perform a soft start from this precharged condition, that is, from the last known value of the output voltage. This process is how the OCP/feedback recovery feature operates.

However, if at any time the voltage on the COMP pin is above the maximum clamp voltage for a period greater than 1.5 ms, the system enters hiccup mode.

During the soft start from precharge, the output voltage rises at the same rate as determined by the capacitor on the SS2 pin. If, however, there is a detrimental fault in the power stage that prevents the rise of the output voltage, V_{FB} does not track SS2, and when SS2 > (V_{FB} + 100 mV), the COMP pin voltage increases to the clamp level, and the system again enters OCP/feedback recovery mode.

OUTPUT VOLTAGE TRACKING

The ADP1074 offers a tracking feature. During steady state, the FB pin is at 1.2 V. At this time, the SS2 pin voltage is at 1.4 V. Using an external DAC, the voltage on the SS2 pin can modulate the output voltage. It is recommended that the SS2 pin voltage be changed only after the VDD2 UVLO point is crossed, and control is handed over to the secondary side, or else the handover process does not occur smoothly, resulting in glitches in the output voltage. Ideally, the $\overline{\text{PGOOD}}$ pin can be used as a signal that indicates that regulation is achieved, to initiate the tracking.

The SS2 voltage must be brought down from 1.4 V to 1.2 V, and it must be brought down even further to effect any change in the output voltage. The rate at which the output tracks the SS2 pin is dependent upon the overall system bandwidth. Note that while modulating the output voltage, if the FB pin voltage drops below (1.2 V − 100 mV = 1.1 V), the $\overline{\text{PGOOD}}$ pin toggles.

REMOTE SYSTEM RESET

For a remote (secondary side) system shutdown, an open-drain general-purpose input/output (GPIO) of an external microcontroller can be used to force the SS2 pin to 0 V. This pull-down causes the ADP1074 to regulate to 0 V, and the ADP1074 enters pulse skip mode or outputs a minimum duty cycle because the SS2 pin offsets because of the finite resistance of the GPIO.

When VDD2 is charged from the output bus, this setup is equivalent to a system shutdown, because when VDD2 < VDD2 UVLO, the ADP1074 enters a special hiccup mode of 200 ms (instead of the standard 40 ms hiccup).

When VDD2 is powered using auxiliary winding, the system regulates to the voltage proportional to the voltage on the SS2 pin and eventually enters the special hiccup mode previously mentioned, after the auxiliary rail decays below the VDD2 UVLO threshold.

Therefore, the SS2 pin can achieve output tracking as well as a secondary side shutdown, also known as remote system reset, as shown in Figure 20.

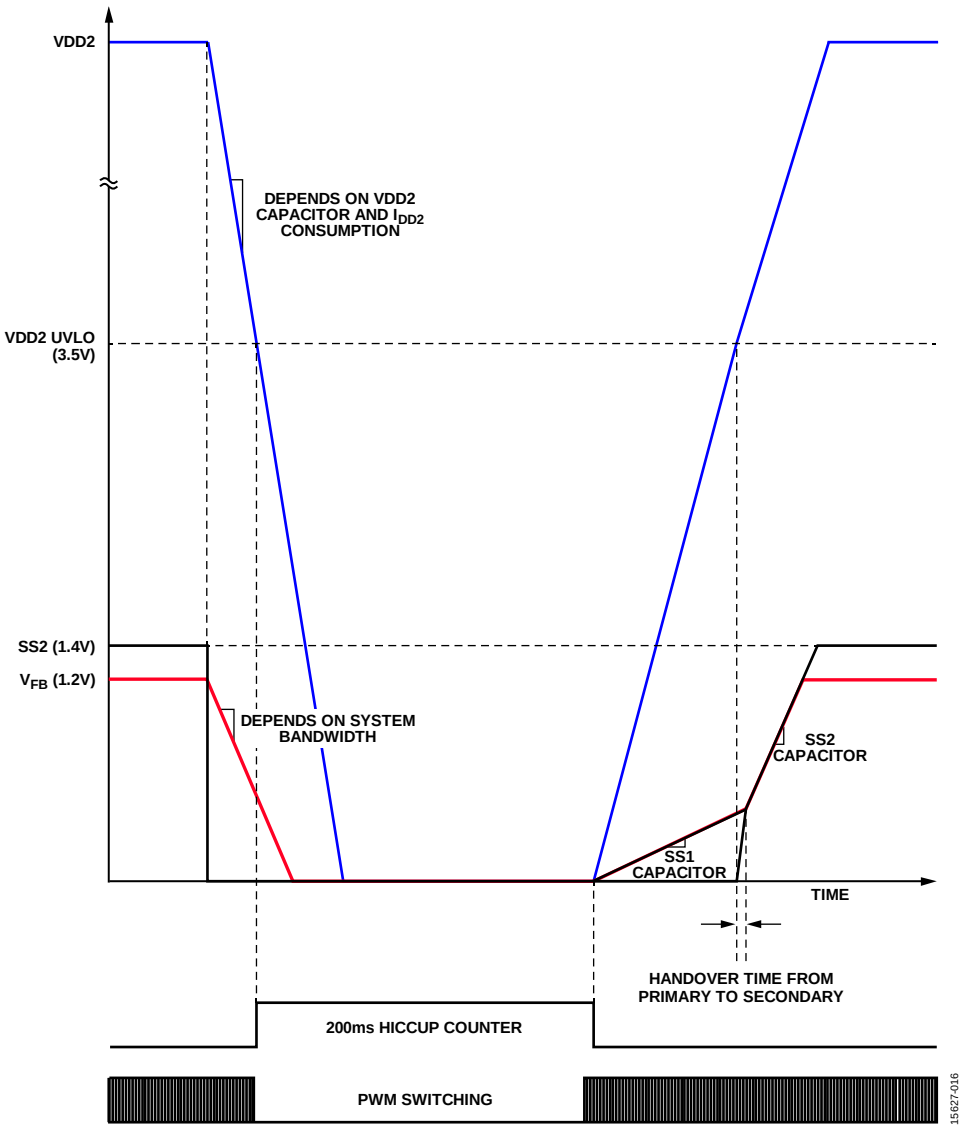

Figure 20. Remote Software Reset with 200 ms Hiccup

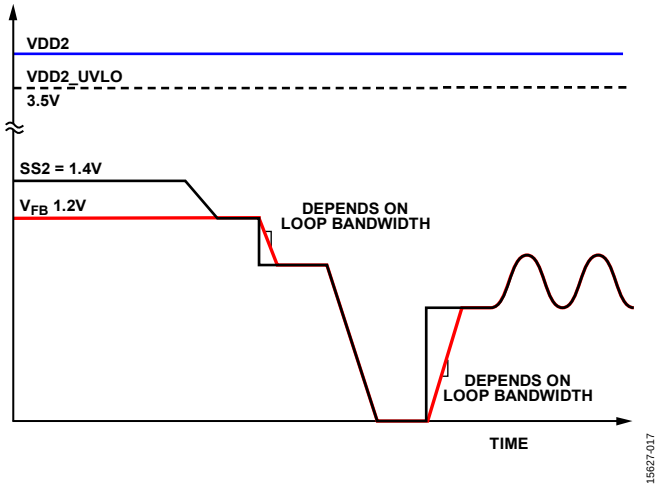

Figure 21. Tracking with SS2 Pin

OCP COUNTER

During overload conditions, when the peak sensed currents exceed the OCP threshold voltage of 120 mV on the CS pin, the ADP1074 immediately terminates the remainder of the PWM pulse. If the peak sense current continues to exceed the threshold every switching period for 1.5 ms, the system enters hiccup mode, by which it shuts down for approximately 40 ms and then soft starts. During an exceeded overcurrent situation, such as a dead short, it is likely that the programmed slope compensation is not enough, and therefore, the system enters subharmonic oscillation. If this is the case, the system cannot enter hiccup mode because the OCP threshold is crossed every alternate switching period, and the 1.5 ms hiccup counter resets.

To prevent this scenario, the ADP1074 latches the last known state, whereby if an OCP condition registered as a 1 in one switching period and as a 0 in the next switching period, it is still counted as a 1. In this manner, the system can enter hiccup mode even in subharmonic oscillation. Missing two OCP thresholds consecutively resets the hiccup counter.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent upon the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADP1074.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 9 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition. In many cases, the approved working voltage is higher than the 50 year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The ADP1074 insulation lifetime depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 22, Figure 23, and Figure 24 show these different isolation voltage waveforms.

A bipolar ac voltage environment is the worst case for the *i*Coupler products, yet meets the 50 year operating lifetime recommended by Analog Devices for maximum working voltage. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. The low stress allows operation at higher working voltages while still achieving a 50 year service life. Treat any cross insulation voltage waveform that does not conform to Figure 23 or Figure 24 as a bipolar ac waveform, and limit its peak voltage to the 50 year lifetime voltage value listed in Table 9.

Note that the voltage presented in Figure 23 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

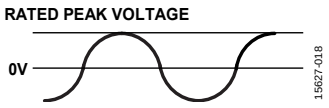

Figure 22. Bipolar AC Waveform

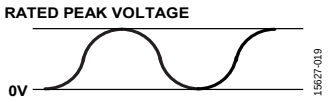

Figure 23. Unipolar AC Waveform

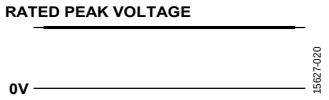

Figure 24. DC Waveform

LAYOUT GUIDELINES

The layout guidelines for the primary side are as follows:

1. Ground all the capacitors to their respective grounds. For example, ground the SS1 capacitor to AGND1.
2. Use the CS pin and the AGND1 pin to differentially sense the primary current measurement through the sense resistor. Do not cross the CS and AGND1 traces for current sensing across any switch nodes.
3. Place a capacitor (33 pF to 470 pF typical) close to the CS pin, connected to AGND1.
4. Connect the ground plane on the primary side to PGND1.
5. Connect AGND1 to PGND1 using a 0 Ω resistor.
6. Place resistors (1 Ω to 5 Ω typical) in series with NGATE and the main power MOSFET. These resistors aid in eliminating any ringing on the drive voltages.

The layout guidelines for the secondary side are as follows:

1. Ground all the capacitors to their respective grounds. For example, ground the SS2 capacitor to AGND2.
2. Place resistors (1 Ω to 5 Ω) in series with SRx and the synchronous MOSFET. These resistors aid in eliminating any ringing on the drive voltages.
3. Connect the ground plane on the secondary side to PGND2. Connect the negative terminal of the output voltage to the PGND2 plane.
4. Use the FB pin and the AGND2 pin to remotely differentially sense the output voltage by connecting AGND2 to the negative terminal of the output voltage using a 0 Ω resistor.
5. Use a 100 nF capacitor on the MODE pin if light load mode is used in noisy environments.

TYPICAL APPLICATION CIRCUITS

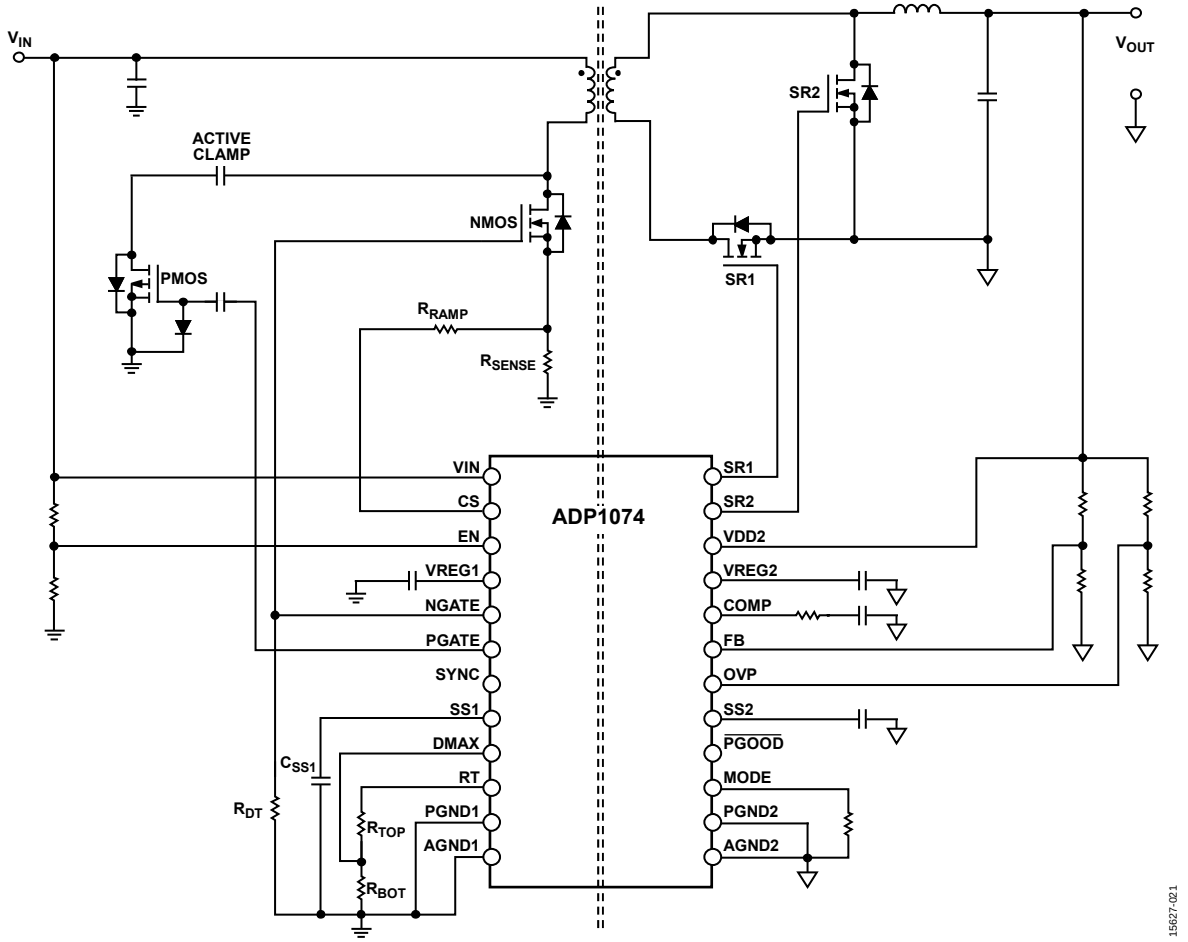

Figure 25. Typical Application Circuit for Active Clamp Forward Topology

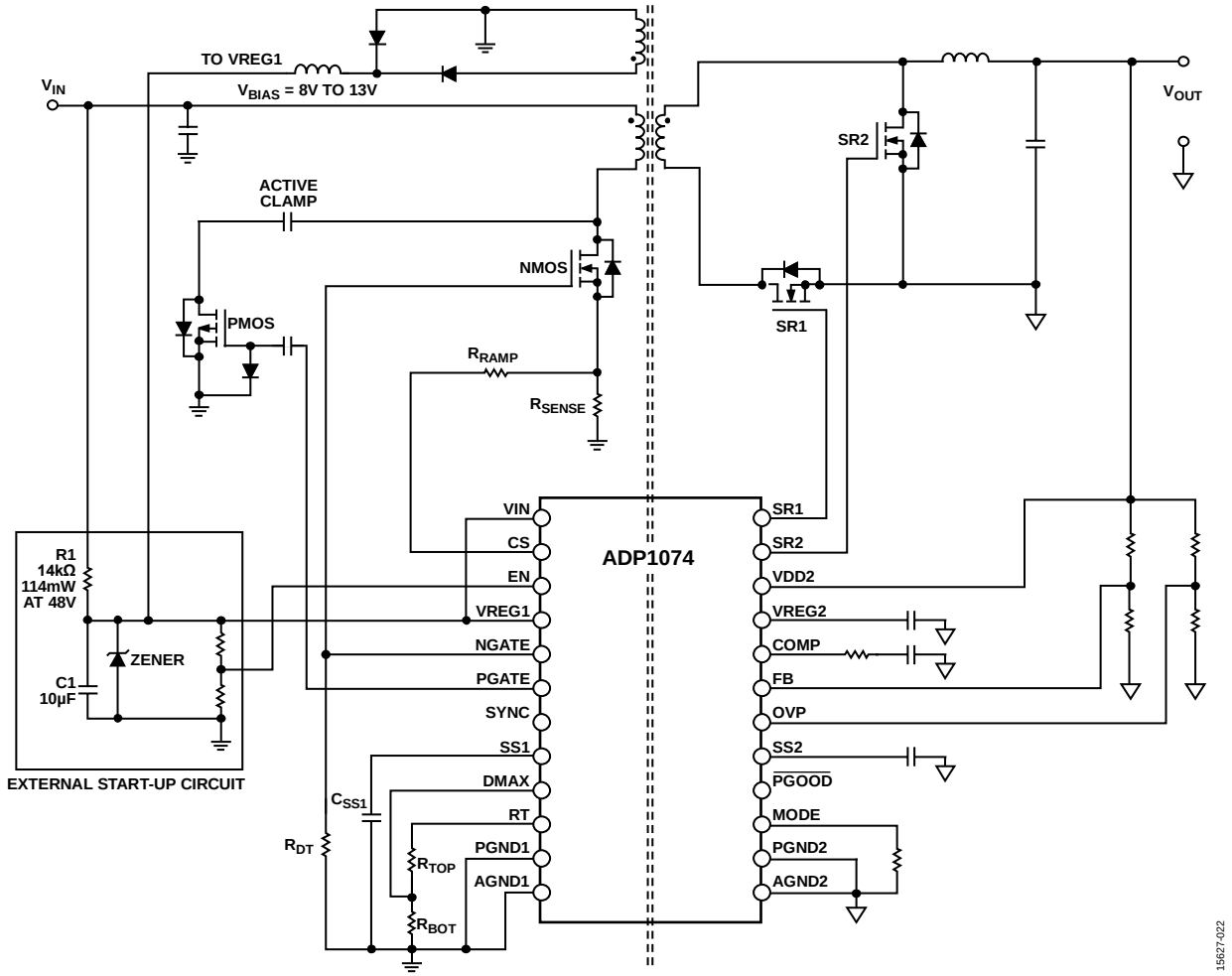

Figure 26. Typical Application Circuit for Active Clamp Forward Topology with Simple Start-Up Circuit and Bias Winding

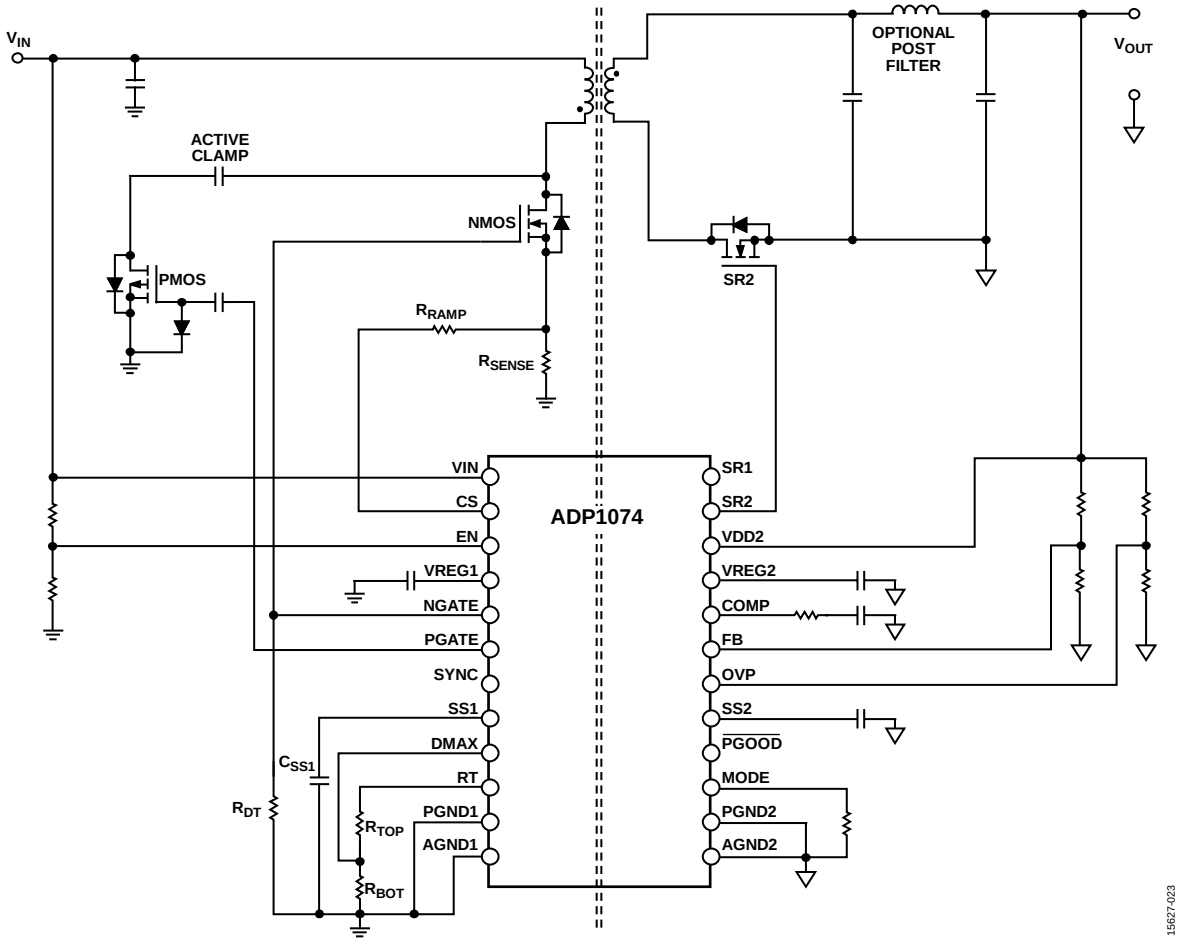

Figure 27. Typical Application Circuit for Active Clamp Flyback Topology

OUTLINE DIMENSIONS

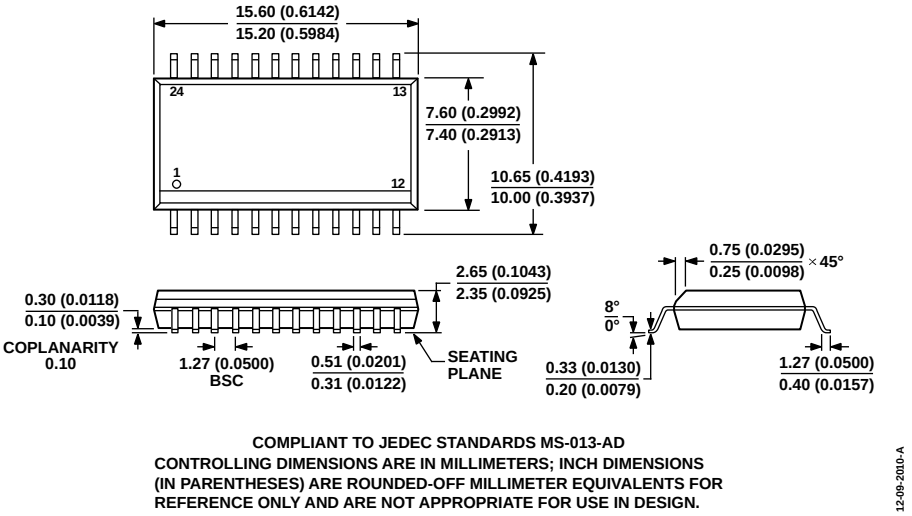

Figure 28. 24-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-24)
Dimensions shown in millimeters and (inches)

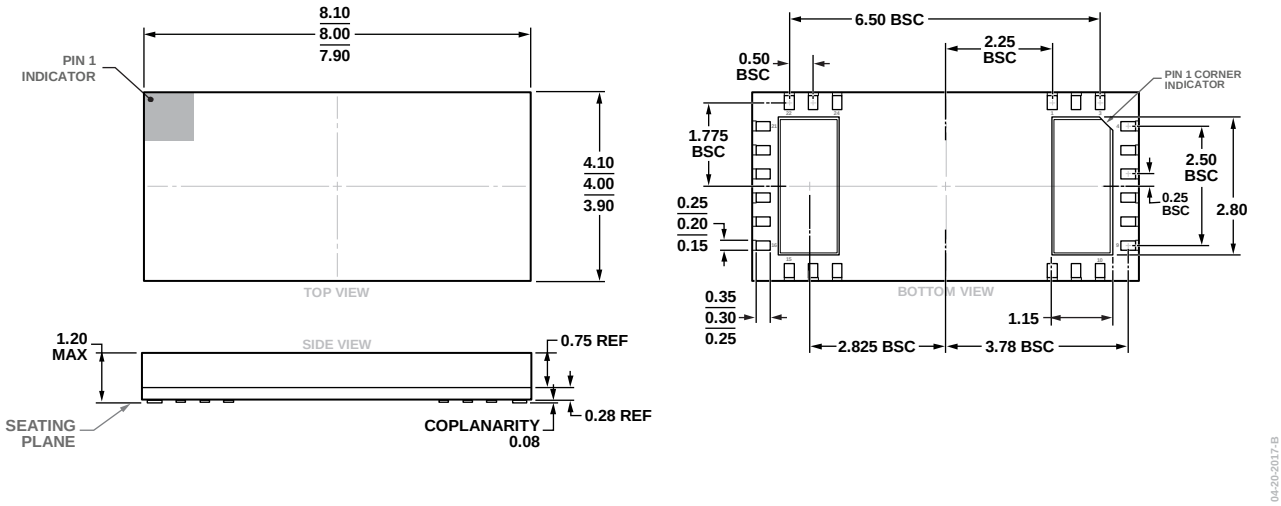

Figure 29. 24-Terminal Land Grid Array [LGA]
(CC-24-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP1074ARWZ	−40°C to +125°C	24-Lead Standard Small Outline Package [SOIC_W]	RW-24
ADP1074ARWZ-RL	−40°C to +125°C	24-Lead Standard Small Outline Package [SOIC_W]	RW-24
ADP1074ARWZ-R7	−40°C to +125°C	24-Lead Standard Small Outline Package [SOIC_W]	RW-24
ADP1074-EVALZ		ADP1074 Evaluation Board with Wide Body IC	
ADP1074ACCZ	−40°C to +125°C	24-Terminal Land Grid Array [LGA]	CC-24-6
ADP1074ACCZ-RL	−40°C to +125°C	24-Terminal Land Grid Array [LGA]	CC-24-6
ADP1074ACCZ-R7	−40°C to +125°C	24-Terminal Land Grid Array [LGA]	CC-24-6
ADP1074LGA-EVALZ		ADP1074 Evaluation Board with LGA IC	

[1] Z = RoHS Compliant Part.

NOTES

D15627-0-8/18(A)