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# FemtoClock® NG QUAD Universal Frequency Translator

# IDT8T49N445I

## DATA SHEET

## General Description

The IDT8T49N445I is a quad PLL with FemtoClock® NG technology. The IDT8T49N445I integrates low phase noise Frequency Translation / Synthesizer and jitter attenuation. It includes alarm and monitoring functions suitable for networking and communications applications. The device has four fully independent PLLs, each PLL is able to generate any output frequency in the 0.98MHz - 312.5MHz range and most output frequencies in the 312.5MHz - 1,300MHz range (see Table 3 for details). A wide range of input reference clocks may be used as the source for the output frequency.

Each PLL of IDT8T49N445I has three operating modes to support a very broad spectrum of applications:

1) Frequency Synthesizer
   - Synthesizes output frequencies from an external reference clock REFCLK.
   - Fractional feedback division is used, so there are no requirements for any specific input reference clock frequency to produce the desired output frequency with a high degree of accuracy.
2) High-Bandwidth Frequency Translator
   - Applications: PCI Express, Computing, General Purpose
   - Translates any input clock in the 16MHz - 710MHz frequency range into any supported output frequency.
   - This mode has a high PLL loop bandwidth in order to track input reference changes, such as Spread-Spectrum Clock modulation.
3) Low-Bandwidth Frequency Translator
   - Applications: Networking & Communications.
   - Translates any input clock in the 8kHz -710MHz frequency range into any supported output frequency.
   - This mode supports PLL loop bandwidths in the 10Hz - 580Hz range and makes use of an external reference clock REFCLK to provide significant jitter attenuation.

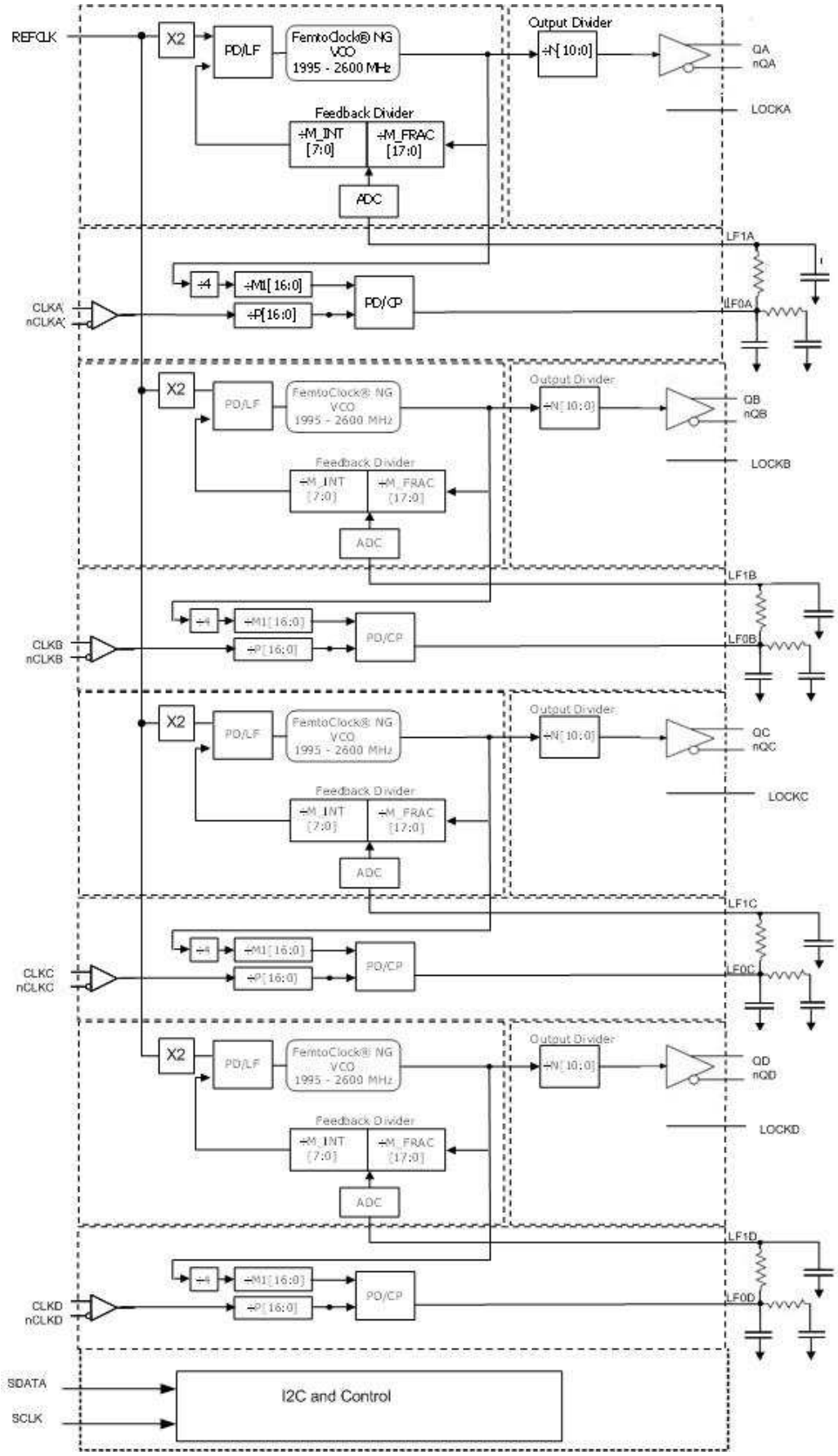
Each PLL provides factory-programmed default power-up configuration burned into One-Time Programmable (OTP) memory. The configuration is specified by the customer and are programmed by IDT during the final test phase from an on-hand stock of blank devices.

To implement other configurations, these power-up default settings can be overwritten after power-up using the $I^2C$ interface and the device can be completely reconfigured.

## Features

- Fourth generation FemtoClock® NG technology
- Four fully independent PLLs
- Universal Frequency Translator™ Frequency Synthesizer and Jitter attenuator
- Output is programmable as LVPECL or LVDS
- Programmable output frequency: 0.98MHz up to 1,300MHz
- Differential inputs support the following input types: LVPECL, LVDS, LVHSTL, HCSL
- Input frequency range: 8kHz - 710MHz (Low-Bandwidth mode)
- Input frequency range: 16kHz - 710MHz (High-Bandwidth mode)
- REFCLK frequency range: 16MHz - 40MHz
- Input clock monitor on each PLL will smoothly switch between redundant input references
- Operation reference frequency range: 16MHz - 40MHz
- Input clock monitor and alarm
- Factory-set register configuration for power-up default state
- Power-up default configuration
- Configuration customized via One-Time Programmable ROM
- Settings may be overwritten after power-up via $I^2C$
- $I^2C$ Serial interface for register programming
- RMS phase jitter at 161.1328125MHz, using 40MHz REFCLK (12kHz - 20MHz): 465fs (typical), Low Bandwidth Mode (FracN)
- RMS phase jitter at 400MHz, using 40MHz REFCLK (12kHz - 20MHz): 333fs (typical), synthesizer Mode (integer FB)
- Full 2.5V supply mode
- -40°C to 85°C ambient operating temperature
- 10mm X 10mm CABGA
- Lead-free (RoHS 6) packaging

# Complete Block Diagram



# Pin Description and Pin Characteristic Tables

**Table 1. Pin Description Table**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| E5 | REFCLK | Input | Pulldown | Reference clock for device operation. LVCMOS/LVTTL interface levels. |
| C2 | CLKA | Input | Pulldown | Non-inverting differential clock input. |
| D2 | nCLKA | Input | Pullup/ Pulldown | Inverting differential clock input. $V_{CC}/2$ default when left floating (set by the internal pullup and pulldown resistors). |
| B7 | CLKB | Input | Pulldown | Non-inverting differential clock input. |
| B6 | nCLKB | Input | Pullup/ Pulldown | Inverting differential clock input. $V_{CC}/2$ default when left floating (set by the internal pullup and pulldown resistors). |
| G8 | CLKC | Input | Pulldown | Non-inverting differential clock input. |
| F8 | nCLKC | Input | Pullup/ Pulldown | Inverting differential clock input. $V_{CC}/2$ default when left floating (set by the internal pullup and pulldown resistors). |
| H3 | CLKD | Input | Pulldown | Non-inverting differential clock input. |
| H4 | nCLKD | Input | Pullup/ Pulldown | Inverting differential clock input. $V_{CC}/2$ default when left floating (set by the internal pullup and pulldown resistors). |
| B1, A2 | QA, nQA | Output | | Differential output. Output type is programmable to LVDS or LVPECL interface levels. |
| A9, B9 | QB, nQB | Output | | Differential output. Output type is programmable to LVDS or LVPECL interface levels. |
| J9, J8 | QC, nQC | Output | | Differential output. Output type is programmable to LVDS or LVPECL interface levels. |
| J1, H1 | QD, nQD | Output | | Differential output. Output type is programmable to LVDS or LVPECL interface levels. |
| A4, A5 | LF0A, LF1A | Analog I/O | | Loop filter connection node pins. LF0A is the output, LF1A is the input. |
| D9, E9 | LF0B, LF1B | Analog I/O | | Loop filter connection node pins. LF0B is the output, LF1B is the input. |
| J6, J5 | LF0C, LF1C | Analog I/O | | Loop filter connection node pins. LF0C is the output, LF1C is the input. |
| F1, E1 | LF0D, LF1D | Analog I/O | | Loop filter connection node pins. LF0D is the output, LF1D is the input. |
| E2 | LOCKA | Output | | Lock Indicator - indicates that the PLL is in a locked condition. LVCMOS/LVTTL interface levels. |
| C5 | LOCKB | Output | | Lock Indicator - indicates that the PLL is in a locked condition. LVCMOS/LVTTL interface levels. |
| E8 | LOCKC | Output | | Lock Indicator - indicates that the PLL is in a locked condition. LVCMOS/LVTTL interface levels. |
| H5 | LOCKD | Output | | Lock Indicator - indicates that the PLL is in a locked condition. LVCMOS/LVTTL interface levels. |
| G6 | SDATA | I/O | Pullup | $I^2C$ Data Input/Output. Open drain. LVCMOS/LVTTL interface levels. |
| G5 | SCLK | Input | Pullup | $I^2C$ Clock Input. LVCMOS/LVTTL interface levels. |
| C1 | $V_{CCA\_A}$ | Power | | Analog power supply for PLLA. |
| C4 | $V_{CCO\_A}$ | Power | | Output power supply for PLLA. |
| B5 | $V_{CC\_A}$ | Power | | Core power supply for PLLA. |
| A7 | $V_{CCA\_B}$ | Power | | Analog power supply for PLLB. |
| D5 | $V_{CCO\_B}$ | Power | | Output power supply for PLLB. |

**Table 1. Pin Description Table**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| D7 | $V_{CC\_B}$ | Power | | Core power supply for PLLB. |
| E7 | $V_{CCA\_C}$ | Power | | Analog power supply for PLLC. |
| G9 | $V_{CCO\_C}$ | Power | | Output power supply for PLLC. |
| F5 | $V_{CC\_C}$ | Power | | Core power supply for PLLC. |
| E3 | $V_{CCA\_D}$ | Power | | Analog power supply for PLLD. |
| J3 | $V_{CCO\_D}$ | Power | | Output power supply for PLLD. |
| F3 | $V_{CC\_D}$ | Power | | Core power supply for PLLD. |
| A3, B2, B3 | $V_{EE\_A}$ | Power | | Negative supply for PLLA. |
| A8, B8, C9 | $V_{EE\_B}$ | Power | | Negative supply for PLLB. |
| H8, H9, J7 | $V_{EE\_C}$ | Power | | Negative supply for PLLC. |
| G1, H2, J2 | $V_{EE\_D}$ | Power | | Negative supply for PLLD. |
| A6, B4, C3, C6, C7, D1, D3, D4, D6, D8, F2, F4, F6, F7, F9, G3, G4, G7, | nc | Unused | | No connect. These pins are to be left unconnected. |
| E6 | Rsvd | Input | | Reserved, connect to $V_{EE.}$ |
| E4 | Rsvd | Input | | Reserved, connect to $V_{EE.}$ |
| C8 | Rsvd | Input | | Reserved, connect to $V_{EE.}$ |
| H7 | Rsvd | Input | | Reserved, connect to $V_{EE.}$ |
| G2 | Rsvd | Input | | Reserved, connect to $V_{EE.}$ |

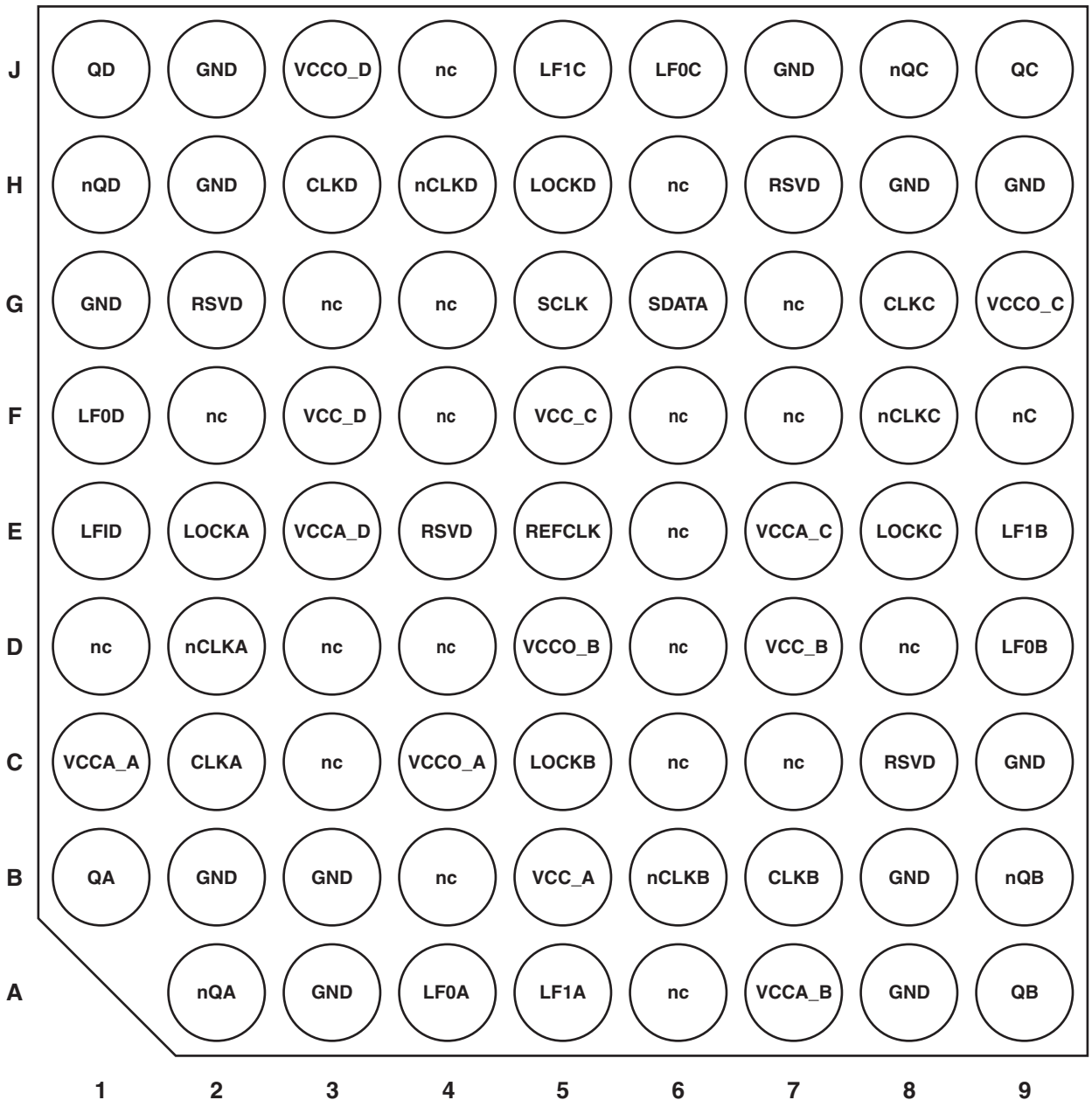
NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

**Table 2. Pin Characteristics**

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | | 3.5 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | REFCLK | | | 12.5 | | kΩ |
| $R_{PULLUP}$ | Input Pullup Resistor | SDATA, SCLK | | | 12.5 | | kΩ |

# Pin Assignment




**IDT8T49N445I Pin Map**

80-Ball Lead
10mm x 10mm x1mm package body
CABGA Package
(bottom view)

# Functional Description

The IDT8T49N445I is a 4-PLL device. The 4 PLLs are fully independent and identical. Each PLL can generate desired output frequency (0.98 - 1300MHz) from any input source in the operating range (8kHz - 710MHz). It is capable of synthesizing frequencies from REFCLK source. The output frequency is generated regardless of the relationship to the input frequency. Each PLL of IDT8T49N445I can translate the desired output frequency from input clock. In this frequency translation mode, a low-bandwidth, jitter attenuation option is available that makes use of an external fixed-frequency REFCLK to translate from a noisy input source. If the input clock is known to be fairly clean or if some modulation on the input needs to be tracked, then the high-bandwidth frequency translation mode can be used, without the need for the external clock source.

The input clock references and REFCLK input are monitored continuously and appropriate alarm outputs are raised by register bits and hard-wired pins in the event of any out-of-specification conditions arising.

Each PLL of IDT8T49N445I has factory-programmed configuration as the default operating state after reset. These defaults may be over-written by $I^2C$ register access at any time, but those over-written settings will be lost on power-down. Please contact IDT if a specific set of power-up default settings is desired.

The following sections apply individually to each PLL. Signal and register bit names have a lowercase ‘x’ on the end where ‘x’ should be ‘A’, ‘B’, ‘C’ or ‘D’ as appropriate for the PLL being controlled.

## Operating Modes

Each PLL of IDT8T49N445I has three operating modes which are set by the MODE_SEL[1:0] bits. There are two frequency translator modes - low bandwidth and high bandwidth and a frequency synthesizer mode.

Please make use of IDT-provided configuration applications to determine the best operating settings for the desired configuration of the device.

### Output Dividers & Supported Output Frequencies

The internal VCO is capable of operating in a range anywhere from 1.995GHz - 2.6GHz. It is necessary to choose an integer multiplier of the desired output frequency that results in a VCO operating frequency within that range. The output divider stage N[10:0] is limited to selection of integers from 2 to 2046. Please refer to Table 3 for the values of N applicable to the desired output frequency.

**Table 3. Output Divider Settings & Frequency Ranges**

| Register Setting | Frequency Divider | Minimum $f_{OUT}$ | Maximum $f_{OUT}$ |
|---|---|---|---|
| Nn[10:0] | N | (MHz) | (MHz) |
| 0000000000x | 2 | 997.5 | 1300 |
| 00000000010 | 2 | 997.5 | 1300 |
| 00000000011 | 3 | 665 | 866.7 |
| 00000000100 | 4 | 498.75 | 650 |
| 00000000101 | 5 | 399 | 520 |
| 0000000011x | 6 | 332.5 | 433.3 |
| 0000000100x | 8 | 249.4 | 325 |
| 0000000101x | 10 | 199.5 | 260 |
| 0000000110x | 12 | 166.3 | 216.7 |
| 0000000111x | 14 | 142.5 | 185.7 |
| 0000001000x | 16 | 124.7 | 162.5 |
| 0000001001x | 18 | 110.8 | 144.4 |
| ... | Even N | 1995 / N | 2600 / N |
| 1111111111x | 2046 | 0.98 | 1.27 |

### Frequency Synthesizer Mode

This mode of operation allows an arbitrary output frequency to be generated from a external clock source. For improved phase noise performance, this input frequency is doubled. As can be seen from the block diagram in *Figure 1,* only the upper feedback loop is used in this mode of operation. It is recommended that CLK be left unused in this mode of operation.

The upper feedback loop supports a delta-sigma fractional feedback divider. This allows the VCO operating frequency to be a non-integer multiple of the REFCLK frequency. By using an integer multiple only, lower phase noise jitter on the output can be achieved, however the use of the delta-sigma divider logic will provide excellent performance on the output if a fractional divisor is used.

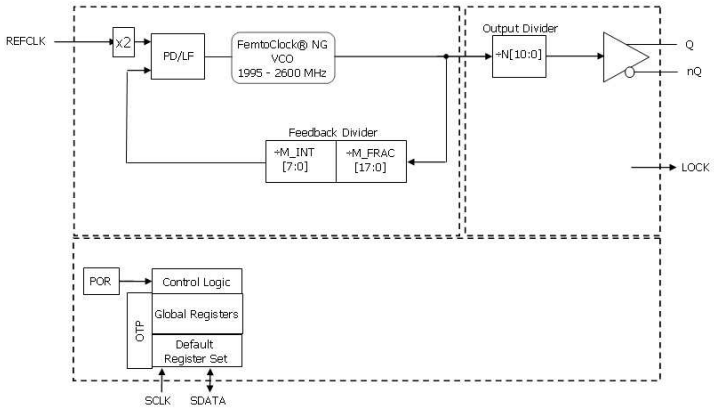



**Figure 1. Frequency Synthesizer Mode Block Diagram**

### High-Bandwidth Frequency Translator Mode

This mode of operation is used to translate input clock of the same nominal frequency into an output frequency with little jitter attenuation. As can be seen from the block diagram in Figure 2, similarly to the Frequency Synthesizer mode, only the upper feedback loop is used.

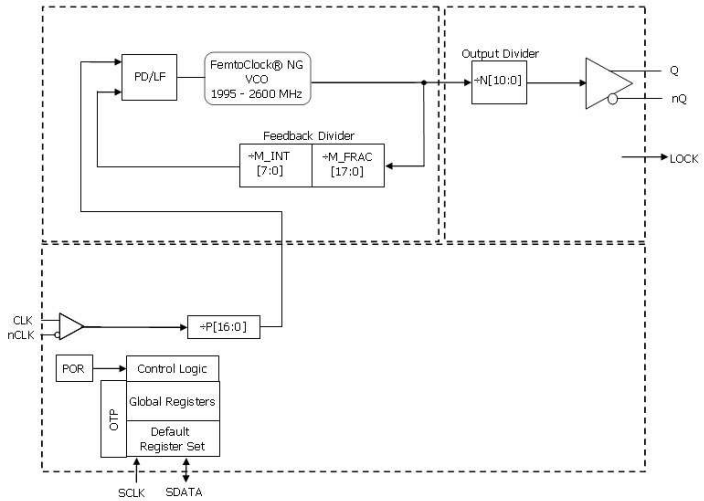



**Figure 2. High Bandwidth Frequency Translator Mode Block Diagram**

The input reference frequency range is now extended up to 710MHz. A pre-divider stage P is needed to keep the operating frequencies at the phase detector within limits.

### Low-Bandwidth Frequency Translator Mode

As can be seen from the block diagram in Figure 3, this mode involves two PLL loops. The lower loop with the large integer dividers is the low bandwidth loop and it sets the output-to-input frequency translation ratio.This loop drives the upper DCXO loop (digitally controlled crystal oscillator) via an analog-digital converter.

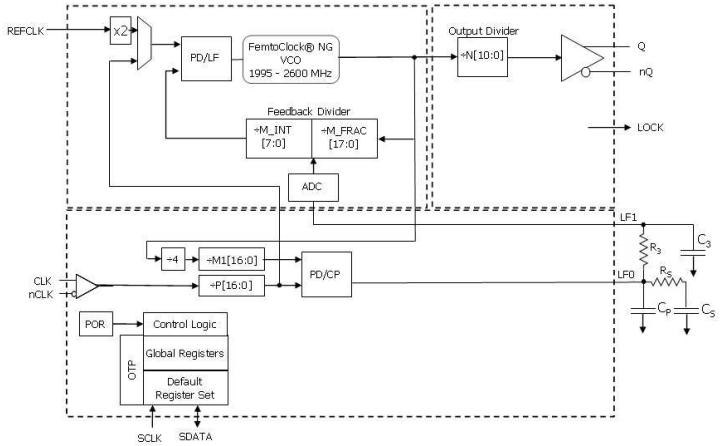



**Figure 3. Low Bandwidth Frequency Translator Mode Block Diagram**

The phase detector of the lower loop is designed to work with frequencies in the 8kHz - 16kHz range. The pre-divider stage is used to scale down the input frequency by an integer value to achieve a frequency in this range. By dividing down the fed-back VCO operating frequency by the integer divider M1[18:0] to as close as possible to the same frequency, exact output frequency translations can be achieved.

## Alarm Conditions & Status Bits

Each PLL of IDT8T49N445I monitors a number of conditions and reports their status via both output pins and/or register bits. All alarms will behave as indicated below in all modes of operation, but some of the conditions monitored have no valid meaning in some operating modes. For example, the status of CLKBAD is not relevant in Frequency Synthesizer mode. The outputs will still be active and it is left to the user to determine

LOCK - This status is asserted on the pin & register bit when the PLL is locked to the appropriate input reference for the chosen mode of operation. The status bit will not assert until frequency lock has been achieved, but will de-assert once lock is lost.

REFBAD - indicates if valid edges are being received on the REFCLK input. Detection is performed by comparing the input to the feedback signal at the upper loop's Phase / Frequency Detector (PFD). If three edges are received on the feedback without an edge on the REFCLK input, the REFBAD alarm is asserted on the pin & register bit. Once an edge is detected on the REFCLK input, the alarm is immediately deasserted.

CLKBAD - indicates if valid edges are being received on the CLK reference input. Detection is performed by comparing the input to the feedback signal at the appropriate Phase / Frequency Detector (PFD). When operating in high-bandwidth mode, the feedback at the upper PFD is used. In low-bandwidth mode, the feedback at the lower PFD is used. If three edges are received on the feedback without an edge on the divided down (÷P) CLK reference input, the CLKBAD alarm is asserted on the pin & register bit. Once an edge is detected on the CLK reference input, the alarm is deasserted.

### Holdover / Free-run Behavior

When input reference has failed, the PLL will enter holdover (Low Bandwidth Frequency Translator mode) or free-run (High Bandwidth Frequency Translator mode) state if. In both cases, once the input reference is lost, the PLL will stop making adjustments to the output phase.

If operating in Low Bandwidth Frequency Translation mode, the PLL will continue to reference itself to the local oscillator and will hold its output phase and frequency in relation to that source. Output stability is determined by the stability of the local oscillator in this case.

However, if operating in High Bandwidth Frequency Translation mode, the PLL no longer has any frequency reference to use and output stability is now determined by the stability of the internal VCO.

## Output Configuration

The output is selectable as LVDS or LVPECL output types via the Q_TYPE register bit. The output can be enabled via register control bit. When both the OE register bit is enabled, then the output is enabled. When the differential output is in the disabled state, it will show a high impedance condition.

## Serial Interface Configuration Description

The IDT8T49N445I has an $I^2C$-compatible configuration interface to access any of the internal registers (Table 4D). Each PLL acts as slave device on the $I^2C$ bus and has the address 0b11011xx, where the xx is fixed values as Table 4A (see Table 4A for details). The interface accepts byte-oriented block write and block read operations. An address byte (P) specifies the register address (Table 4D) as the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first, see Table 4B, 4C). Read and write block transfers can be stopped after any complete byte transfer. It is recommended to terminate $I^2C$ the read or write transfer after accessing byte #23 of each PLL.

For full electrical $I^2C$ compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 50kΩ typical.

Note: if a different device slave address is desired, please contact IDT.

**Table 4A. $I^2C$ Device Slave Address**

| | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|---|---|---|---|---|---|---|---|---|
| **PLL-A** | 1 | 1 | 0 | 1 | 1 | 0 | 0 | R/W |
| **PLL-B** | 1 | 1 | 0 | 1 | 1 | 0 | 1 | R/W |
| **PLL-C** | 1 | 1 | 0 | 1 | 1 | 1 | 0 | R/W |
| **PLL-D** | 1 | 1 | 0 | 1 | 1 | 1 | 1 | R/W |

**Table 4B. Block Write Operation**

| **Bit** | **1** | **2:8** | **9** | **10** | **11:18** | **19** | **20:27** | **28** | **29-36** | **37** | **...** | **...** | **...** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Description** | START | Slave Address | W (0) | ACK | Address Byte (P) | ACK | Data Byte (P) | ACK | Data Byte (P+1) | ACK | Data Byte ... | ACK | STOP |
| **Length (bits)** | 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |

**Table 4C. Block Read Operation**

| Bit | 1 | 2:8 | 9 | 10 | 11:18 | 19 | 20 | 21:27 | 28 | 29 | 30:37 | 38 | 39-46 | 47 | ... | ... | ... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Description** | START | Slave Address | W (0) | ACK | Address Byte (P) | ACK | Repeated START | Slave Address | R (1) | ACK | Data Byte (P) | ACK | Data Byte (P+1) | ACK | Data Byte ... | ACK | STOP |
| **Length (bits)** | 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |

# Register Descriptions

Please consult IDT for configuration software and/or programming guides to assist in selection of optimal register settings for the desired configurations. The below register map table applies to each PLL.

**Table 4D. I²C Register Map**

| Reg | Binary Register Address | Register Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 00000 | MFRACx[17] | MFRACx[16] | MFRACx[15] | MFRACx[14] | MFRACx[13] | MFRACx[12] | MFRACx[11] | MFRACx[10] |
| 1 | 00001 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD |
| 2 | 00010 | MFRACx[9] | MFRACx[8] | MFRACx[7] | MFRACx[6] | MFRACx[5] | MFRACx[4] | MFRACx[3] | MFRACx[2] |
| 3 | 00011 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD |
| 4 | 00100 | MFRACx[1] | MFRACx[0] | MINTx[7] | MINTx[6] | MINTx[5] | MINTx[4] | MINTx[3] | MINTx[2] |
| 5 | 00101 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD |
| 6 | 00110 | MINTx[1] | MINTx[0] | Px[16] | Px[15] | Px[14] | Px[13] | Px[12] | Px[11] |
| 7 | 00111 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD |
| 8 | 01000 | Px[10] | Px[9] | Px[8] | Px[7] | Px[6] | Px[5] | Px[4] | Px[3] |
| 9 | 01001 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD |
| 10 | 01010 | Px[2] | Px[1] | Px[0] | M1_x[16] | M1_x[15] | M1_x[14] | M1_x[13] | M1_x[12] |
| 11 | 01011 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD |
| 12 | 01100 | M1_x[11] | M1_x[10] | M1_x[9] | M1_x[8] | M1_x[7] | M1_x[6] | M1_x[5] | M1_x[4] |
| 13 | 01101 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD |
| 14 | 01110 | M1_x[3] | M1_x[2] | M1_x[1] | M1_x[0] | Nx[10] | Nx[9] | Nx[8] | Nx[7] |
| 15 | 01111 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD |
| 16 | 10000 | Nx[6] | Nx[5] | Nx[4] | Nx[3] | Nx[2] | Nx[1] | Nx[0] | BWx[6] |
| 17 | 10001 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD |
| 18 | 10010 | BWx[5] | BWx[4] | BWx[3] | BWx[2] | BWx[1] | BWx[0] | Rsvd | Q_TYPEx |
| 19 | 10011 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD |
| 20 | 10100 | MODE_SELx[1] | MODE_SELx[0] | 0 | 1 | 0 | OEx | Rsvd | Rsvd |
| 21 | 10101 | 0 | 1 | 1 ] | 0 | ADC_RATEx[1] | ADC_RATEx[0] | LCK_WINx[1] | LCK_WINx[0] |
| 22 | 10110 | 1 | 0 | 1 | 0 | DBL_REFCLKx | 0 | 0 | 1 |
| 23 | 10111 | Rsvd | HOLDOVERx | Rsvd | CLKBADx | REFBADx | LOCKx | Rsvd | Rsvd |

NOTE: “x” denotes A, B, C or D.

**Table 4E. Configuration-Specific Control Bits**

| Register Bits | Function |
|---|---|
| Q_TYPEx | Determines the output type for output pair Q, nQ for PLLx.<br>0 = LVPECL<br>1 = LVDS |
| Px[16:0] | Reference Pre-Divider. |
| M1_x[16:0] | Integer Feedback Divider for PLLx in Lower Feedback Loop. |
| M_INTx[7:0] | Feedback Divider, Integer Value in Upper Feedback Loop for PLLx. |
| M_FRACx[17:0] | Feedback Divider, Fractional Value in Upper Feedback Loop for PLLx. |
| Nx[10:0] | Output Divider for PLLx. |
| BWx[6:0] | Internal Operation Settings for PLLx.<br>Please use IDT IDT8T49N445I Configuration Software to determine the correct settings for these bits for the specific configuration. Alternatively, please consult with IDT directly for further information on the functions of these bits.The function of these bits are explained in Tables 4J and 4K. |
| MODE_SELx[1:0] | PLL Mode Select for PLLx.<br>00 = Low Bandwidth Frequency Translator<br>01 = Frequency Synthesizer<br>10 = High Bandwidth Frequency Translator<br>11 = High Bandwidth Frequency Translator |
| OEx | Output Enable Control for Output for PLLx.<br>0 = Output Q, nQ disabled<br>1 = Output Q, nQ enabled |
| Rsvd | Reserved bits - user should write a ‘0’ to these bit positions if a write to these registers is needed. |
| ADC_RATEx1:0] | Sets the ADC sampling rate in Low-Bandwidth Mode as a fraction of the REFCLK input frequency for PLLx.<br>00 = REFCLK Frequency / 16 if doubler is disabled<br>01 = REFCLK Frequency / 8 if doubler is disabled<br>10 = REFCLK Frequency / 4 if doubler is disabled(recommended)<br>11 = REFCLK Frequency / 2 if doubler is disabled |
| LCK_WINx[1:0] | Sets the width of the window in which a new reference edge must fall relative to the feedback edge for PLLx.<br>00 = 2usec (recommended), 01 = 4usec, 10 = 8usec, 11 = 16usec |
| DBL_REFCLKx | When set, this bit will double the frequency of the REFCLK input before applying it to the Phase-Frequency Detector for PLLx. |

**Table 4F. Global Status Bits**

| Register Bits | Function |
|---|---|
| CLKBADx | Status Bit for input clock for PLLx.<br>0 = input good<br>1 = input bad. Self clears when input clock returns to good status |
| REFBADx | Status Bit.<br>0 = REFCLK input good<br>1 = REFCLK input bad. Self-clears for PLLx when the REFCLK returns to good status |
| LOCKx | Status bit. This function is mirrored on the LOCK pin for PLLx.<br>0 = PLL unlocked<br>1 = PLL locked |
| HOLDOVERx | Status Bit for PLLx.<br>0 = Input to phase detector is within specifications and device is tracking to it<br>1 = Phase detector input not within specifications and DCXO is frozen at last value |

**Table 4G. BWx[6:0] Bits**

| Mode | BWx[6] | BWx[5] | BWx[4] | BWx[3] | BWx[2] | BWx[1] | BWx[0] |
|---|---|---|---|---|---|---|---|
| Synthesizer Mode | PLL2_LFx[1] | PLL2_LFx[0] | DSM_ORDx | DSM_ENx | PLL2_CPx[1] | PLL2_CPx[0] | PLL2_LOW_LCPx |
| High-Bandwidth Mode | PLL2_LFx[1] | PLL2_LFx[0] | DSM_ORDx | DSM_ENx | PLL2_CPx[1] | PLL2_CPx[0] | PLL2_LOW_LCPx |
| Low-Bandwidth Mode | ADC_GAINx[3] | ADC_GAINx[2] | ADC_GAINx[1] | ADC_GAINx[0] | PLL1_CPx[1] | PLL1_CPx[0] | PLL2_LOW_LCPpx |

**Table 4H. Functions of Fields in BW[6:0]**

| Register Bits | Function |
|---|---|
| PLL2_LFx[1:0] | Sets loop filter values for upper loop PLL in Frequency Synthesizer & High-Bandwidth modes for PLLx. Defaults to setting of 00 when in Low Bandwidth Mode. See Table 4I for settings. |
| DSM_ORDx | Sets Delta-Sigma Modulation to 2nd (0) or 3rd order (1) operation. |
| DSM_ENx | Enables Delta-Sigma Modulator for PLLx.<br>0 = Disabled - feedback in integer mode only<br>1 = Enabled - feedback in fractional mode |
| PLL2_CPx[1:0] | Upper loop PLL charge pump current settings for PLLx:<br>00 = 173µA (defaults to this setting in Low Bandwidth Mode)<br>01 = 346µA<br>10 = 692µA<br>11 = reserved |
| PLL2_LOW_LCPx | Reduces Charge Pump current by 1/3 to reduce bandwidth variations resulting from higher feedback register settings or high VCO operating frequency (>2.4GHz) for PLLx. |
| ADC_GAINx[3:0] | Gain setting for ADC in Low Bandwidth Mode for PLLx. |
| PLL1_CPx[1:0] | Lower loop PLL charge pump current settings (lower loop is only used in Low Bandwidth Mode) for PLLx:<br>00 = 800µA<br>01 = 400µA<br>10 = 200µA<br>11 = 100µA |

**Table 4I. Upper Loop (PLL2) Bandwidth Settings**

| Desired Bandwidth | PLL2_CP | | PLL2_LOW_ICP | PLL2_LF | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Frequency Synthesizer Mode** | | | | | | | | | |
| 200kHz | 00 | | 1 | 00 | | | | | |
| 400kHz | 01 | | 1 | 01 | | | | | |
| 800kHz | 10 | | 1 | 10 | | | | | |
| 2MHz | 10 | | 1 | 11 | | | | | |
| **High Bandwidth Frequency Translator Mode** | | | | | | | | | |
| 200kHz | 00 | | 1 | 00 | | | | | |
| 400kHz | 01 | | 1 | 01 | | | | | |
| 800kHz | 10 | | 1 | 10 | | | | | |
| 4MHz | 10 | | 0 | 11 | | | | | |

NOTE: To achieve 4MHz bandwidth, reference to the phase detector should be 80MHz.

# Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{CC\_x}$ | 3.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC\_X}$ + 0.5V |
| Outputs, $V_O$ (LVCMOS) | -0.5V to $V_{CC\_X}$ + 0.5V |
| Outputs, $I_O$ (LVPECL)<br>Continuous Current<br>Surge Current | <br>50mA<br>100mA |
| Outputs, $I_O$ (LVDS)<br>Continuous Current<br>Surge Current | <br>10mA<br>15mA |
| Package Thermal Impedance, $\theta_{JA}$ | 12.4°C/W (0mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

# DC Electrical Characteristics

**Table 5A. LVPECL Power Supply DC Characteristics,** $V_{CC\_X} = V_{CCO\_X} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC\_X}$ | Core Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{CCA\_X}$ | Analog Supply Voltage | | $V_{CC\_X}$ – 0.26 | 2.5 | $V_{CC\_X}$ | V |
| $V_{CCO\_X}$ | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{EE}$ | Power Supply Current | | | | 1151 | mA |
| $I_{CCA}$ | Analog Supply Current | | | | 104 | mA |

NOTE: X denotes: A, B, C or D.

**Table 5B. LVDS Power Supply DC Characteristics,** $V_{CC\_X} = V_{CCO\_X} = 2.5V \pm 5\%$, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC\_X}$ | Core Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{CCA\_X}$ | Analog Supply Voltage | | $V_{CC\_X}$ – 0.26 | 2.5 | $V_{CC\_X}$ | V |
| $V_{CCO\_X}$ | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{EE}$ | Power Supply Current | | | | 979 | mA |
| $I_{CCA}$ | Analog Supply Current | | | | 104 | mA |
| $I_{CCO}$ | Output Supply Current | | | | 88 | mA |

NOTE: X denotes: A, B, C or D.

**Table 5C. LVCMOS/LVTTL DC Characteristics,** $V_{CC\_X} = V_{CCO\_X} = 2.5V±5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 1.7 | | $V_{CCx} + 0.3$ | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.7 | V |
| $I_{IH}$ | Input High Current; NOTE 1 | REFCLK | $V_{CC\_X} = V_{IN} = 2.625V$ | | | 150 | µA |
| | | SCLK, SDATA | $V_{CC\_X} = V_{IN} = 2.625V$ | | | 5 | µA |
| $I_{IL}$ | Input Low Current; NOTE 1 | REFCLK | $V_{CC\_X} = 2.625V$, $V_{IN} = 0V$ | -5 | | | µA |
| | | SCLK, SDATA | $V_{CC\_X} = 2.625V$, $V_{IN} = 0V$ | -150 | | | µA |
| $V_{OH}$ | Output High Voltage | SDATA, LOCK[A:D] | $V_{CCO\_X} = 2.625V$ $I_{OH} = -8mA$ | 1.8 | | | V |
| $V_{OL}$ | Output Low Voltage | SDATA, LOCK[A:D] | $V_{CCO\_X} = 2.625V$ $I_{OL} = 8mA$ | | | 0.5 | V |

NOTE1: For REFCLK/SCLK/SDATA pins, specification is for each individual PLL and is guaranteed by design. Production Test is performed all PLLs combined.
NOTE: X denotes: A, B, C or D.

**Table 5D. Differential DC Characteristics,** $V_{CC\_X} = 2.5V±5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | CLK[A:D], nCLK[A:D] | $V_{CC\_X} = V_{IN} = 2.625V$ | | | 150 | µA |
| $I_{IL}$ | Input Low Current | CLK[A:D] | $V_{CC\_X} = 2.625V$, $V_{IN} = 0V$ | -5 | | | µA |
| | | nCLK[A:D] | $V_{CC\_X} = 2.625V$, $V_{IN} = 0V$ | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Voltage | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1 | | | $V_{EE} + 0.5$ | | $V_{CCX} – 0.85$ | V |

NOTE: X denotes: A, B, C or D.
NOTE 1: Common mode input voltage is defined at the crosspoint.

**Table 5E. LVPECL DC Characteristics,** $V_{CCO\_X} = 2.5V±5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CCO\_X} – 1.1$ | | $V_{CCO\_X} – 0.7$ | V |
| $V_{OL}$ | Output Low Voltage NOTE 1 | | $V_{CCO\_X} – 2.0$ | | $V_{CCO\_X} – 1.5$ | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE: X denotes: A, B, C or D.
NOTE 1: Outputs terminated with 50Ω to $V_{CCO\_X} – 2V$.

**Table 5F. LVDS DC Characteristics,** $V_{CCO\_X}$ = 2.5V ± 5%, $V_{EE}$ = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential Output Voltage | | 247 | | 454 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change | | | | 50 | mV |
| $V_{OS}$ | Offset Voltage | | 1.125 | | 1.375 | V |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change | | | | 50 | mV |

NOTE: X denotes: A, B, C or D.

**Table 6. Input Frequency Characteristics,** $V_{CC\_X}$ = 2.5V ± 5%, $V_{EE}$ = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Frequency | REFCLK; NOTE 1 | | 16 | | 40 | MHz |
| | | CLK[A:D], nCLK[A:D | High Bandwidth Mode | 16 | | 710 | MHz |
| | | | Low Bandwidth Mode | 0.008 | | 710 | MHz |
| | | SCLK | | | | 5 | MHz |

NOTE: X denotes: A, B, C or D.
NOTE 1: For the input REFCLK and CLK, nCLK frequency range, the M value must be set for the VCO to operate within the 1995MHz to 2600MHz range.

# AC Electrical Characteristics

**Table 7. AC Characteristics,** $V_{CC\_X} = V_{CCO\_X} = 2.5V±5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$*.

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | | | 0.98 | | 1300 | MHz |
| $f_{VCO}$ | VCO Frequency | | | 1995 | | 2600 | MHz |
| $t_{jit}(Ø)$ | RMS Phase Jitter (Random), Integer Divide Ratio NOTE 1 | | Synth Mode (Integer FB), $f_{OUT}$ = 400MHz, 40MHz REFCLK, Integration Range: 12kHz – 20MHz | | 333 | 435 | fs |
| | | | Synth Mode (FracN FB), $f_{OUT}$ = 698.81MHz, 40MHz REFCLK, Integration Range: 12kHz – 20MHz | | 408 | 665 | fs |
| | | | HBW Mode, $f_{IN}$ = 133.33MHz, $f_{OUT}$ = 400MHz, Integration Range: 12kHz – 20MHz | | 338 | 490 | fs |
| | | | LBW Mode (near integer), 40MHz REFCLK, $f_{IN}$ = 19.44MHz, $f_{OUT}$ = 622.08MHz, Integration Range: 12kHz – 20MHz | | 444 | 680 | fs |
| | | | LBW Mode (FracN), 40MHz REFCLK, $f_{IN}$ = 25MHz, $f_{OUT}$ = 161.1328125MHz, Integration Range: 12kHz – 20MHz | | 465 | 680 | fs |
| $t_{jit}(cc)$ | Cycle-to-Cycle Jitter; NOTE 2, 3 | | Frequency Synthesizer Mode | | | 35 | ps |
| | | | Frequency Translator Mode | | | 40 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time; NOTE 3 | LVPECL Outputs | 20% to 80% | 100 | | 520 | ps |
| | | LVDS Outputs | 20% to 80% | 100 | | 520 | ps |
| odc | Output Duty Cycle; NOTE 3 | | $f_{OUT}$ < 600MHz | 45 | | 55 | % |
| | | | $f_{OUT} \geq$ 600MHz | 40 | | 60 | % |

NOTE: X denotes: A, B, C or D..

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

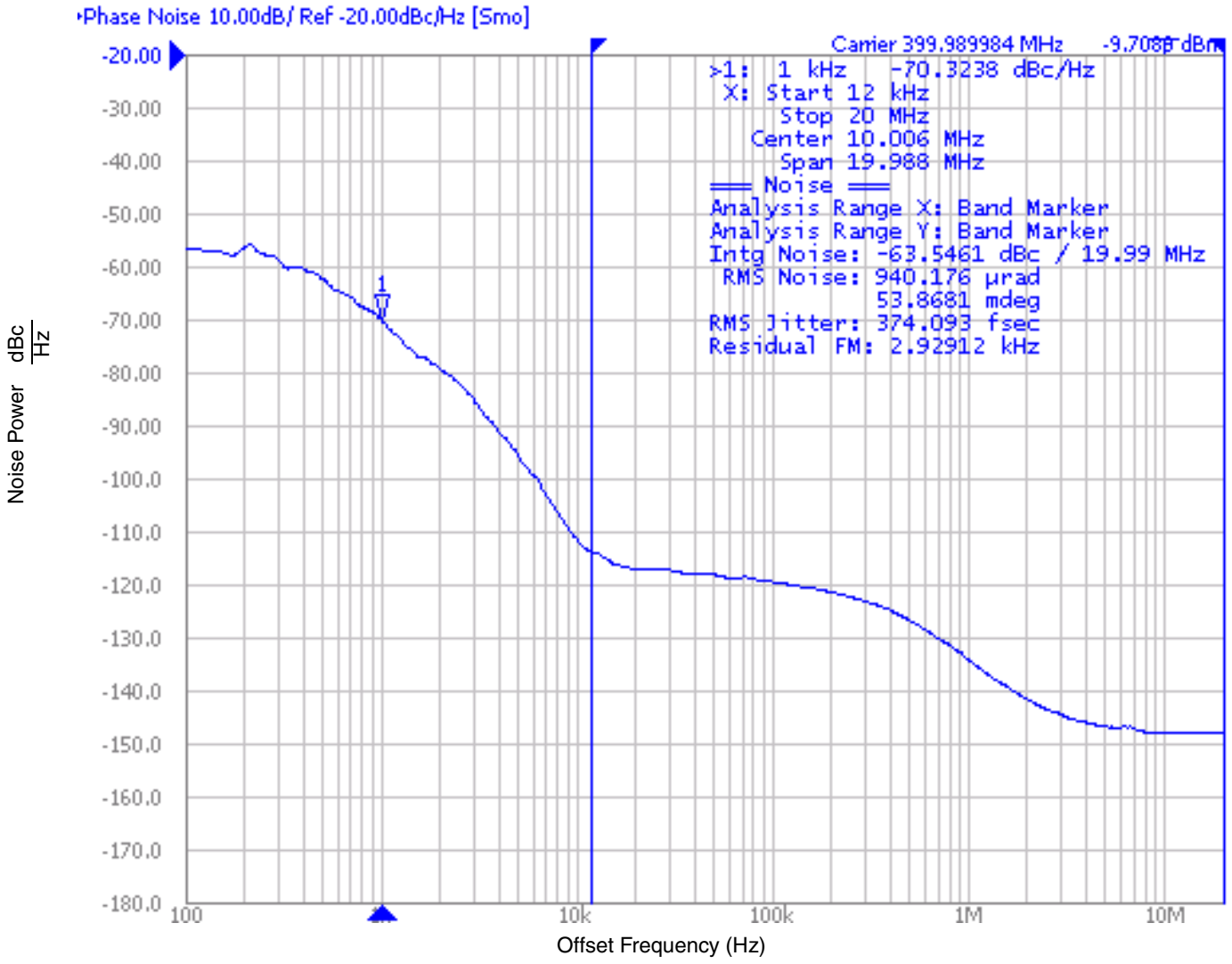
NOTE 1: For RMS Phase Jitter measurement in Synth and HBW mode, all four PLLs are programmed with the same configuration. For the LBW mode. only the PLL under test is programmed with LBW configuration, the other PLLs are programmed with Synth mode with the same output frequency. A Rohde & Schwarz SMA-100 signal generator, 9kHz – 6GHz, is used as the REFCLK source. All configurations are with DBL_REFCLK bit set to 1.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Measurements are collected with the following output frequency: 66.6667MHz, 125MHz, 156.25MHz, 161.138125MHz, 400MHz, 622.08MHz, 698.81MHz, 1300MHz.

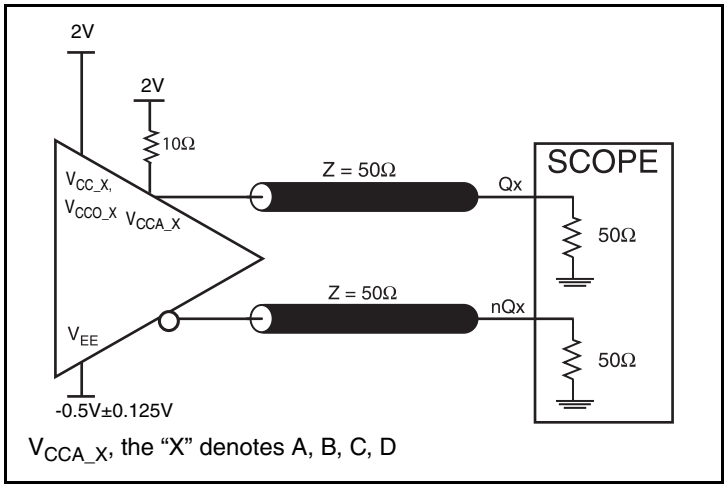
 

## Typical Phase Noise at 400MHz (HBW Mode)

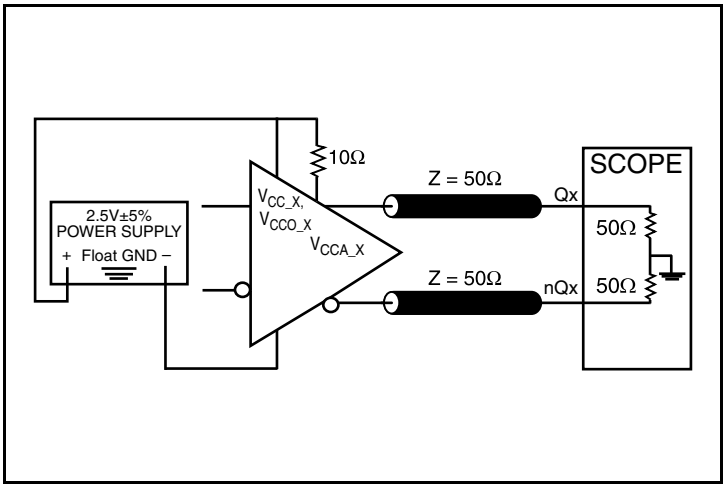


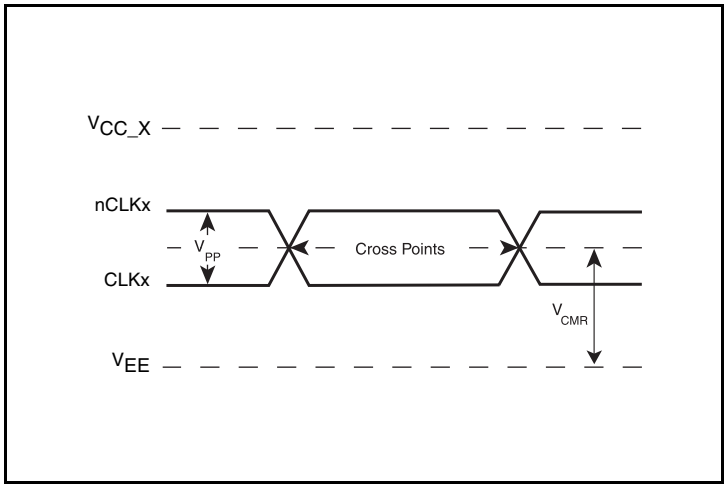
# Parameter Measurement Information



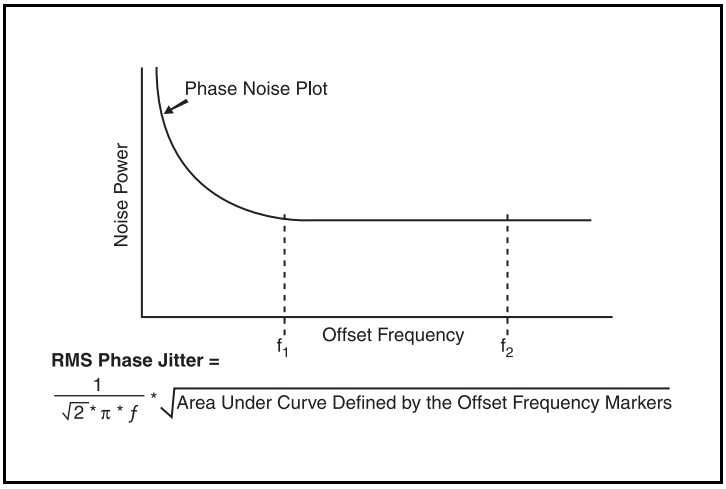

**2.5V LVPECL Output Load Test Circuit**



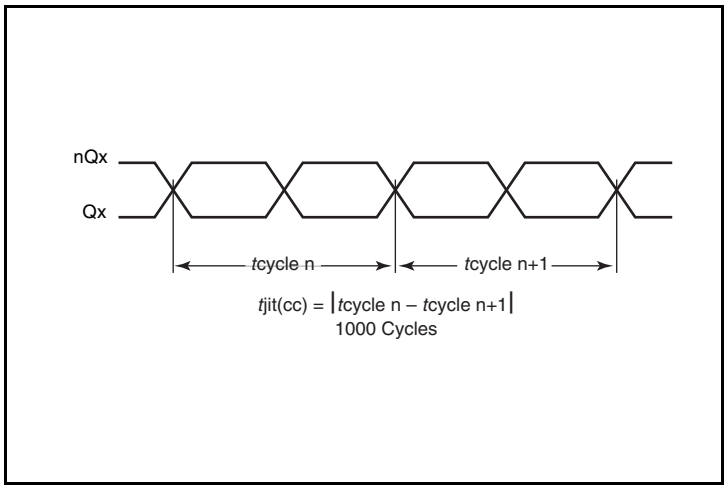

**2.5V LVDS Output Load Test Circuit**



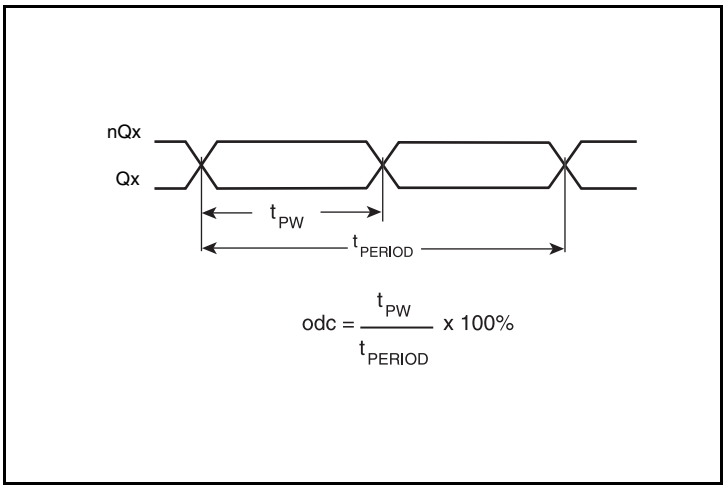

**Differential Input Levels**




**RMS Phase Jitter**



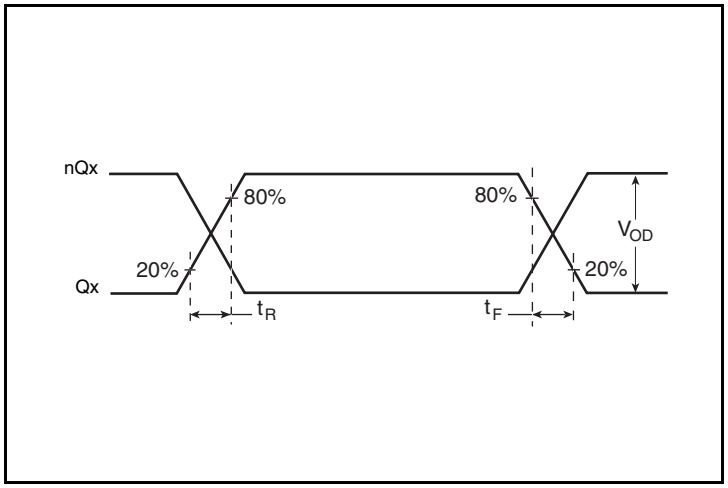

**Cycle-to-Cycle Jitter**



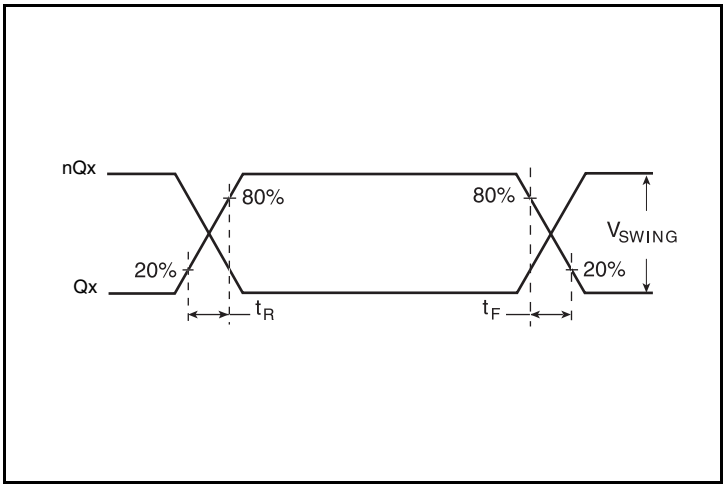

**Output Duty Cycle/Pulse Width/Period**

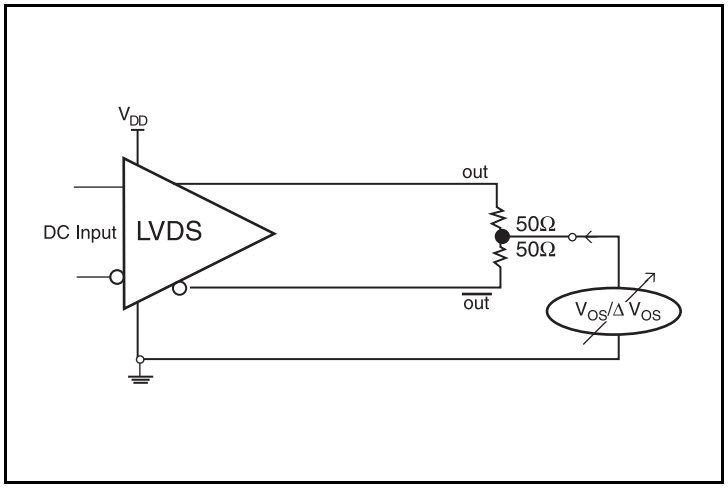
## Parameter Measurement Information, continued



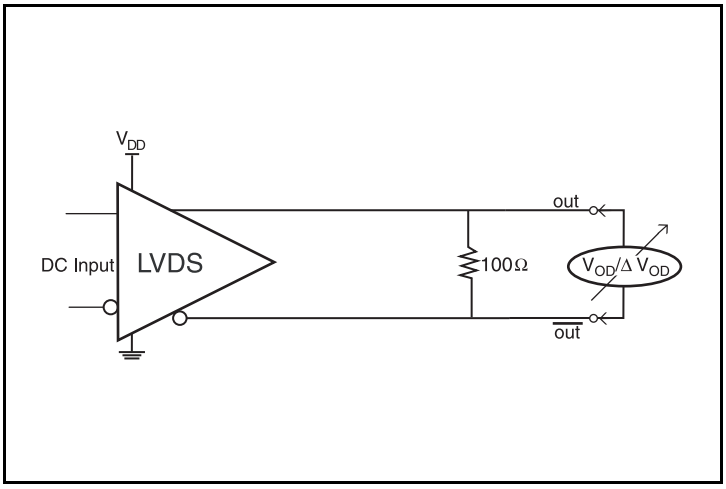

**LVDS Output Rise/Fall Time**




**LVPECL Output Rise/Fall Time**




**Offset Voltage Setup**




**Differential Output Voltage Setup**

# Applications Information

## Recommendations for Unused Input and Output Pins

### Inputs:

#### CLKx/nCLKx Inputs

For applications not requiring the use of either differential input, both CLKx and nCLKx can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLKx to ground. It is recommended that CLKx, nCLKx be left unconnected in frequency synthesizer mode.

#### LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

#### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

#### LVCMOS Outputs

All unused LVCMOS outputs can be left floating. There should be no trace attached.

## Recommended Values for Low-Bandwidth Mode Loop Filter

External loop filter components are not needed in Frequency Synthesizer or High-Bandwidth modes. In Low-Bandwidth mode, the loop filter structure and components are recommended, refer to the Application Schematic. Please consult IDT if other values are needed.

## Wiring the Differential Input to Accept Single-Ended Levels

*Figure 4* shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the $V_1$ in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{CC}$ = 3.3V, R1 and R2 value should be adjusted to set $V_1$ at 1.25V. The values below are for when both the single ended swing and $V_{CC}$ are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however $V_{IL}$ cannot be less than -0.3V and $V_{IH}$ cannot be more than $V_{CC}$ + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

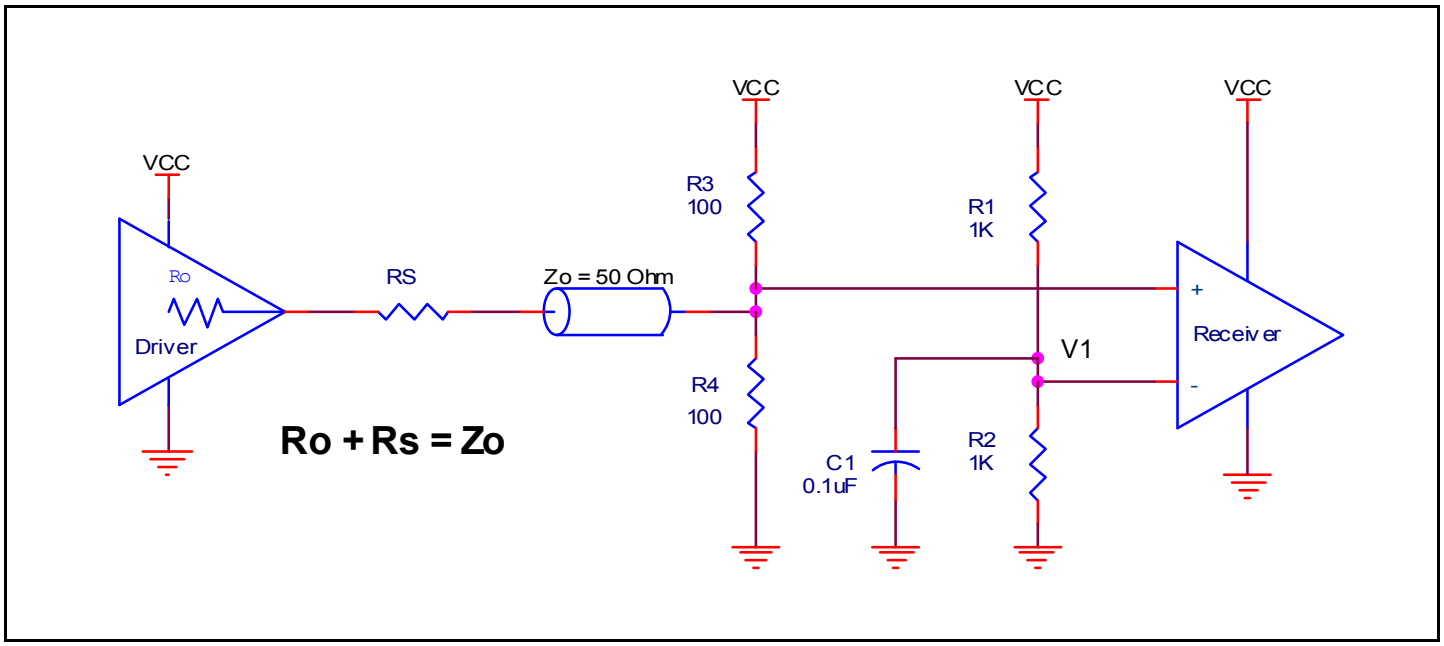



**Figure 4. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels**

## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both differential signals must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 5A to 5E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 5A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

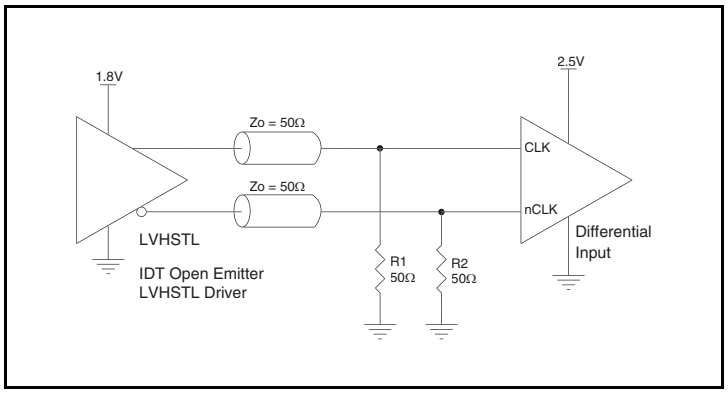



**Figure 5A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver**

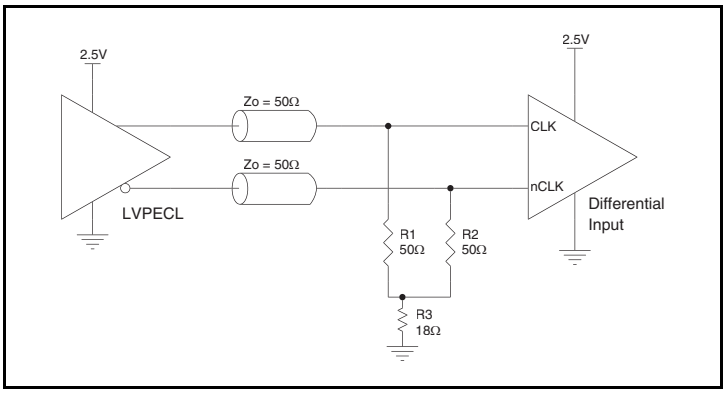



**Figure 5B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver**

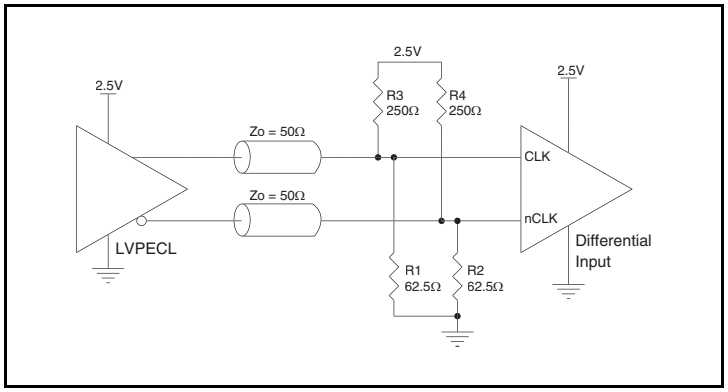



**Figure 5C. CLK/nCLK Input Driven by a 2.5V LVPECL Driver**

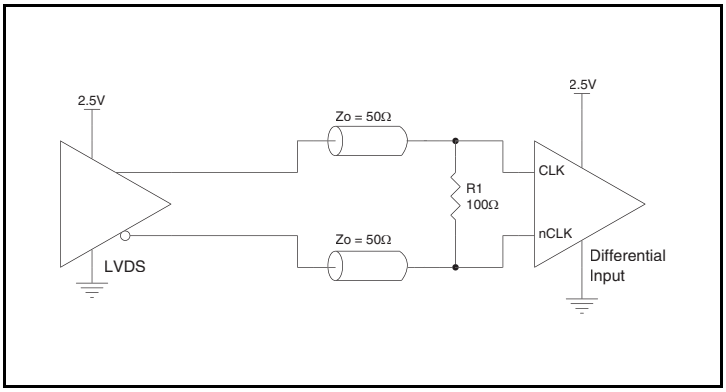



**Figure 5D. CLK/nCLK Input Driven by a 2.5V LVDS Driver**

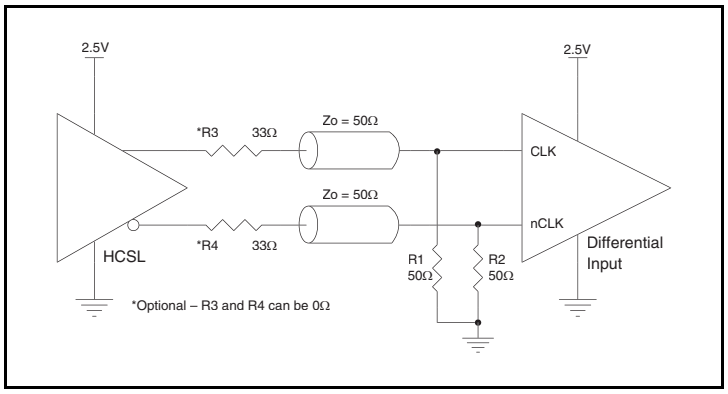



**Figure 5E. CLK/nCLK Input Driven by a 2.5V HCSL Driver**

## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ($Z_T$) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance ($Z_0$) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 6A* can be used with either type of output structure. *Figure 6B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

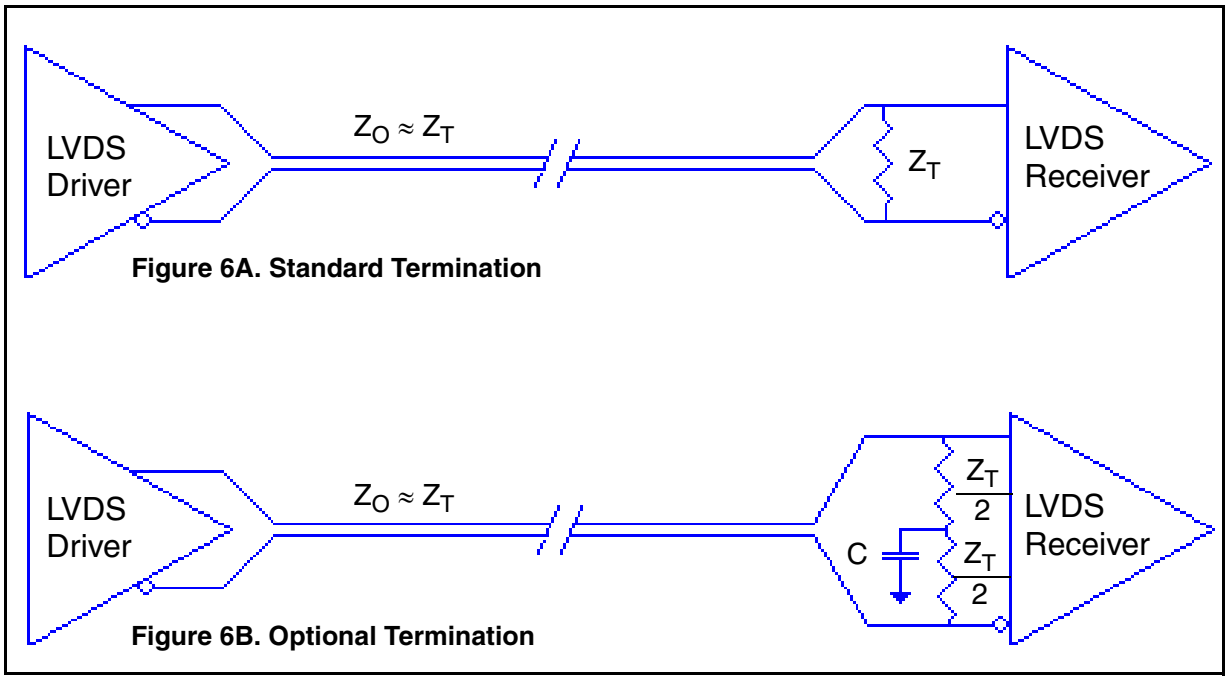



**Figure 6A. Standard Termination**

**Figure 6B. Optional Termination**

**LVDS Termination**

## Termination for 2.5V LVPECL Outputs

*Figure 7A* and *Figure 7B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC}$ – 2V. For $V_{CC}$ = 2.5V, the $V_{CC}$ – 2V is very close to ground level. The R3 in Figure 7B can be eliminated and the termination is shown in *Figure 7C.*

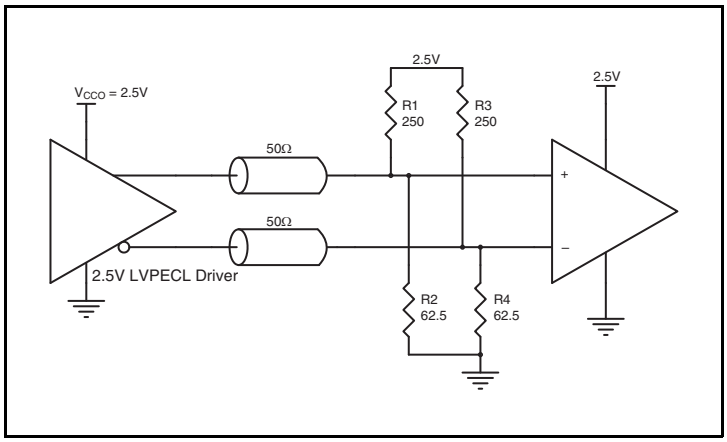



**Figure 7A. 2.5V LVPECL Driver Termination Example**

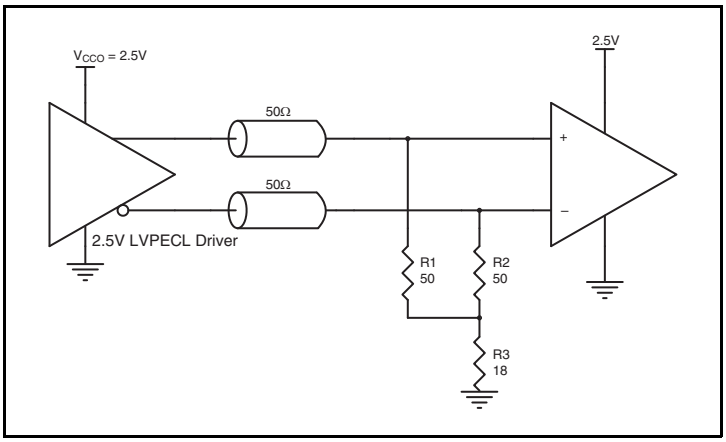



**Figure 7B. 2.5V LVPECL Driver Termination Example**

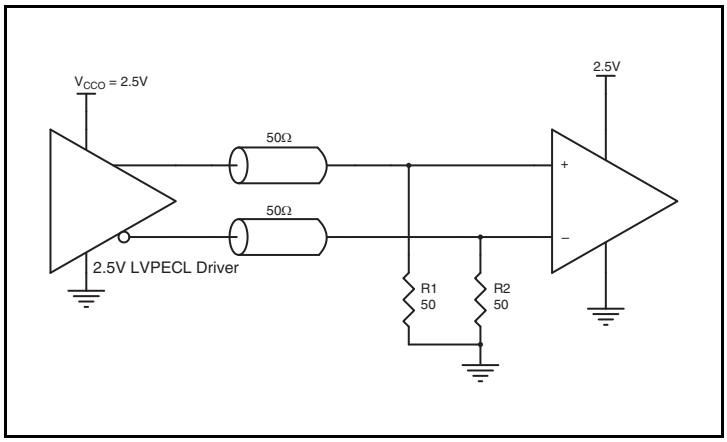



**Figure 7C. 2.5V LVPECL Driver Termination Example**

## Schematic Layout

*Figure 8* (next page) shows an example IDT8T49N445I application schematic. The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the PLL_BYPASS pin is properly set. Input and output terminations shown are intended as examples only and may not match the exact user application. To promote readability in this schematic, only Jitter Attenuator B and the global pins REFCLK and SDATA and SCLK are shown connected. Jitter Attenuator A, C and D are recommended to be connected similarly to Jitter Attenuator B, however different connections may be used; the four jitter attenuators are fully independent.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The IDT8T49N445Iprovides separate $V_{CC\_X}$, $V_{CCA\_X}$ and $V_{CCO\_X}$ power supplies for each jitter attenuator to isolate any high switching noise from coupling into the internal PLLs.

In order to achieve the best possible filtering, it is highly recommended that the 0.1uF capacitors on the device side of the ferrite beads be placed on the device side of the PCB as close to the power pins as possible. This is represented by the placement of these capacitors in the schematic. If space is limited, the ferrite beads, 10uf and 0.1uF capacitor connected to 2.5V can be placed on the opposite side of the PCB. If space permits, place all filter components on the device side of the board.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

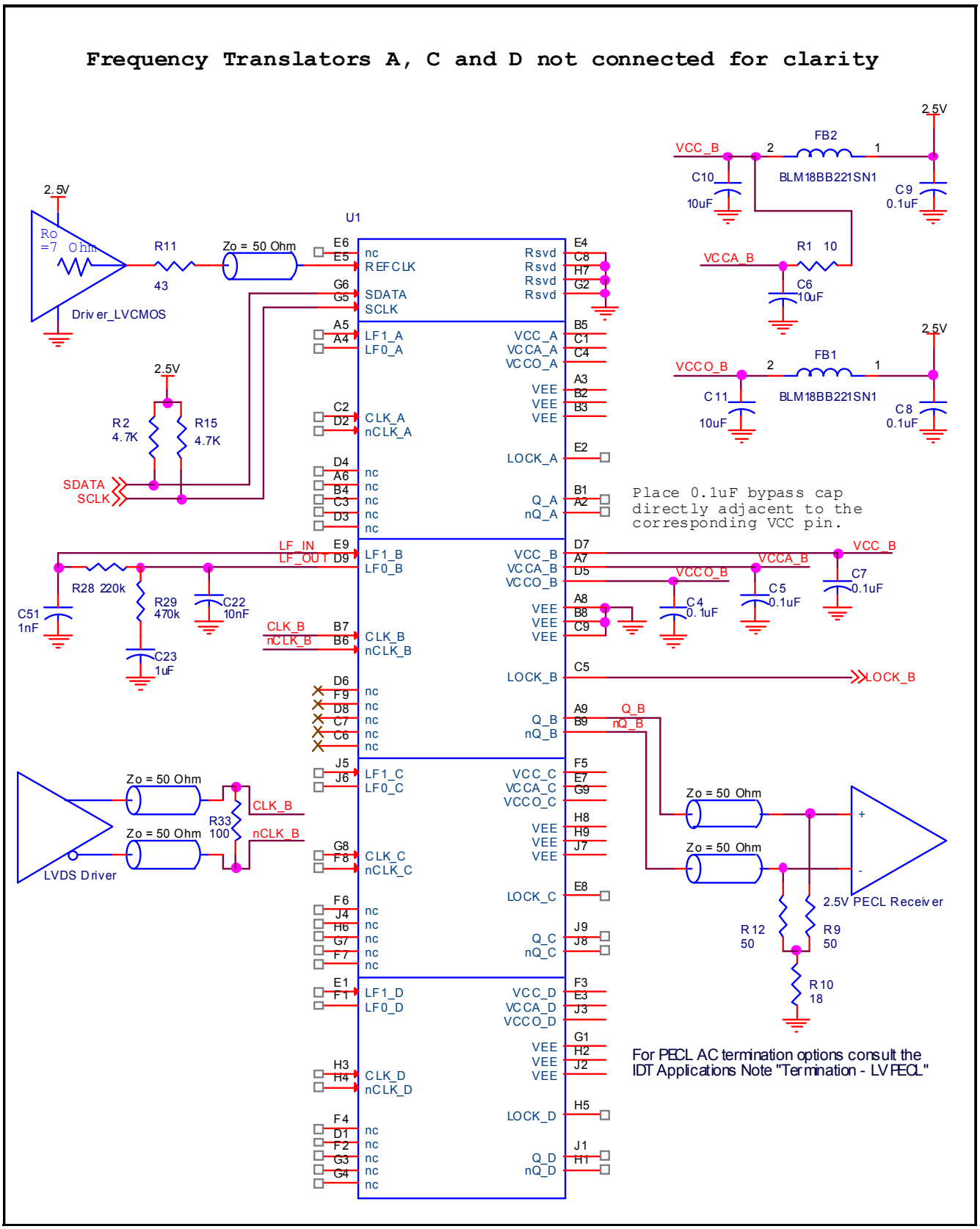



**Figure 8. IDT8T49N445I Schematic Example**