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TLE82452-3SA

2 Channel High-Side and Low-Side Linear Solenoid Driver IC

Dragon IC

Data Sheet

-

Rev 1.0, 2015-03-27

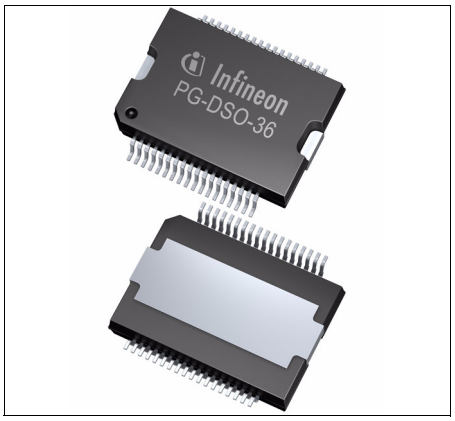
Automotive Power

Table of Contents

2 Channel High-Side and Low-Side Linear Solenoid Driver IC
Dragon IC

TLE82452-3SA

1 Overview



PG-DSO-36

Features

- Two independent low side / high side configurable channels
- Integrated half-bridge power stages
- R_{ON}(max) = 250 mΩ @ Tj = 150 °C
- Integrated sense resistor with internal TCR compensation
- Load current measurement range = 0 mA to 1500 mA (typical)
- Current setpoint resolution = 11 bits
- Current control accuracy
  - +/- 5mA for load currents less than 500 mA
  - +/- 1% for load currents greater than 500 mA
- Excellent immunity to large load supply voltage changes
- Integrated dither generator with programmable amplitude & frequency
- SPI interface for output control, diagnosis, and configuration
- Independent thermal shutdown for each channel
- Open load, switch bypass, and overcurrent protection and diagnosis for each channel
- Programmable slew rate control for reduced EMI
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLE82452-3SA is a flexible, monolithic solenoid driver IC designed for the control of linear solenoids in automatic transmission, electronic stability control, and active suspension applications. The two channels can be used as either lowside or highside drivers in any combination.The device includes the drive transistor, recirculation transistor, and current sensing resistor; minimizing the number of required external components.

This device is capable of regulating the average current flow in a load up to 1500 mA, depending on the dither settings and the load characteristics, with 11 bits resolution. A triangular dither waveform generator, when enabled, superimposes a triangular waveform with programmable amplitude and frequency on the programmed current setpoint.

A 32 bit SPI interface is used to control the two channels and to monitor the status of the diagnostic functions.

An active low reset input, RESN, is used to disable all of the channels and reset the internal registers to the default values. An active high enable pin, EN, is used to enable or disable the operation of the output channels. When the EN pin is low, the channels are disabled, and the SPI interface is fully functional. A fault output pin is provided to generate a signal that can be used as an external interrupt to the microcontroller whenever a fault is detected.

Type	Package	Marking
TLE82452-3SA	PG-DSO-36	TLE82452-3SA

2 Block Diagram

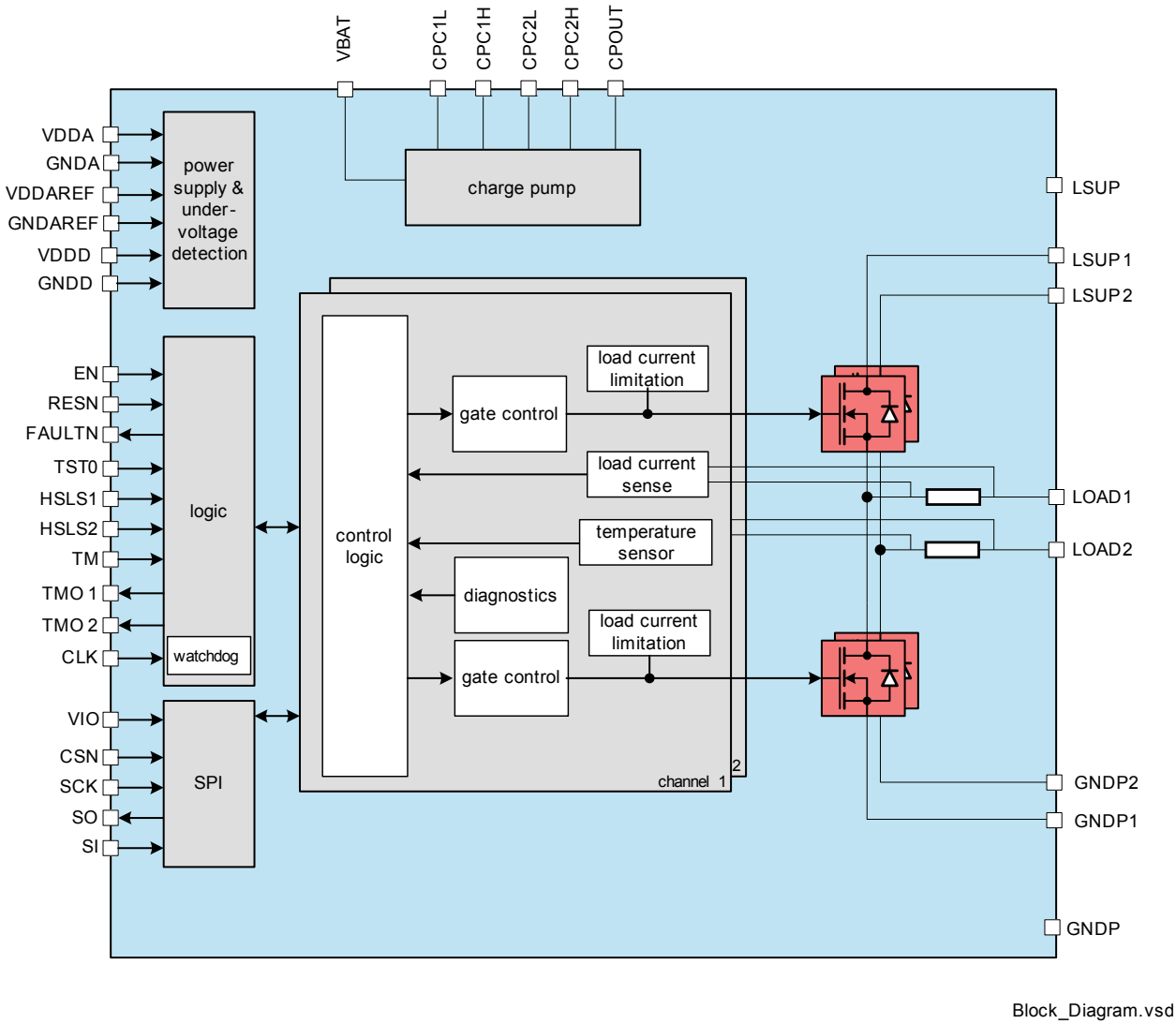


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

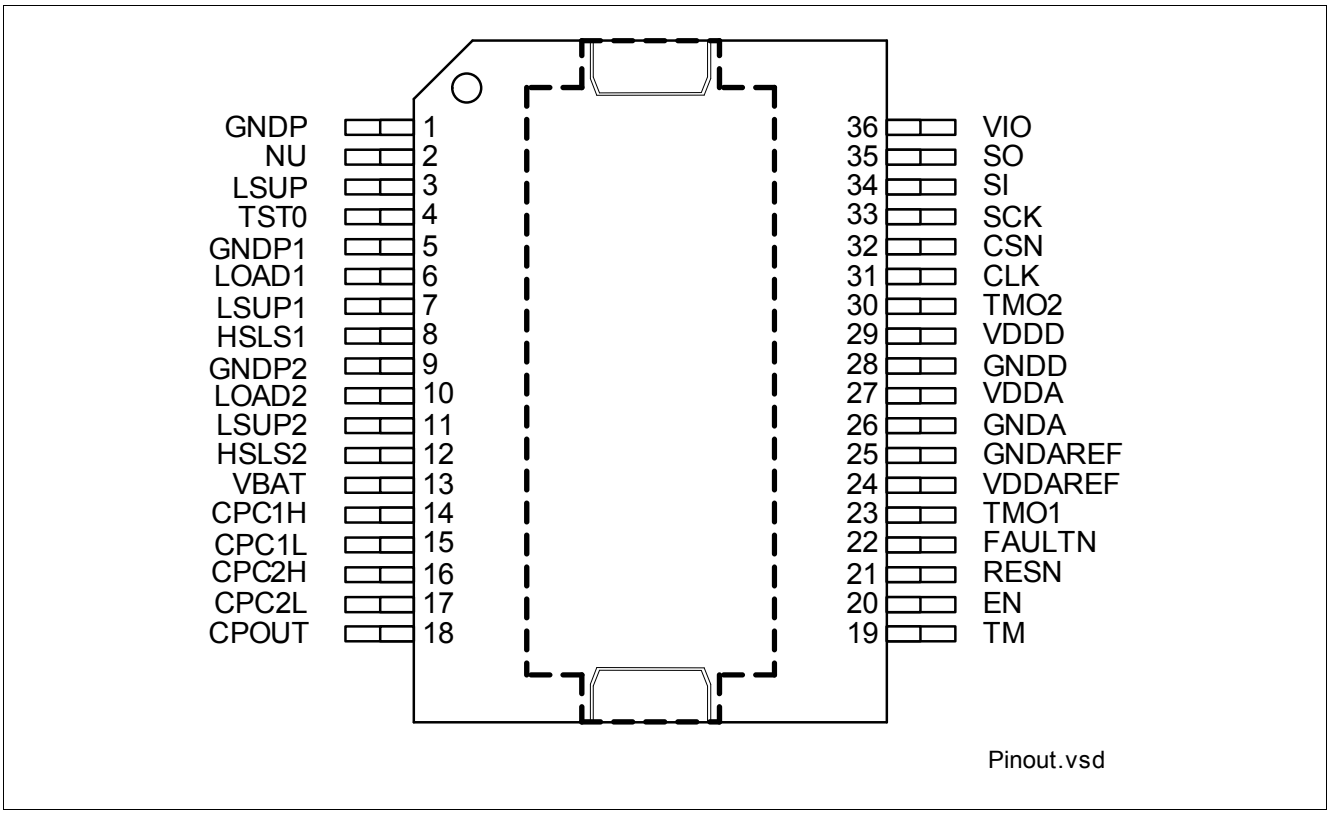


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GNDP	**Ground;** Ground connection. Chip damaged if connection lost.
2	NU	**Not Used** No connection should be made to this pin.
3	LSUP	**Supply Voltage;** Connect to Switched Battery Voltage with reverse protection diode and filter against EMC
4	TST0	**Test Pin;** connect to GND or +5V
5	GNDP1	**Ground;** Ground connection for channel 1 power stage. Chip damaged if connection lost.
6	LOAD1	**Output** Connect a ceramic capacitor of <= 10 nF to GND for ESD protection.
7	LSUP1	**Supply Voltage;** Supplies channel 1. Connect to Switched Battery Voltage with Reverse protection diode and filter against EMC.

Pin	Symbol	Function
8	HSLS1	**Control Input;** Digital input. Connect to ground for high-side configuration. Connect to +5V or VBAT for low-side configuration.
9	GNDP2	**Ground;** Ground connection for channel 2 power stage. Chip damaged if connection lost.
10	LOAD2	**Output;** Connect a ceramic capacitor of <= 10 nF to GND for ESD protection.
11	LSUP2	**Supply;** Supplies channel 2. Connect to Switched Battery Voltage with reverse protection diode and filter against EMC.
12	HSLS2	**Control Input;** Digital input. Connect to ground for high-side configuration. Connect to +5V or VBAT for low-side configuration.
13	VBAT	**Supply Voltage;** Connected to Battery Voltage with reverse protection diode and filter against EMC.
14	CPC1H	**Charge Pump;** For internal charge pump; connect a ceramic capacitor between CPC1H and CPC1L.
15	CPC1L	**Charge Pump;** For internal charge pump; connect a ceramic capacitor between CPC1H and CPC1L.
16	CPC2H	**Charge Pump;** For internal charge pump; connect a ceramic capacitor between CPC2H and CPC2L.
17	CPC2L	**Charge Pump;** For internal charge pump; connect a ceramic capacitor between CPC2H and CPC2L.
18	CPOUT	**Charge Pump Output** For internal charge pump; connect a ceramic storage capacitor from this pin to VBAT. This pin should not be connected to other external components or used as a supply for other circuits.
19	TM	**Test Pin;** connect to GND.
20	EN	**Control Input;** Digital input: 3.3V or 5.0V logic levels. Active high enable input.
21	RESN	**Control Input;** Digital input: 3.3V or 5.0V logic levels. Active low reset input.
22	FAULTN	**Status Output;** Open Drain output. In case not used, keep open.
23	TMO1	**Test Pin;** connect to GND.
24	VDDAREF	**Supply Voltage;** Supplies analog circuits. Connect to 5.0V supply voltage.
25	GNDAREF	**Ground;** Ground connection for analog circuits.
26	GNDA	**Ground;** Ground connection for analog circuits.
27	VDDA	**Supply Voltage;** Supplies analog circuits. Connect to 5.0V supply voltage.
28	GNDD	**Ground;** Ground connection for digital circuits.
29	VDDD	**Supply Voltage;** Supplies digital circuits. Connect to 5.0V supply voltage
30	TMO2	**Test Pin;** connect to GND.
31	CLK	**Clock Input;** Main system clock.
32	CSN	**SPI Chip Select Input;** Digital input: 3.3V or 5.0V logic levels.
33	SCK	**SPI Clock Input;** Digital input: 3.3V or 5.0V logic levels.
34	SI	**SPI Input;** Digital input: 3.3V or 5.0V logic levels.
35	SO	**SPI Output;** Push Pull output compatible to 3.3 V and 5.0 V logic levels.

Pin	Symbol	Function
36	VIO	**IO Supply;** Connected to 3.3 V or 5.0 V supply.
Cooling Tab	GND	Cooling Tab; internally connected to GND.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground (GNDD), positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply Voltage	V_{BAT}	-0.3	–	45	V	–	P_4.1.1
Load Supply Voltage	V_{LSUP}	-0.3	–	45	V	–	P_4.1.2
Digital, Analog, and IO Supply Voltage	V_{DDD}, V_{DDA}, V_{DDAREF}, V_{IO}	-0.3	–	5.5	V	with respect to GNDD, GNDA, GNDAREF, and GNDPx	P_4.1.3
Input Voltage; SCK, CSN, SI, RESN, EN, TM, CLK	V_{INLV}	-0.3	–	V_{DDD}+ 0.3[2)]	V	–	P_4.1.4
Input Voltage; HSLS1, and HSLS2	V_{HSLSX}	-0.3	–	V_{BAT}+ 0.3[3)]	V	–	P_4.1.6
Open Drain Output; FAULTN	V_{FAULTN}	-0.3	–	V_{IO}+ 0.3[2)]	V	–	P_4.1.9
Push Pull Output; SO	V_{SO}	-0.3	–	V_{IO}+ 0.3[2)]	V	–	P_4.1.10
Voltage; LOADx	V_{LOAD}	-2	–	V_x+ 5 [4)]	V	$\|I_l\|$ < 1.6 A	P_4.1.11
Voltage; CPOUT	V_{CPOUT}	V_{BAT} - 0.3	–	50	V	–	P_4.1.12
Maximum Voltage; CPC1L, CPC2L	V_{CPCxL}	-0.3	–	50	V	–	P_4.1.13
Maximum Voltage; CPC1H, CPC2H	V_{CPCxH}	-0.3	–	50	V	–	P_4.1.14
Maximum Voltage; GNDPx	V_{GNDP}	-0.3	–	1.0	V	with respect to GNDD	P_4.1.15
Maximum Voltage; GNDA, GNDAREF	V_{GND}	-0.3	–	0.3	V	with respect to GNDD	P_4.1.16
Currents							
Output Current	I	-1.6	–	1.6	A	DC[5)]	P_4.1.17
Output Current, FAULTN Pin	I_{FAULTN}	0	–	20	mA	DC	P_4.1.18
Output Current, SO Pin	I_{SO}	-20	–	20	mA	DC	P_4.1.19

Table 1 Absolute Maximum Ratings[1)] (cont'd)

T_j = -40 °C to +150 °C; all voltages with respect to ground (GNDD), positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Current; SCK, CSN, SI, RESN, EN, TM, CLK	I_{IN}	-5	–	5	mA	maximum allowable forward and reverse current through the ESD structure	P_4.1.20
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	continuous operation	P_4.1.21
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.22
ESD Susceptibility							
ESD Resistivity to GND	V_{ESD}	-2	–	2	kV	HBM[6)]	P_4.1.23
ESD Resistivity all pins[7)]	V_{ESD}	-2	–	2	kV	HBM[6)]	P_4.1.24
ESD Resistivity to GND	V_{ESD}	-500	–	500	V	CDM[8)]	P_4.1.25
ESD Resistivity Pin 1, 18, 19, 36 (corner pins)	$V_{ESD1,18,19,36}$	-750	–	750	V	CDM[8)]	P_4.1.26

1) Not subject to production test, specified by design.
2) Voltage must not exceed 5.5V.
3) Voltage must not exceed 45.0V.
4) VLOADx - VGNDPx and VLSUPx-VLOADx must not exceed 45.0V.
5) Compliant to short circuit requirements according to AEC-Q100-012.
6) ESD susceptibility, HBM according to EIA/JESD 22-A114B.
7) Pin VBAT vs. Pin CPC1H : +/- 1.5kV.
8) ESD susceptibility, Charged Device Model "CDM" EIA/JESD22-C101 or ESDA STM5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage Range for Nominal Operation	V_{BATnom}	8	–	17	V	–	P_4.2.1
Extended Supply Voltage Range for Operation	$V_{BAT(ext)}$, $V_{LSUP\_UV(ext)}$	V_{LSUP_UV}	–	8	V	Parameter deviations possible	P_4.2.2
Extended Supply Voltage Range for Operation	$V_{BAT(ext)}$, $V_{LSUP(ext)}$	17	–	40	V	Parameter deviations possible	P_4.2.3
VBAT Supply Voltage transients slew rate	dV_{BAT}/dt	-1	–	1	V/µs	[1] –	P_4.2.4
Load Supply Voltage	V_{LSUP}	8	–	V_{BAT}+0.3 [2]	V	–	P_4.2.5
Load Supply Voltage transients slew rate	dV_{LSUP}/dt	-1	–	1	V/µs	[1] –	P_4.2.6
Digital Supply Voltage	V_{VDDD}	4.75	–	5.25	V		P_4.2.7
Analog Supply Voltage	V_{VDDA}, $V_{VDDAREF}$	4.75	–	5.25	V		P_4.2.8
Ground Offset Voltage; GNDA, GNDAREF	V_{GND}	-0.1	–	0.1	V	with respect to GNDD	P_4.2.9
IO Supply Voltage	V_{IO}	3.0	–	5.25	V	–	P_4.2.10
Voltage (static); LOADx	V_{LOADx}	-0.3	–	V+ 0.3	V	–	P_4.2.11
Voltage (dynamic); LOADx	V_{LOADx}	-2	–	V+ 5	V	$\|I_l\|$ < 1.6 A	P_4.2.12
System Clock Frequency	F_{SYS}	4	–	6	MHz	F_{SYS} = F_{CLK} / F_{SYS_div}	P_4.2.13
CLK pin Frequency	F_{CLK}	8	–	40	MHz	–	P_4.2.14
SPI Clock Frequency	F_{SCK}	–	–	8	MHz	–	P_4.2.15
LOADx PWM Frequency	F_{LOAD}	100	–	4000	Hz	dependent on solenoid characteristics	P_4.2.16
Junction Temperature	T_j	-40	–	150	°C	–	P_4.2.17

1) Not subject to production test, specified by design.

2) VLSUPx - GNDD must not exceed 45.0V.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case[1)]	R_{thJC}	–	–	2	K/W	–	P_4.3.1
Junction to Ambient	R_{thJA}	–	15	–	K/W	[2)]	P_4.3.2

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

5 Input / Output

5.1 I/O Description

The CLK pin must be connected to a precise clock signal. This clock is used by the internal analog to digital converters and by the internal logic. A small internal pull down current will keep the voltage on this pin near ground when the pin is open. The device includes a programmable divider to generate the internal system clock from the CLK pin signal. This divider ratio is programmed in the CLK-DIVIDER register by the SPI interface. The output stages cannot be enabled until this field has been written.

An internal watchdog circuit will hold the device in an internal reset state if the delay between rising edges on the CLK pin is greater than the threshold time, T_{CLK_MSS}. The watchdog is initially disabled when the device exits the reset state. The watchdog is enabled by setting the WDEN bit in the CLK-DIVIDER register. If the watchdog is enabled, there are no settings which can prevent the fault pin being pulled low during a WD event.

Until the watchdog is enabled, the output stages are disabled. Once the watchdog function is enabled, a missing CLK signal will set the Watchdog Status Bit in the IC VERSION register, set the FAULTN pin to a logic low state, disable the output stages, and cause the device to enter an internal reset state. If the CLK signal is missing, the SPI response from the device will always be the response to an IC VERSION register read command. If the CLK signal returns after the watchdog function has triggered, the SPI response to a specific register read command will be the reset value of the specific register, except of the ICVID Register that is indicating the Watchdog timeout fault. Be aware that the CLK-DIVIDER is reset to 8 when the CLK is lost and than returns, which affects the system clock frequency (F_{SYS} = F_{CLK}/8) and thus the transfer delay time (see P_11.3.6).

In both cases it is not possible to write to any SPI register. To return to normal operation and exit this internal reset state the device must be reset externally by the RESN pin or an power on reset must be performed.

The EN pin is used to enable / disable the output stages. If the EN pin is low, all of the channels are disabled and (when the fault mask bit FME = 1) the FAULTN pin is pulled low. The SPI interface remains functional. However, when the EN pin is low, the EN bits in the SET-POINT registers are cleared. The EN pin can be connected to a general purpose output pin of the microcontroller or to an output of a safing circuit. However, all other SPI register settings remain unchanged. After the EN pin goes high the EN bits in the set point registers remain 0 until they are changed to 1. The EN bits will immediately return to 0 if the EN pin is low.

The RESN pin is the reset input for the device. If the RESN pin is low, the device is held in an internal reset state, the FAULTN pin is held low, and the SPI interface is disabled. An internal pull down current source will hold the RESN pin low in case the pin is open.

The FAULTN pin is an open drain output. This pin is pulled low when a fault is detected by the diagnosis circuit or when the device is in an internal reset state. An external resistor should be connected between this pin and the VIO supply.

The SI, SO, CSN, and SCLK pins comprise the SPI interface. See **Chapter 11**and **Chapter 12** for details.

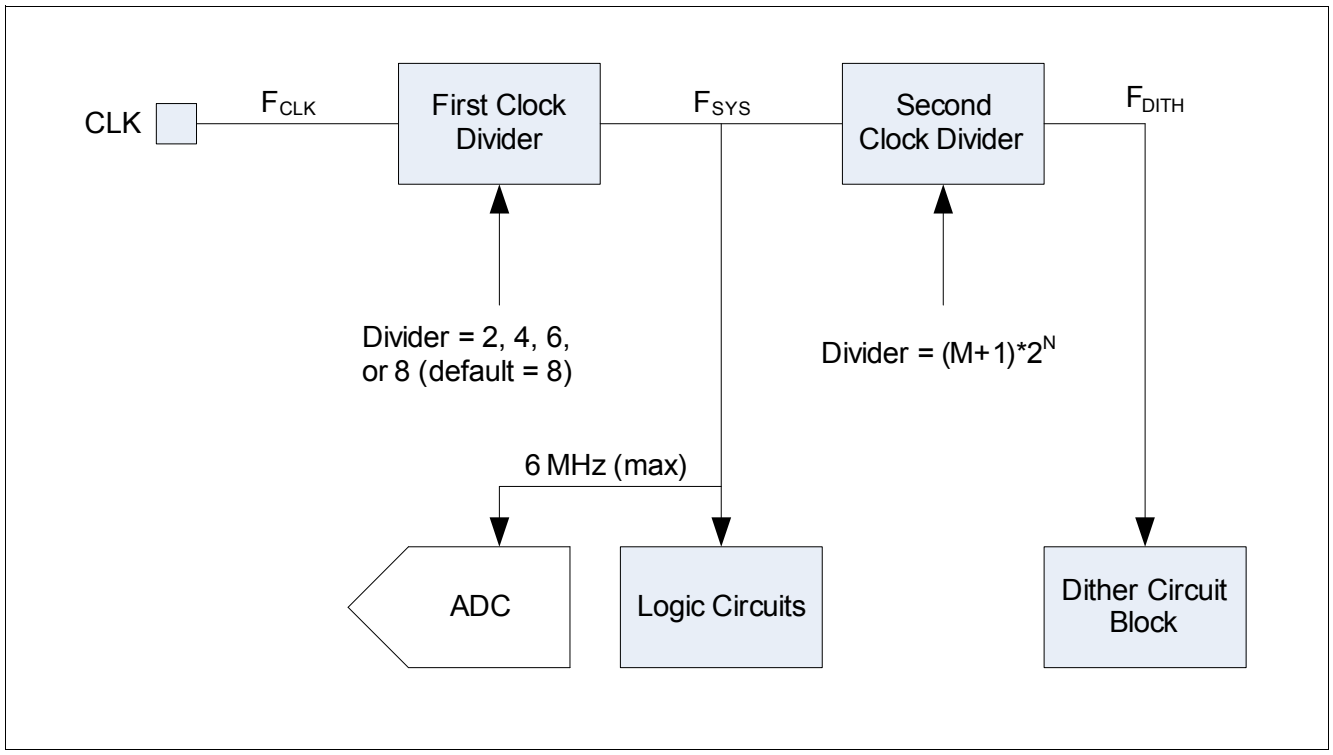


Figure 3 Clock Divider

5.2 Electrical Characteristics I/O

Table 4 Electrical Characteristics:

V_{BAT} = 8 V to 17 V, V_{DDx} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C, all voltages with respect to ground (GNDD), positive current flowing into pin
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Control Inputs EN, RESN, CSN, SI, SCK, CLK							
Input threshold - low	V_{IN_L}	0.8	–	–	V	V_{IN} increasing	P_5.2.1
Input threshold - high	V_{IN_H}	–	–	2.0	V	V_{IN} decreasing	P_5.2.2
Input hysteresis	V_{IN_HYS}	–	50		mV		P_5.2.3
Pull up current - CSN	I_{PU}	-50	–	-10	µA		P_5.2.4
Pull down current - EN, SI, SCK, CLK, RESN	I_{PD}	10	–	50	µA		P_5.2.5
Output SO							
Output low-level voltage	V_{SO_L}	0	–	0.5	V	I_{SO} = 0.5mA	P_5.2.6
Output high-level voltage	V_{SO_H}	V_{IO} - 0.5	–	V_{IO}	V	I_{SO} = -0.5mA, 3.0V < V_{IO} < 5.5V	P_5.2.7
Output tri-state leakage current	I_{SO_OFF}	-10	–	10	µA	V_{CSN}=V_{IO}	P_5.2.8
Output FAULTN							
Output low-level voltage	V_{FLT_L}	0	–	0.4	V	I_{FLT} = 2mA	P_5.2.9
Output tri-state leakage current	V_{FLT_OFF}	-10	–	10	µA		P_5.2.10

6 Power Supply

6.1 Overview

The TLE82452-3SA has multiple supply pins. The internal circuits are powered by three +5.0 V supply pins; VDDD, VDDA, and VDDAREF; and by one battery pin, VBAT. A separate supply pin, VIO, can be connected to either a 3.3 V or 5 V supply depending on the logic levels of the interfaced microcontroller I/O signals. The device includes a charge pump circuit which generates a supply voltage greater than VBAT.

6.2 Battery Supply (VBAT)

This pin is the supply for the internal charge pump and must be connected to the reverse polarity protected battery voltage supply. For correct operation the voltage on this pin must not be lower than the voltage on any of the LSUPx pins. This pin is also used by the overvoltage detection circuit.

6.3 Load Supplies (LSUP2, LSUP1)

These pins are the supply pins for the two output stages. If the voltage on one of these pins is lower than the LSUP under voltage threshold, the respective power stage is disabled and the respective UVx fault bit is set in the DIAGNOSIS register. The LSUP pins of unused channels must be connected to VBAT.

6.4 Analog Supplies (VDDA and VDDAREF)

The VDDA pin is the supply for the internal analog circuits such as the amplifiers and analog-to-digital converters. The VDDAREF pin is the supply for the internal bandgap references. An externally regulated 5.0 VDC +/- 5% supply must be connected to these pins. A ceramic capacitor with a value of 100nF must be connected between each of these pins and ground near the IC.

These pins are monitored by a pair of internal comparators. The internal logic circuits are held in a reset state if the voltage on either of these pins is less than the threshold V_{DDA_UV} and V_{DDAREF_UV}.

6.5 Digital Supply (VDDD)

This pin is the supply for all of the internal logic circuitry. An externally regulated 5.0 VDC +/- 5% supply must be connected to this pin. A ceramic capacitor with a value of 100nF must be connected between this pin and ground near the IC.

This pin is monitored by an internal comparator. The internal logic circuits are held in a reset state if the voltage on this pin is less than the threshold V_{DDD_UV}.

6.6 I/O Supply (VIO)

This pin is used to supply the pins that interface with the external microcontroller. This pin must be connected to a supply with the same voltage, 3.3V or 5.0V, that is used to supply the peripherals of the microcontroller.

6.7 Power On Reset

An internal power on reset circuit holds the device in a reset state if any of the supplies VDDD, VDDA, or VDDAREF is below the respective undervoltage detection threshold. The device is also held in reset if the clock signal on the CLK pin is missing or the clock frequency is too low when the CLK pin watchdog is enabled. The power on reset is released after the following conditions. All of the supplies are above their respective threshold voltages then a fixed power on reset time (T_{POR}) elapses. The SPI interface can be accessed after the power on reset time.

The fault bit “RST” in the DIAGNOSIS register is set whenever the device exits the reset state. This bit is cleared automatically whenever the DIAGNOSIS register is accessed. The microcontroller can use this bit to determine if an internal or external reset has occurred.

6.8 Charge Pump

In order to provide low Rdson of the high-side mosfet transistors, a charge pump is used to drive the internal gate voltage above VBAT. The device uses a common charge pump for all channels. The charge pump uses the battery voltage supply connected to the VBAT pin. The charge pump output voltage at the CPOUT pin is regulated to typically 11V above the voltage at the VBAT pin.
The charge pump circuit requires three external capacitors. A reservoir capacitor with a recommended value of 220nF must be connected between the CPOUT pin and the VBAT pin. Two pump capacitors with recommended values of 27nF must be connected between the CPC1L and CPC1H pins and also between the CPC2L and CPC2H pins. A built in supervisor circuit checks if the charge pump output voltage is sufficient to control the high-side mosfet transistors. If the VCPOUT voltage is less than the charge pump undervoltage threshold, the output transistors are disabled and the CPUV fault flag is set in the DIAGNOSIS register. A separate CPW (Charge Pump Warning) fault bit in the DIAGNOSIS register is set if the VCPOUT voltage is below the CP warning threshold voltage. The device will continue to operate normally when the VCPOUT voltage is between the CPW threshold and the CPUV threshold, however the current control accuracy may be outside of the specification limits.

6.9 Sleep Mode

If any one of the VDDD, VDDA, and VDDAREF voltage supplies is below the respective undervoltage threshold, the device enters sleep mode. The current drawn into the VBAT pin is reduced during this mode of operation. Sleep mode is automatically exited when all of the VDDD, VDDA, and VDDAREF supply pins are above the respective undervoltage threshold. The sleep mode has the same effect as a reset and follows the Initialization Sequence.

6.10 Power Supply Modes

The following table describes the operation of the device with all possible power supply modes of VBAT, VCPOUT, VDDD, VDDA, VDDAREF, and VIO. The “X” symbol means that the state of this supply does not effect the result (can be either supplied or not supplied) in the specific case.

VDDD	< VDDx_UV	X	X	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV
VDDA	X	< VDDx_UV	X	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV
VDDAREF	X	X	< VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV	> VDDx_UV
RESN	X	X	X	LOW	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
CLK	X	X	X	X	TCLK > TCLK_MSS	TCLK > TCLK_MSS	TCLK < TCLK_MSS	TCLK < TCLK_MSS	TCLK < TCLK_MSS	TCLK < TCLK_MSS	TCLK < TCLK_MSS	TCLK < TCLK_MSS
VIO	X	X	X	X	> 3.0V	> 3.0V	0V	> 3.0V	> 3.0V	> 3.0V	> 3.0V	> 3.0V
WDEN	X	X	X	X	LOW	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
EN	X	X	X	X	X	X	HIGH	LOW	HIGH	HIGH	HIGH	HIGH
VCPOUT - VBAT	X	X	X	X	X	X	> CPUV	X	< CPUV	> CPUV	> CPUV	> CPUV
VBAT	X	X	X	X	X	X	< VBATOV	X	X	> VBATOV	< VBATOV	< VBATOV
VLSUP$_x$	X	X	X	X	X	X	> VLSUPUV	X	X	X	< VLSUPUV	> VLSUPUV
Sleep Mode	YES	YES	YES	NO	NO	NO	NO	NO	NO	NO	NO	NO
Watchdog Fault	NO	NO	NO	NO	NO	YES	NO	NO	NO	NO	NO	NO
Channel Operational	NO	NO	NO	NO	NO	NO	YES	NO	NO	NO	NO (Channel X only)	YES
SPI Functional	NO	NO	NO	NO	YES	NO Response is ICVID	INPUT – YES Response is 0000$_H$	YES	YES	YES	YES	YES
Diagnostics Functional	NO	NO	NO	NO	NO	NO	YES	NO Load faults are detected	YES	YES	YES	YES
FAULTN	LOW	LOW	LOW	LOW	LOW	LOW	Undefined	LOW (1)	LOW	LOW	LOW (4)	HIGH
RST bit	HIGH (2)	HIGH (2)	HIGH (2)	HIGH (2)	HIGH (3)	HIGH (3)	unchanged	unchanged	unchanged	unchanged	unchanged	unchanged

Figure 4 Power Supply Mode Diagram

The X's indicate a don't care condition for all the states below the double line.

1. The FAULTN pin is LOW if the FME fault mask bit is set to 1
2. The RST bit in the DIAGNOSIS register will be set after the device exits the reset state
3. A missing CLK signal will result in a reset only if the CLK Watchdog has been enabled
4. The FAULTN pin is LOW if the FMx fault mask bit is set to 1

6.11 Initialization

The following figure illustrates the initialization sequence for the device after power-up. The T_{POR} cycle begins on the first CLK clock cycle after the RESN pin transitions from low to high.

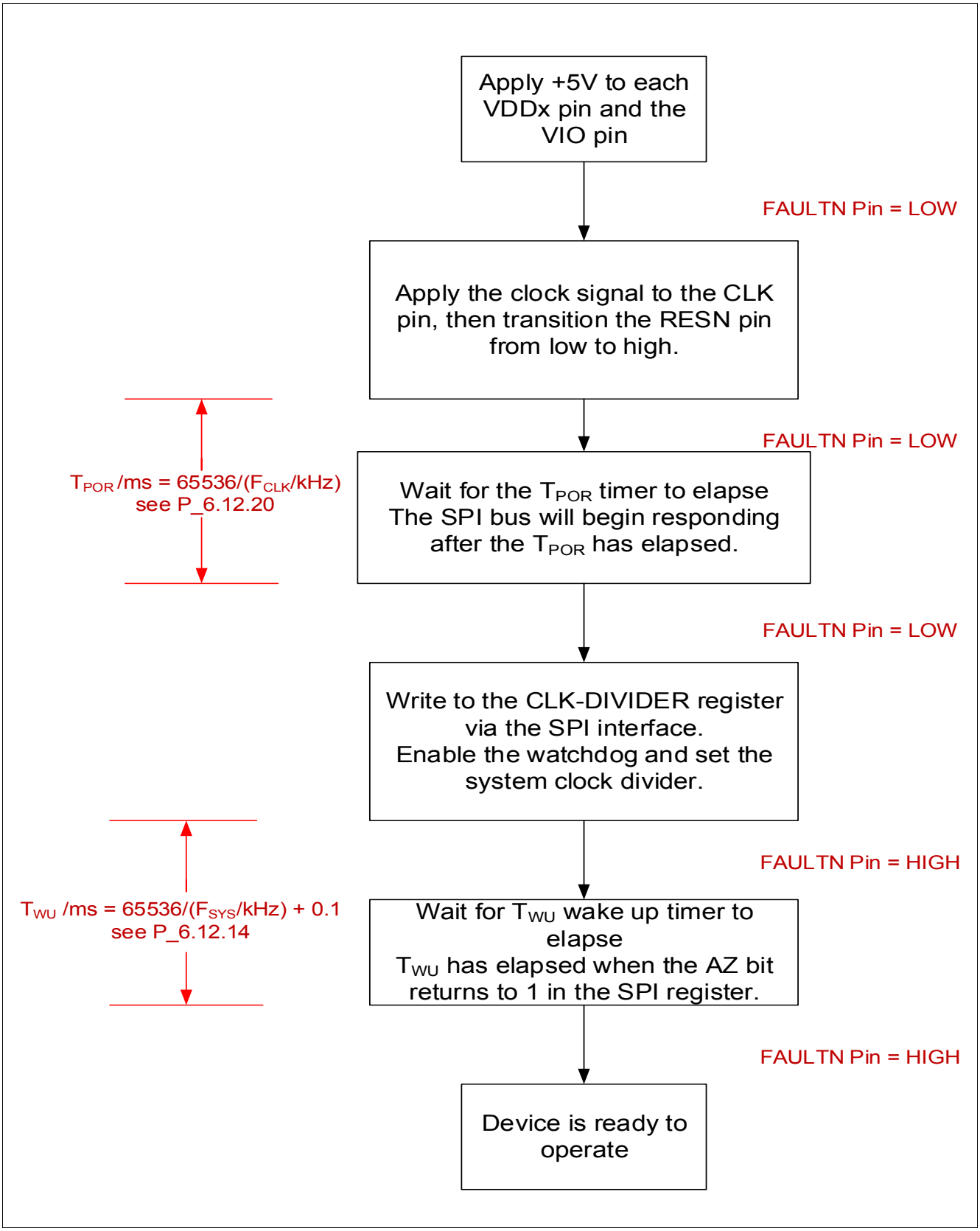


Figure 5 Initialization Sequence

6.12 Reset

If the device needs to be shut down during operation the RESN pin can be pulled low. The RESN pin should be held low until the current flowing in the solenoid decays to zero. If the device is restarted with current flowing in the solenoid the auto zero function will enter the value as an offset, causing an error in the current control.

6.13 Electrical Characteristics

Table 5 Electrical Characteristics: Power Supply

V_{BAT} = 8 V to 17 V, V_{DDx} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C, CPC1 and CPC2 = 27nF CPCOUT = 220nF, all voltages with respect to ground (GNDD), positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
VBAT Current Consumption normal mode	I_{VBAT}	–	–	10	mA	all channels active	P_6.12.1
VBAT Current Consumption sleep mode	I_{VBAT_SLP}	–	–	8	µA		P_6.12.2
VDDD Current Consumption	I_{VDDD}	–	–	20	mA		P_6.12.3
VDDA Current Consumption	I_{VDDA}	–	–	13	mA		P_6.12.4
VDDAREF Current Consumption	$I_{VDDAREF}$	–	–	4	mA		P_6.12.5
VIO Current Consumption	I_{VIO}	–	–	1	mA	CSN=V_{IO}=5.25V	P_6.12.6
Undervoltage reset (internally generated) - VDDA	V_{DDA_UV}	3.8	–	4.3	V	V_{DDA} decreasing	P_6.12.7
Undervoltage reset (internally generated) - VDDAREF	V_{DDAREF_UV}	3.8	–	4.3	V	V_{DDAREF} decreasing	P_6.12.8
Undervoltage reset (internally generated) - VDDD	V_{DDD_UV}	3.8	–	4.3	V	V_{DDD} decreasing	P_6.12.9
Undervoltage hysteresis	V_{UV_HYS}		150		mV		P_6.12.10
LSUP undervoltage threshold	V_{LSUP_UV}	4.5		5.5	V		P_6.12.11
Missing CLK clock detection time	T_{CLK_MSS}	2	–	10	µs		P_6.12.12
Power On Reset time initialized with RESN	T_{POR}	–	–	0.1	ms	[1)]Logic circuits are functional after T_{POR} timer	P_6.12.13
Power On Reset time initialized with undervoltage reset	T_{POR}	–	–	T_{POR} =65536/ (F_{CLK}/kHz)	ms	[1)]Logic circuits are functional after T_{POR} timer	P_6.12.20

Table 5 Electrical Characteristics: Power Supply (cont'd)

V_{BAT} = 8 V to 17 V, V_{DDx} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C, CPC1 and CPC2 = 27nF CPCOUT = 220nF, all voltages with respect to ground (GNDD), positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Power-on wake-up time	T_{WU}	–	–	T_{WU} =65536/ (F_{SYS}/kHz) + 0.1	ms	1)Timer starts after writing to the CLK-DIV register, (CSN goes high) all supplies are above the UV thresholds and RESN pin is high. Output stages are functional after T_{WU} 2)	P_6.12.14
Charge Pump							
Charge pump voltage	V_{CP_OUT}	V_{BAT}+8	–	V_{BAT} +13 3)	V		P_6.12.15
Charge pump clock frequency	F_{CP}	–	65	–	KHz	F_{SYS} = 6 MHz 4)	P_6.12.16
Charge pump warning threshold voltage	V_{CPOUT_W}	V_{BAT}+7	–	V_{BAT}+ 8.5	V		P_6.12.17
Charge pump undervoltage threshold voltage	V_{CPOUT_UV}	V_{BAT} +4.5	–	V_{BAT} +5.5	V		P_6.12.18
Charge pump overvoltage clamp	V_{CPOUT_OV}	–	48.5	–	V		P_6.12.19

1) Not subject to production test, specified by design.

2) To guarantee a proper Autozero result there must not be any I_{LOAD} during power-on wake-up (**Chapter 8.7**).

3) Will not exceed V_{CPOUT_OV}.

4) Parameter not subject to production test, specified by design.

Attention: Voltage Ratings for Charge Pump caps: CPC1/CPC2: Vmin=VBATmax + 10V, CCPOUT: Vmin=16V

7 Power Stages

7.1 Overview

There are two output channels implemented in this device. The output power stages of each channel consists of a half bridge made up of two n-channel DMOS transistors and a current sensing resistor. An internal charge pump generates the voltage required to switch the n-channel DMOS high-side switches. The switches are protected from external failures by built in overcurrent and overtemperature detection circuits.

The half bridge arrangement allows the use of active freewheeling, which reduces the power dissipation of the device. The arrangement also allows each channel to be individually programmed for lowside or highside drive. The output current slew rate of the power stages can be programmed to one of three values by programming the CONFIGURATION register by SPI.

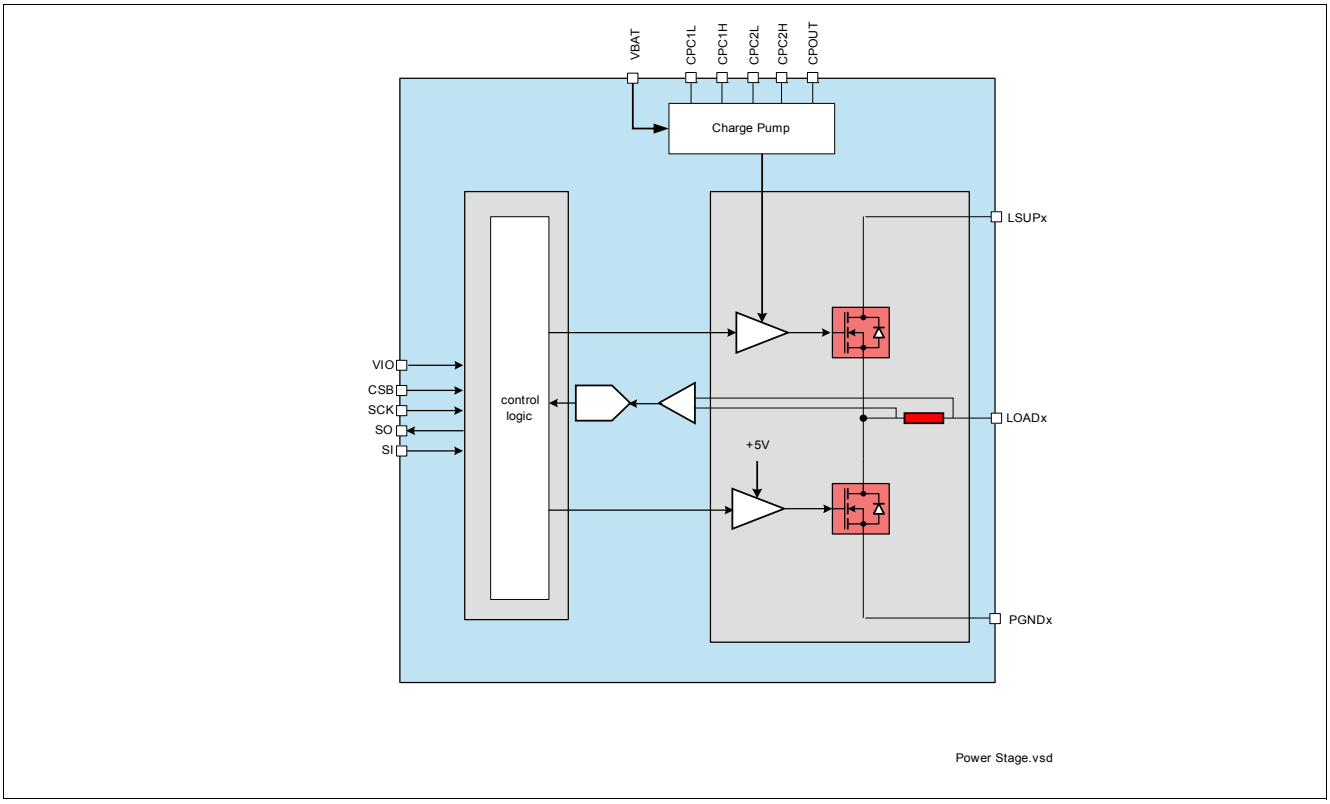


Figure 6 Power Stages

7.2 Channel Disabled

When the channel is disabled, both transistors of the half bridge are turned off. The output stage is in a high output impedance state in this condition. The channel is disabled if the EN pin is 0, or the EN bit is 0, or the set point = 0.

7.3 Channel Enabled

When a channel is configured for lowside operation, the lowside DMOS switch is the “drive” switch and the highside DMOS switch is the “recirculation” switch. Likewise, when a channel is configured for highside operation, the highside DMOS switch is the “drive” switch and the lowside switch is the “recirculation” switch. In normal operation, the “drive” switch is turned on and off with the duty cycle needed to regulate the solenoid current at the target value. During the time that the “drive” switch is turned off, the device is in active freewheeling mode. The “recirculation” switch is turned on in this mode to reduce the voltage drop across the device during recirculation.

The transistors are controlled in a way that prevents shoot through current during switching, that is the control logic prevents the simultaneous activation of both the “drive” switch and the “recirculation” switch. If the EN pin is low, the EN bit is pulled to 0. If the EN pin changes from low to high, the EN bit remains unchanged.

7.4 Configuration of Channels

The pins HSLS1, and HSLS2 are used to configure each channel for highside or lowside operation. The pin must be connected to ground for highside operation and to VBAT or + 5V for lowside operation. The configuration of each channel can be verified by reading the CONFIGURATION register via SPI.

7.5 Electrical Characteristics Power Stages

Table 6 Electrical Characteristics: Power Stages

V_{BAT} = 8 V to 17 V, V_{DDx} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C, all voltages with respect to ground (GNDD), positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
LSUPx leakage current	I_{LSUP_LKG}	-150	–	150	µA	set-point = 0mA 8V < V_{LSUP} < V_{BAT} + 0.3V	P_7.6.1
LSUPx leakage current in sleep mode	$I_{LSUP\_LG\_SLP}$	-50	–	50	µA	Sleep mode All VDDx=0V	P_7.6.2
On-State Resistance - high side FET	$R_{DS(ON)\_HS}$	–	–	250	mΩ	T_j = 150°C; I_{LOAD} = -1.6A	P_7.6.3
On-State Resistance - low side FET	$R_{DS(ON)\_LS}$	–	–	250	mΩ	T_j = 150°C; I_{LOAD} = 1.6A	P_7.6.4
LOADx leakage current	I_{LOAD_LKG}	-300	–	0	µA	set-point = 0mA 8V < V_{LSUP} < V_{BAT} + 0.3V; 0V < V_{LOAD} < V_{LSUP}	P_7.6.5
LOADx leakage current in sleep mode	$I_{LOAD\_LKG\_SLP}$	-80	–	80	µA		P_7.6.6
Current rise and fall times - SR0	$T_{R0,}$ $T_{F0,}$	–	1[1)]	–	µs	I_{LOAD} = 1.4A; 8V < V_{LSUP} < V_{BAT} + 0.3V; 20% to 80% ΔI_{LSUP} & ΔI_{GNDP}	P_7.6.7
Current rise and fall times - SR1	$T_{R1,}$ T_{F1}	–	0.5[1)]	–	µs	I_{LOAD} = 1.4A; 8V < V_{LSUP} < V_{BAT} + 0.3V; 20% to 80% ΔI_{LSUP} & ΔI_{GNDP}	P_7.6.8
Current rise and fall times	$T_{R2,}$ T_{F2}	–	2[1)]	–	µs	I_{LOAD} = 1.4A; 8V < V_{LSUP} < V_{BAT} + 0.3V; 20% to 80% ΔI_{LSUP} & ΔI_{GNDP}	P_7.6.9
Voltage slew rate SR0		–	5	–	V/µs		P_7.6.10
Voltage slew rate SR1		–	10	–	V/µs		P_7.6.11
Voltage slew rate SR2		–	2.5	–	V/µs		P_7.6.12
Current Sense Resistor							
Sense resistor resistance	R_{SENSE}	–	250	380	mΩ		P_7.6.13

1) Not subject to production test, specified by design.

8 Current Control

8.1 Overview

The device has independent controller blocks for each channel. Each control loop consists of the average current setpoint input, the dither generator, the load current feedback path, the controller block, and the output stage.

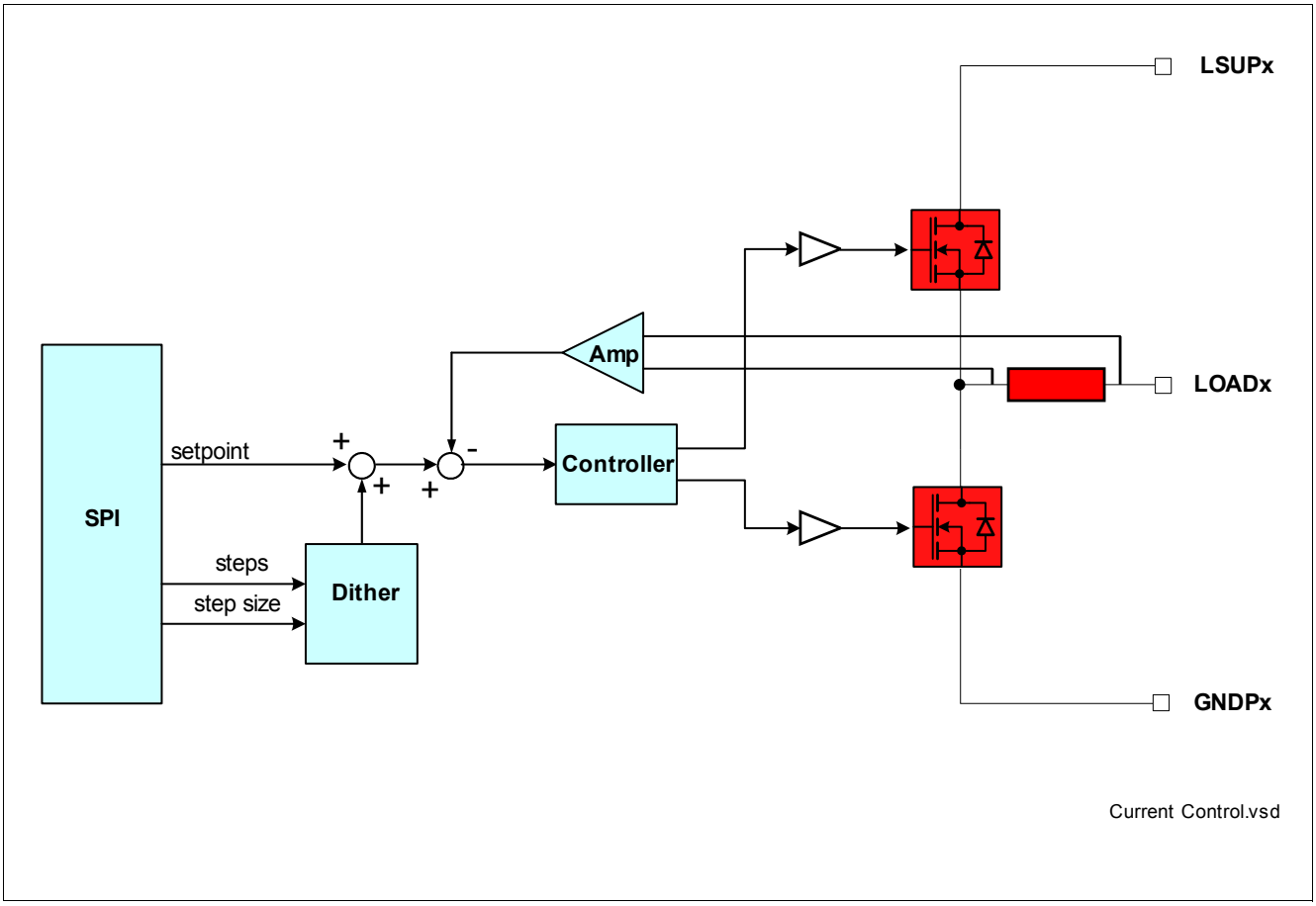


Figure 7 Controller Block Diagram

8.2 Average current setpoint

The average current setpoint value is determined by the contents of the SETPOINT register. The relationship between the value of the setpoint register and the average load current is shown in **Figure 8**.The accuracy band of the current regulation is also shown in **Figure 8**. The accuracy is specified over the normal operating range of the device (including the full normal operating junction temperature range). An automatic auto-zero feature is included in the device. The auto-zero feature will automatically measure the offset of the current measurement circuits of each channel after power-up. When a channel is programmed to regulate current, the offset is compensated by an automatic modification of the setpoint. The content of the SPI accessed average current setpoint register is not influenced by the autozero circuit.