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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



N-Channel 30-V (D-S) Fast Switching MOSFET

PRODUCT SUMMARY

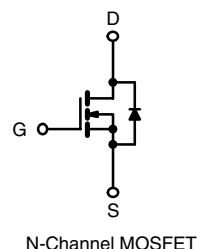
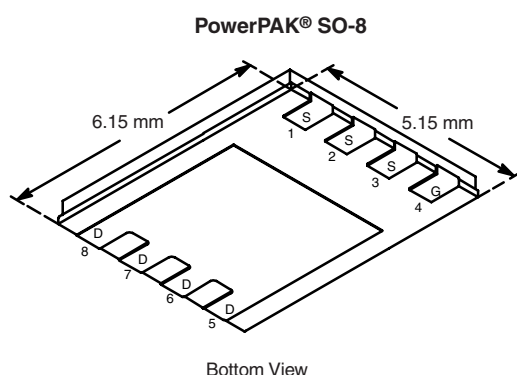
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
30	0.0075 at $V_{GS} = 10$ V	19
	0.010 at $V_{GS} = 4.5$ V	17

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available



Ordering Information: Si7446BDP-T1-E3 (Lead (Pb)-free)
Si7446BDP-T1-GE3 (Lead-(Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

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Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current ($T_J = 150^{\circ}\text{C}$) ^a	$T_A = 25^{\circ}\text{C}$	I_D	19	12	A
	$T_A = 70^{\circ}\text{C}$		15	9	
Pulsed Drain Current		I_{DM}	50		
Continuous Source Current (Diode Conduction) ^a		I_S	4.0	1.6	
Maximum Power Dissipation ^a	$T_A = 25^{\circ}\text{C}$	P_D	4.8	1.9	W
	$T_A = 70^{\circ}\text{C}$		3.0	1.2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature) ^{b, c}			260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	21	26	$^\circ\text{C/W}$
		55	65	
Maximum Junction-to-Case (Drain)	R_{thJC}	1.6	2.0	

Notes

- Surface Mounted on 1" x 1" FR4 board.
- See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

MOSFET SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

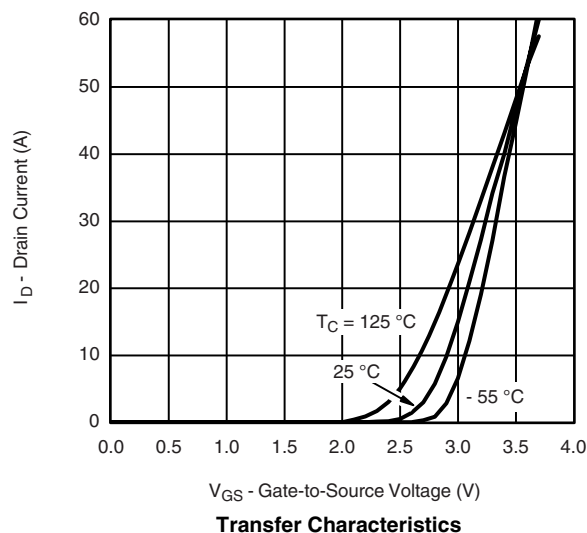
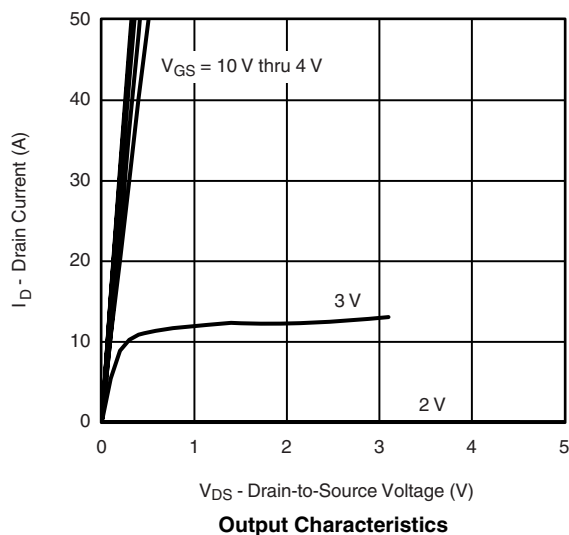
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1.0		3.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	40			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 19\ \text{A}$		0.0064	0.0075	Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 17\ \text{A}$		0.0084	0.010	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 19\ \text{A}$		60		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 4.0\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.75	1.2	V
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$		3076		pF
Output Capacitance	C_{oss}			657		
Reverse Transfer Capacitance	C_{rss}			248		
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}$, $V_{GS} = 5.0\ \text{V}$, $I_D = 19\ \text{A}$		22	33	nC
Gate-Source Charge	Q_{gs}			8.3		
Gate-Drain Charge	Q_{gd}			4.7		
Gate Resistance	R_g		0.4	0.8	1.2	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}$, $R_L = 15\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_g = 6\ \Omega$		20	30	ns
Rise Time	t_r			16	25	
Turn-Off Delay Time	$t_{d(off)}$			120	180	
Fall Time	t_f			43	65	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.3\ \text{A}$, $dI/dt = 100\ \text{A}/\mu\text{s}$		40	80	

Notes:

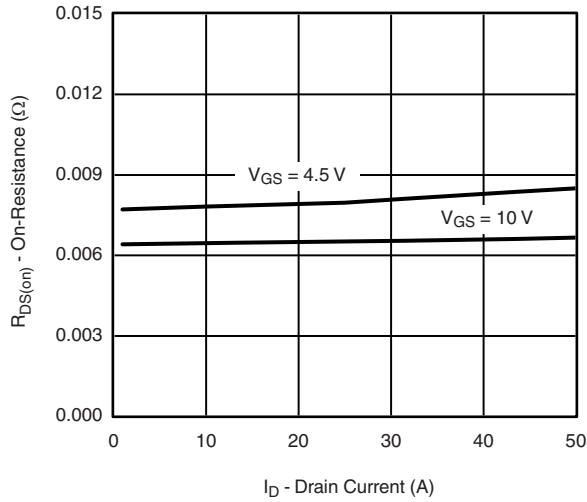
a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

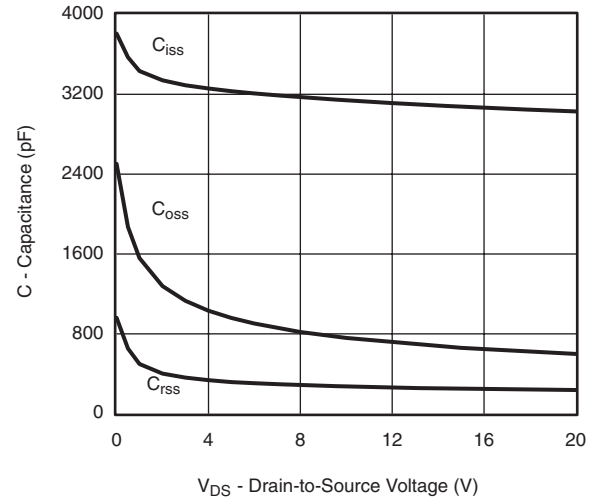
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25°C , unless otherwise noted

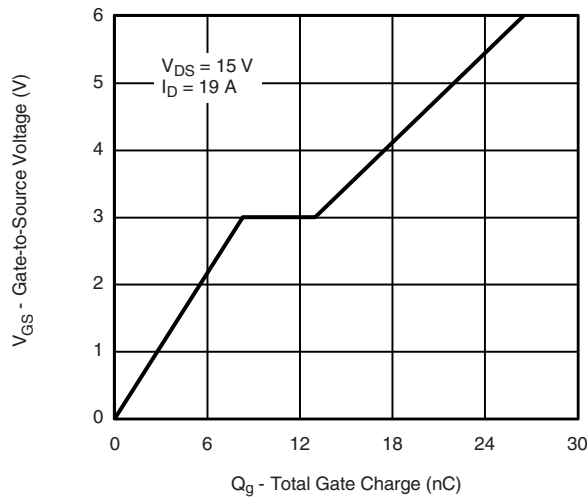
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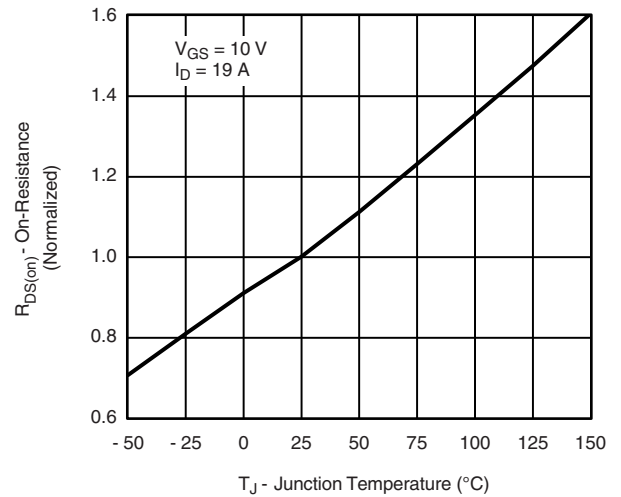
On-Resistance vs. Drain Current



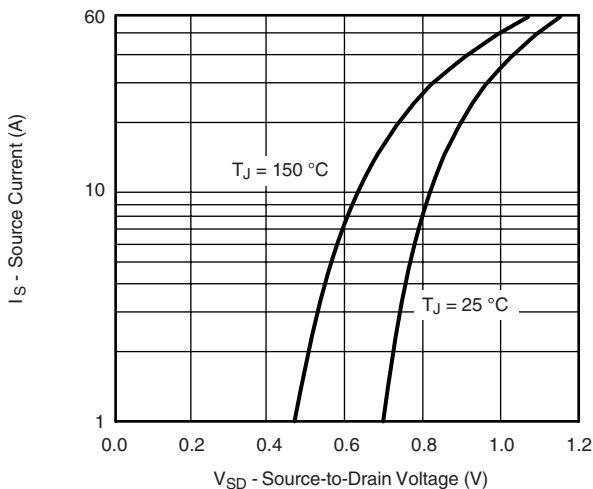
Capacitance



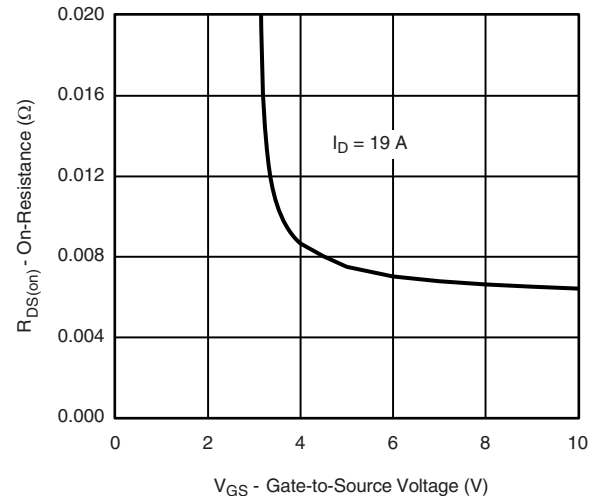
Gate Charge



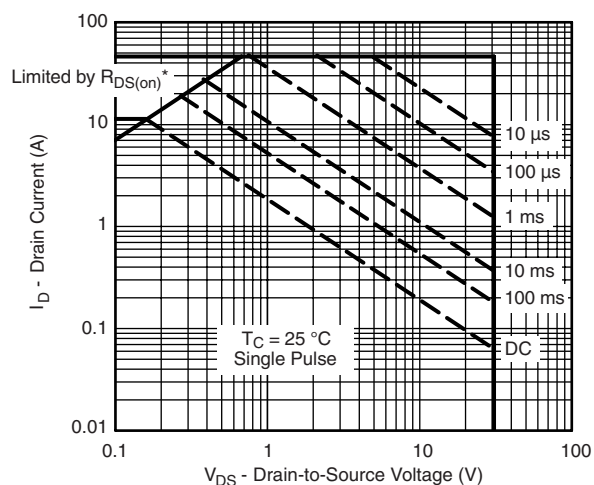
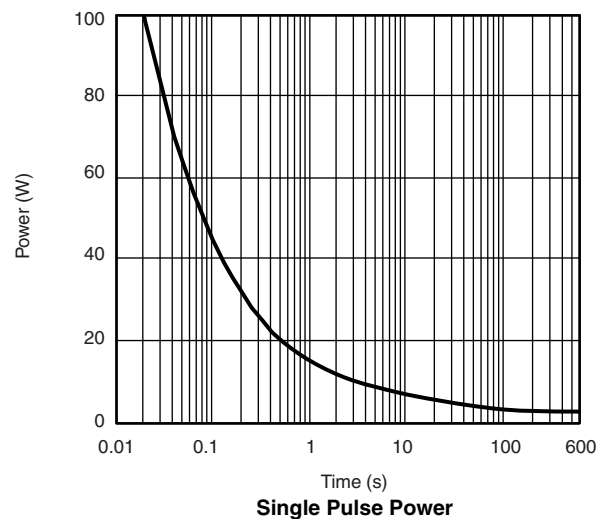
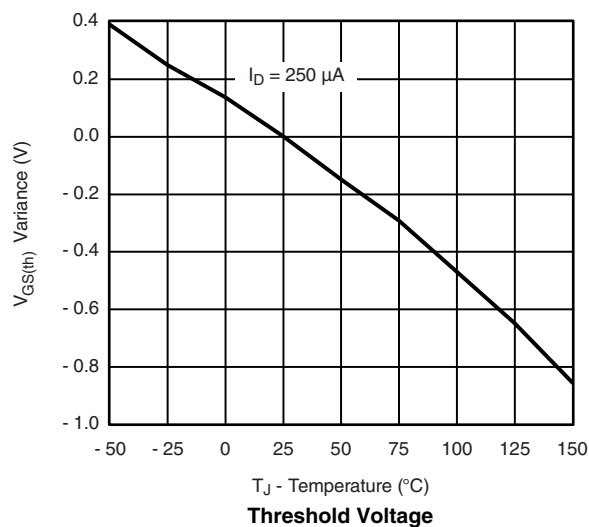
On-Resistance vs. Junction Temperature



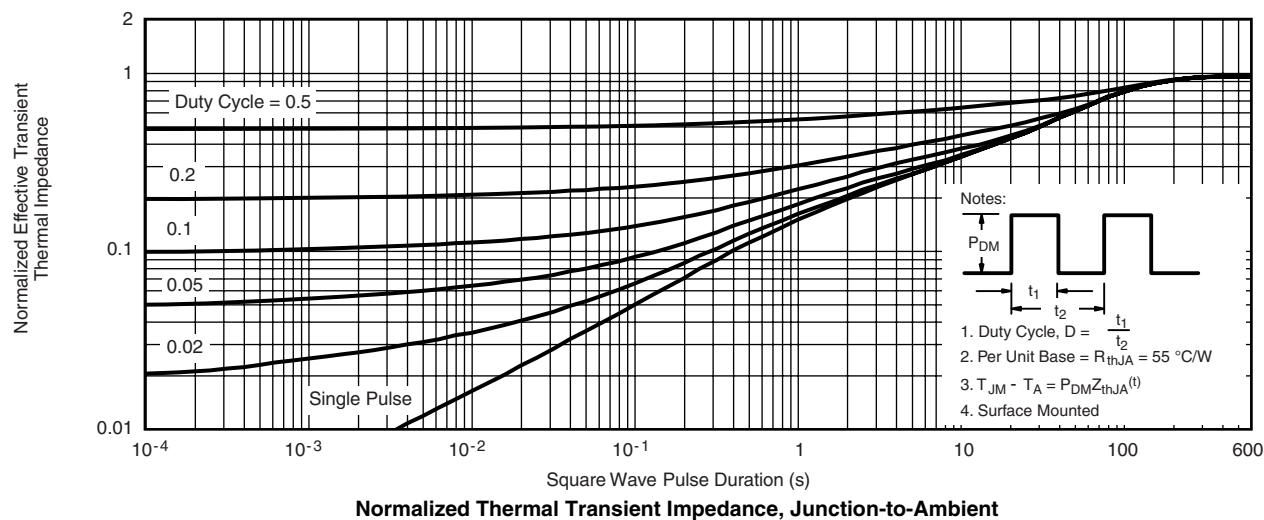
Source-Drain Diode Forward Voltage



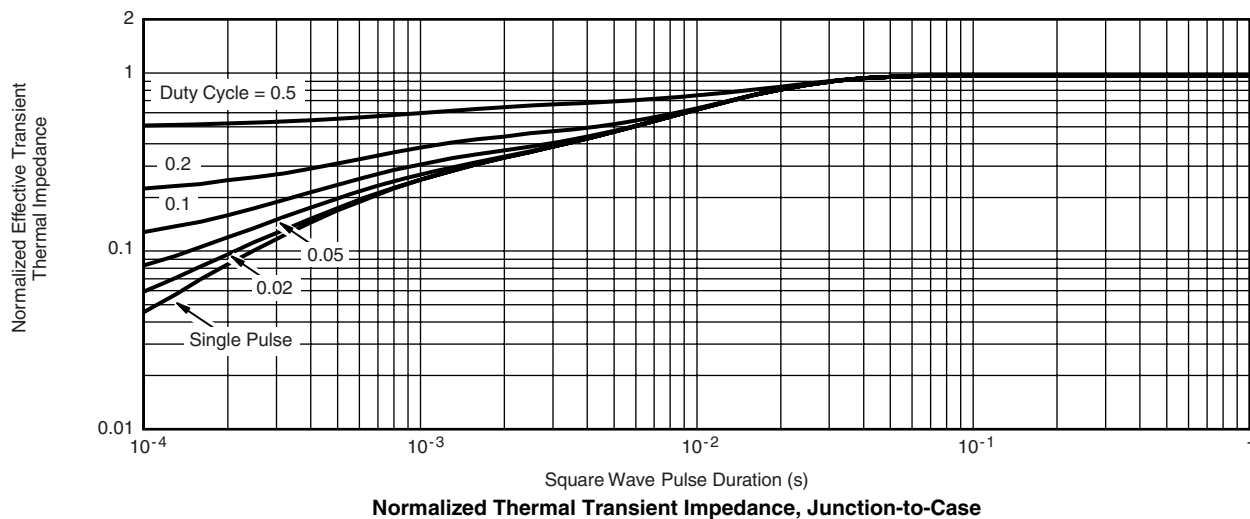
On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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