1EDN7550 and 1EDN8550

Single-channel EiceDRIVER™ with true differential inputs

Feature list

- Single-channel non-isolated gate-drive IC with true differential inputs
- Very large common-mode input voltage range (CMR) up to ± 150 V (***Table 1***)
- Supply voltage (V_{DD}) up to 20 V
- 2 UVLO options: 4 V and 8 V
- Separate low impedance source and sink outputs
  - 4 A / 0.85 Ω source
  - 8 A / 0.35 Ω sink
- 45 ns propagation delay with -7 / +10 ns accuracy
- SOT23 6-pin package
- Fully qualified for industrial applications according to JEDEC

Description

1EDNx550 is a new family of single-channel non-isolated gate-driver ICs. Due to the unique fully differential input circuitry with excellent common-mode rejection, the logic driver state is exclusively controlled by the voltage difference between the two inputs, completely independent of the driver's reference (ground) potential. This eliminates the risk for wrong triggering and thus is a significant benefit in all applications exhibiting voltage differences between driver and controller ground, a problem typical for systems with

- 4-pin packages (Kelvin Source connection)
- high parasitic PCB inductances (long distances, single-layer PCB)
- bipolar gate drive

In addition, within the allowed common-mode voltage range, CMR (***Table 1***), 1EDNx550 allows to address even high-side applications.

Table 1 Product portfolio

Part number	CMR static	CMR dynamic	UVLO	Package	Orderable Part Number
1EDN7550B	+ 72 V / - 84 V	± 150 V	4 V	PG-SOT23-6	1EDN7550BXTSA1
1EDN8550B	+ 72 V / - 84 V	± 150 V	8 V	PG-SOT23-6	1EDN8550BXTSA1

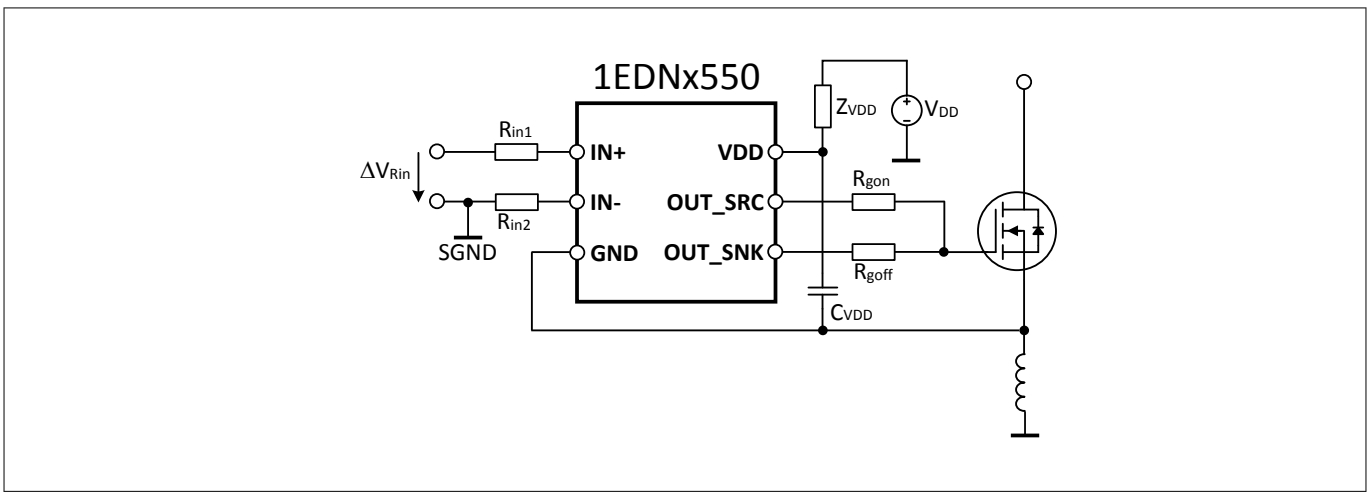

Figure 1 Typical application

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1 Pin configuration and description

The pin configuration for the SOT23 6-pin package is illustrated in ***Figure 2***; a description is given in ***Table 2*** . For functional details, please read ***Chapter 3***.

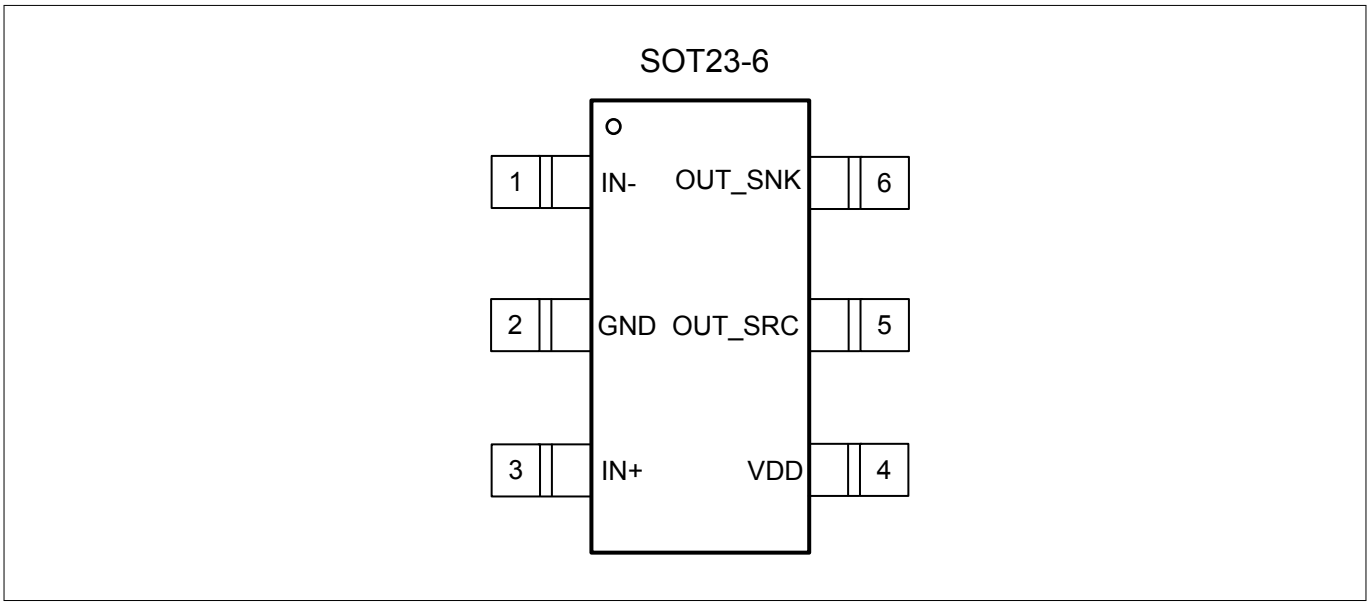

Figure 2 Pin configuration SOT23 6-pin (top side view)

Table 2 Pin description

Symbol	Description
IN+	**Positive input** connected to PWM output of controller via resistor (typically 33 kΩ)
IN-	**Negative input** connected to controller ground via resistor (typically 33 kΩ)
GND	**Ground** negative gate drive voltage ("off" state)
VDD	**Positive supply voltage** positive gate drive voltage ("on" state)
OUT_SNK	**Driver output sink** low-impedance switch to GND (8 A / 0.35 Ω)
OUT_SRC	**Driver output source** low-impedance switch to VDD (4 A / 0.85 Ω)

2 Block diagram

A simplified functional block diagram of 1EDNx550 is given in ***Figure 3***.

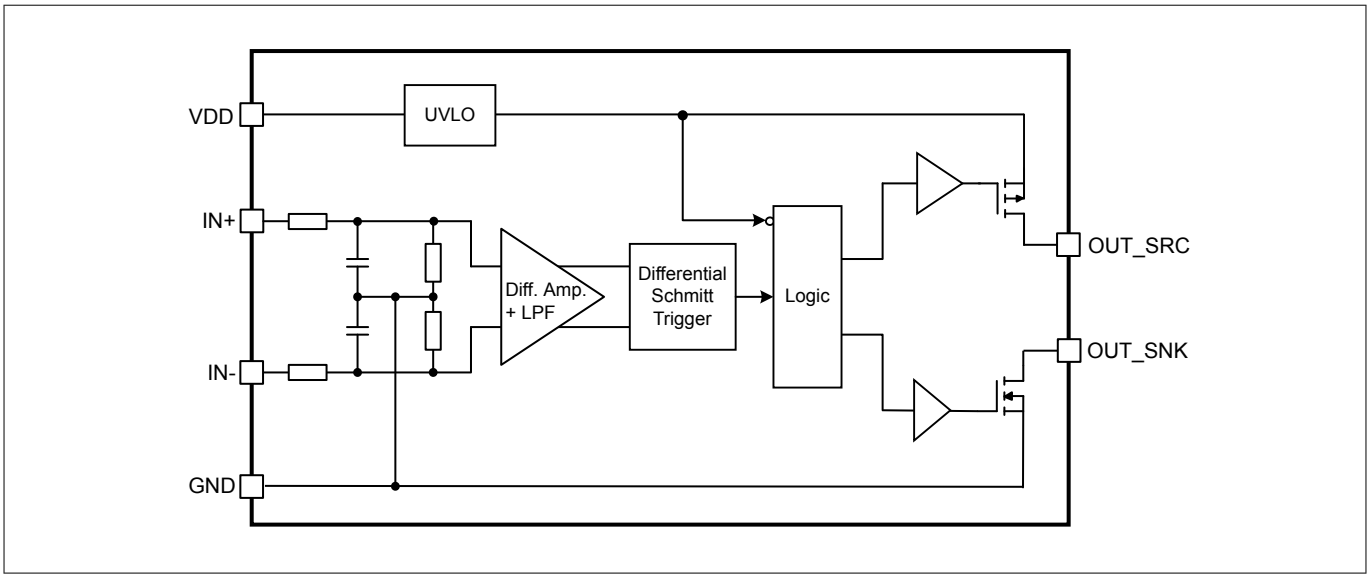

Figure 3 Block diagram

3 Functional description

1EDNx550 is a fast single-channel non-isolated gate driver. However, compared with standard drivers, this new gate driver family extends the range of possible applications into fields usually reserved for isolated drivers, thereby generating significant system cost benefits.

The key to make this possible, is moving from the standard ground related to a true differential input with very high common-mode rejection. The required symmetry of the input circuitry is achieved by on-chip trimming; it finally allows to deal with peak common-mode voltages of up to ± 150 V between driver reference (GND) and system ground (SGND). 1EDNx550 is not only ideally suited for any application with unwanted shifts between driver and system ground, but may also be utilized as a high-side driver within the allowed common-mode range. Besides, switches requiring a bipolar driving voltage can be operated very easily.

3.1 Differential input

Figure 4 depicts the signal path from the controller's PWM output to the logic gate driver signal as implemented on 1EDNx550.

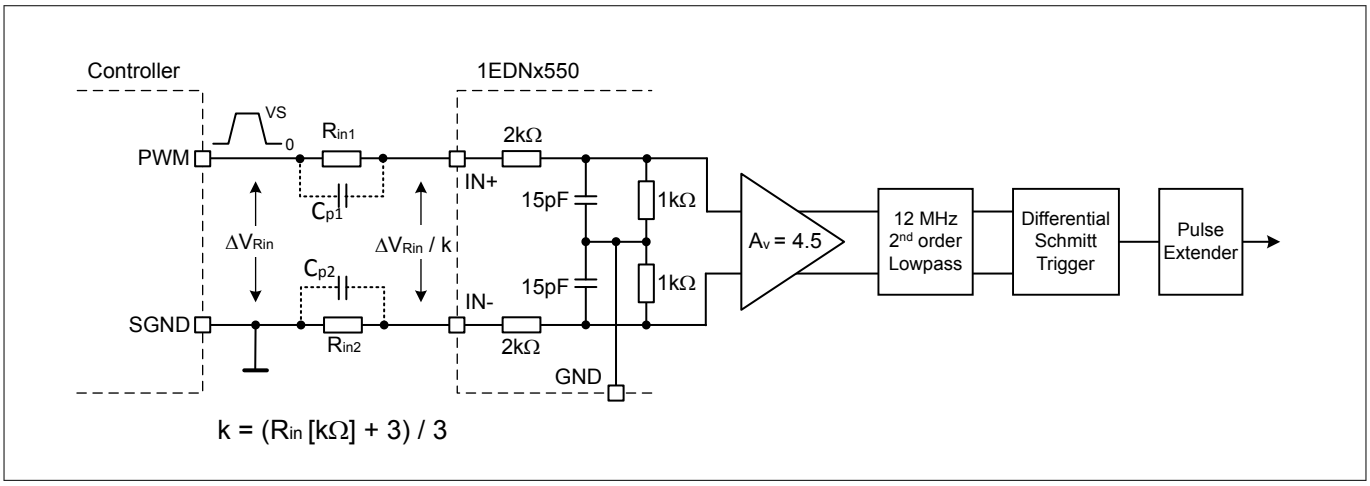

Figure 4 1EDNx550 input signal path

The controller output signal, switching between controller supply VS and zero, is applied at the one leg of a differential voltage divider, while the other is connected to the controller ground SGND. The divider ratio has to be adapted to VS to allow a fixed Schmitt-Trigger threshold voltage. For VS = 3.3 V, R_{in1} and R_{in2} are chosen to be 33 kΩ, resulting in a static divider ratio of k = 12 at the driver inputs and 36 at the internal voltage amplifier. With VS other than 3.3 V, R_{in} has to fulfil the relation: $R_{in1} = R_{in2} = 10.9\ VS - 3\ [k\Omega]$

Amplified by a factor of 4.5, the signal is filtered by a 2nd order low-pass filter. Taking into account the RC filter in front of the amplifier, the overall input path exhibits the frequency behavior of a 3rd order low-pass filter with a corner frequency around 12 MHz. The suppression of high frequencies is important for two reasons. Inductive common-mode ringing in fast-switching power systems is typically in the 100 MHz and above range and thus is effectively damped. The high-frequency symmetry of the voltage divider is influenced by parasitic capacitances, particularly C_{p1} and C_{p2}, the parallel capacitances of R_{in1} and R_{in2}. They are typically in the 50 to 100 fF range, rather independent of resistor size. Without filtering, any asymmetry would translate high-frequency common-mode into differential signals.

The filtered signal is then applied to a differential Schmitt-Trigger with accurate trimmed threshold levels and converted to the logic switch control signal. The subsequent pulse extender function guarantees that no pulses shorter than 25 ns are transmitted to the output, thereby further improving noise immunity.

Due to the filtering requirements the input-to-output propagation delay is slightly increased to around 45 ns. By means of on-chip trimming, however, the usually more relevant propagation delay variation can still be kept low at +10 / -7 ns.

3.1.1 Common mode input range

There are two effects limiting the common-mode input range, i.e. the maximum allowed voltage difference between controller outputs PWM/SGND and driver reference GND: the circuit and technology-related input voltage restrictions and the finite common-mode rejection in the input signal path due to asymmetries.

The static voltage range at the input pins is limited to + 6 / - 7 V to guarantee accurate linear operation of the input circuitry. Taking into account the proposed DC voltage divider ratio, this translates to a static common-mode range of + 72 / - 84 V. This range, however, is increased, if the high-frequency common-mode voltages typical for inductive ringing in fast-switching power systems are considered, as in this case the maximum ratings at the input pins are applicable (± 10 V). Together with the frequency-dependence of the voltage divider ratio due to the input RC-filter this leads to a usable dynamic common-mode range of ± 150 V.

The second limitation results from the fact that any imbalance in the signal path converts a common-mode to a differential signal. To utilize the full common-mode range as calculated above, the high accuracy of the trimmed on-chip network must not be affected by the external voltage divider resistors. This condition is easily fulfilled when choosing R_{in1} and R_{in2} with 0.1% tolerance; resistors with only 1% accuracy, however, would reduce the common-mode range significantly to ± 40 V.

3.2 Driver outputs

The rail-to-rail driver output stage realized with complementary MOS transistors is able to provide a typical 4 A sourcing and 8 A sinking current. The low on-resistance coming together with high driving current is particularly beneficial for fast switching of very large MOSFETs. With a R_{on} of 0.85 Ω for the sourcing pMOS and 0.35 Ω for the sinking nMOS transistor the driver can be considered in most applications to behave like an ideal switch. The p-channel sourcing transistor allows real rail-to-rail behavior without suffering from the source-follower's voltage drop typical for n-channel output stages.

In case of floating inputs or insufficient supply voltage the driver output is actively clamped to the “low” level (GND).

3.3 Supply voltage and Undervoltage Lockout (UVLO)

The Undervoltage Lockout function ensures that the output can be switched only, if the supply voltage V_{DD} exceeds the UVLO threshold voltage. Thus it can be guaranteed that the switch transistor is not operated, if the driving voltage is too low to achieve a complete and fast transition to the "on" state, thereby avoiding excessive power dissipation.

1EDNx550 is available in two versions differing in UVLO threshold to support switches with a broad range of threshold voltages

- 1EDN7550 with a typical UVLO threshold of 4.2 V (0.3 V hysteresis)
- 1EDN8550 with a typical UVLO threshold of 8 V (1 V hysteresis)

In addition, the high maximum V_{DD} of 20 V makes the driver family well suited for a broad variety of power switch types.

4 Electrical characteristics and parameters

The absolute maximum ratings are listed in ***Table 3*** . Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.1 Absolute maximum ratings

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	-0.3	–	22	V	Voltage between VDD to GND
Voltage at pins IN+ and IN-	V_{IN}	-10	–	10	V	–
Voltage at pins OUT_SRC and OUT_SNK	V_{INPUT}	-0.3	–	V_{DD}+0.3	V	–
Peak reverse current at OUT_SRC	I_{SRC_rev}	-5	–	–	A	< 500 ns
Peak reverse current at OUT_SRC	I_{SRC_rev}	–	–	5	A	< 500 ns
Junction temperature	T_j	-40	–	150	°C	–
Storage temperature	T_S	-55	–	150	°C	–
ESD capability	V_{ESD_HBM}	–	–	2	kV	Human Body Model (HBM)[1)]
ESD capability	V_{ESD_CDM}	–	–	0.5	kV	Charged Device Mode (CDM)

1 According to EIA/JESD22-A114-B (discharging 100 pF capacitor through 1.5 kΩ resistor)

4.2 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction-ambient[2]	R_{thJA25}	–	170	–	K/W	–
Thermal resistance junction-case (top)[3]	R_{thJC25}	–	81	–	K/W	–
Thermal resistance junction-board[4]	R_{thJB25}	–	52	–	K/W	–
Characterization parameter junction-case (top)[5]	Ψ_{thJC25}	–	14	–	K/W	–
Characterization parameter junction-board[6]	Ψ_{thJB25}	–	51	–	K/W	–

4.3 Operating range

Table 5 Operating Range

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	4.5	–	20	V	Min defined by UVLO
Voltage at pins IN+ and IN-	V_{IN}	-7	–	6	V	–
Junction temperature	T_j	-40	–	150	°C	[7]

2 Obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a

3 Obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88

4 Obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8

5 Estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining R_{th}, using a procedure described in JESD51-2a (sections 6 and 7)

6 Estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining R_{th}, using a procedure described in JESD51-2a (sections 6 and 7)

7 Continuous operation above 125°C may reduce life time

4.4 Electrical characteristics

Unless otherwise noted, min./max. values of characteristics are the lower and upper limits respectively. They are valid within the full operating range. The supply voltage is V_{VDD}= 12 V. Typical values are given at T_j=25°C.

Table 6 Power Supply

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
V_{DD} quiescent current	I_{VDDh}	–	0.86	–	mA	OUT = high
V_{DD} quiescent current	I_{VDDl}	–	1.06	–	mA	OUT = low

Table 7 Undervoltage Lockout 1EDN7550 (Logic level MOSFET)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold	$UVLO_{on}$	3.9	4.2	4.5	V	–
Undervoltage Lockout (UVLO) turn off threshold	$UVLO_{off}$	–	3.9	–	V	–
UVLO threshold hysteresis	$UVLO_{hys}$	0.25	0.3	0.35	V	–

Table 8 Undervoltage Lockout 1EDN8550 (Standard MOSFET)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold	$UVLO_{on}$	7.4	8.0	8.6	V	–
Undervoltage Lockout (UVLO) turn off threshold	$UVLO_{off}$	–	7.0	–	V	–
UVLO threshold hysteresis	$UVLO_{hys}$	0.8	1.0	1.2	V	–

Table 9 Inputs IN+, IN-

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Differential input voltage threshold for transition LH at input resistor	ΔV_{RinH}	–	1.7	–	V	Independent of V_{DD} R_{in1}/R_{in2} = 33 kΩ [8]
Differential input voltage threshold for transition HL at input resistor	ΔV_{RinL}	–	1.5	–	V	Independent of V_{DD} R_{in1}/R_{in2} = 33 kΩ [8]
Total input resistance on each leg	R_{in1} / R_{in2}	–	36	–	kΩ	R_{in1}/R_{in2} = 33 kΩ [8]

8 See ***Figure 1***

Table 10 Static Output Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High-level (sourcing) 0utput resistance	R_{on_SRC}	–	0.85	–	Ω	I_{SRC} = 50 mA
High-level (sourcing) output current	I_{SRC_peak}	–	4.0	9)	A	–
Low-level (sinking) output resistance	R_{on_SNK}	–	0.35	–	Ω	I_{SNK} = 50 mA
Low-level (sinking) output current	I_{SNK_Peak}	–	-8.0	10)	A	–

For an illustration of the dynamic characteristics see ***Figure 5*** and ***Figure 6***

Table 11 Dynamic Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input-to-output propagation delay	t_{PDon}	38	45	55	ns	C_{LOAD}= 200 pF, V_{DD}= 12 V
Input-to-output propagation delay	t_{PDoff}	38	45	55	ns	C_{LOAD}= 200 pF, V_{DD}= 12 V
Rise time	t_{rise}	—	6.5	15 11)	ns	C_{LOAD}= 1.8 nF, V_{DD}= 12 V
Fall time	t_{fall}	—	4.5	15 11)	ns	C_{LOAD}= 1.8 nF, V_{DD}= 12 V
Rise time	t_{rise}	—	1	5 11)	ns	C_{LOAD}= 200 pF, V_{DD}= 12 V
Fall Time	t_{fall}	—	1	5 11)	ns	C_{LOAD}= 200 pF, V_{DD}= 12 V
Minimum input pulse width that changes output state	t_{PW}	—	25	—	ns	C_{LOAD}= 1.8 nF, V_{DD}= 12 V

9 Actively limited by design to approx. 5.2 A_{pk}, parameter is not subject to production test - verified by design / characterization

10 Actively limited by design approx. -10.4 A_{pk}, parameter is not subject to production test - verified by design / characterization

11 Parameter verified by design, not 100% tested in production

4.5 Timing diagram

Figure 5 depicts rise, fall and delay times as given in the ***Chapter 4***.

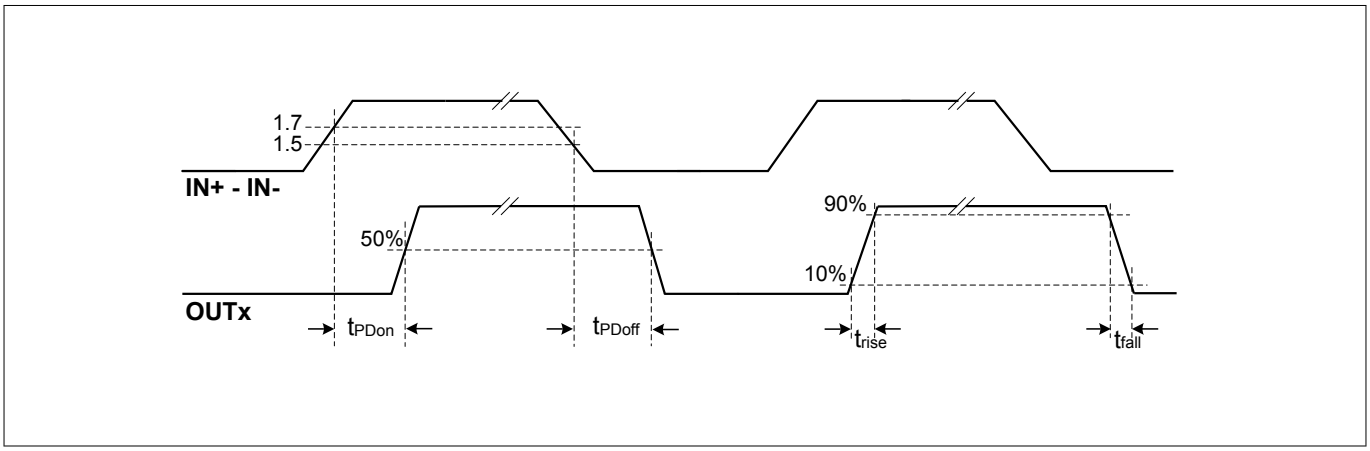

Figure 5 Propagation delay, rise and fall time

Figure 6 illustrates the Undervoltage Lockout function.

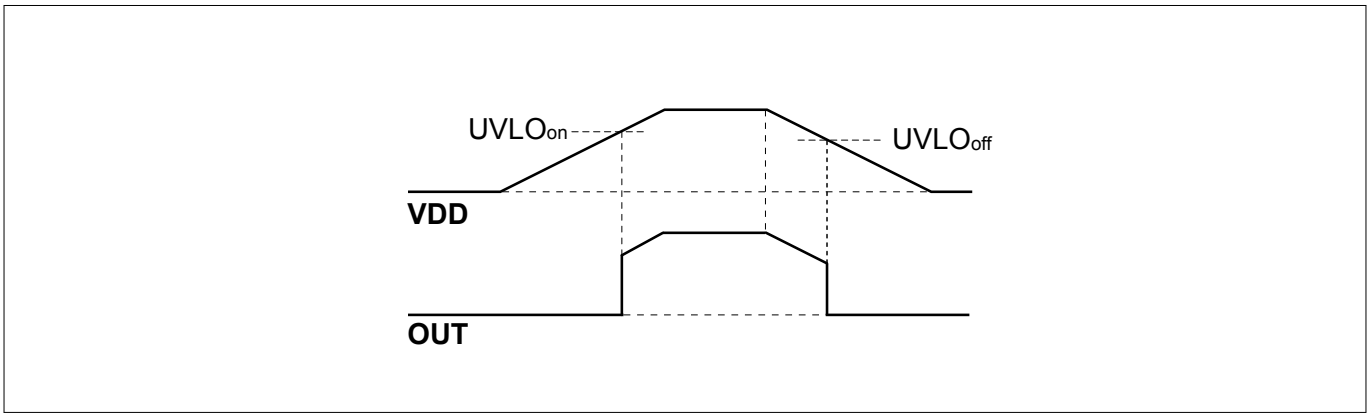

Figure 6 UVLO Behavior (output state high)

5 Typical characteristics

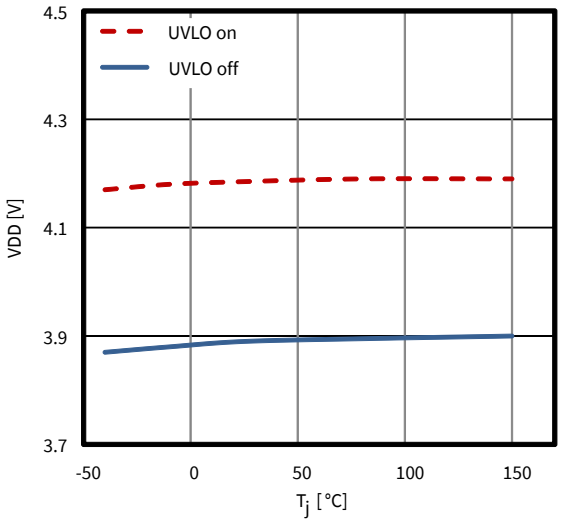

Figure 7 Undervoltage Lockout threshold (1EDN7550) vs temperature

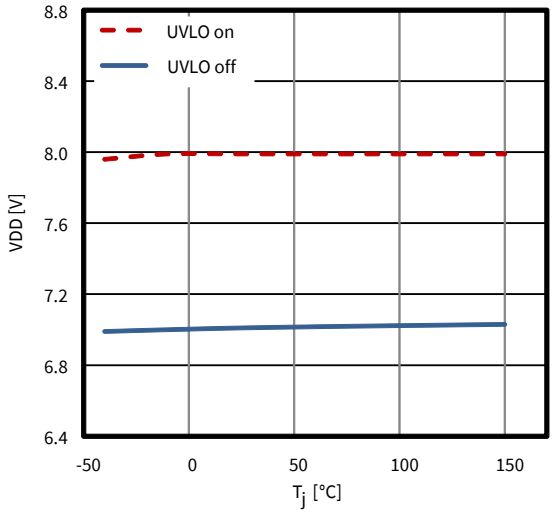

Figure 8 Undervoltage Lockout threshold (1EDN8550) vs temperature

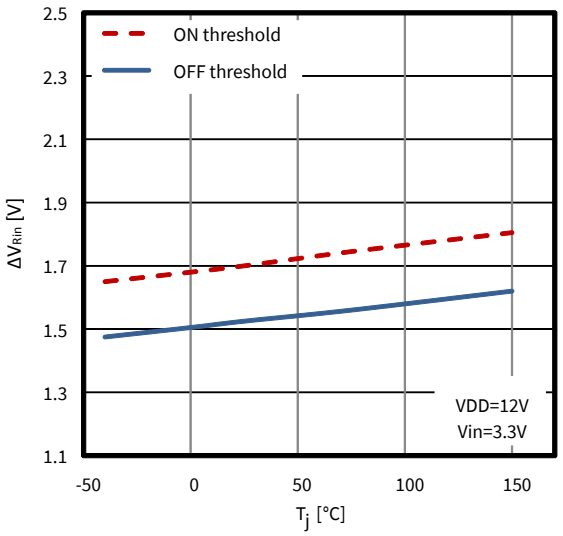

Figure 9 Differential input voltage threshold vs temperature

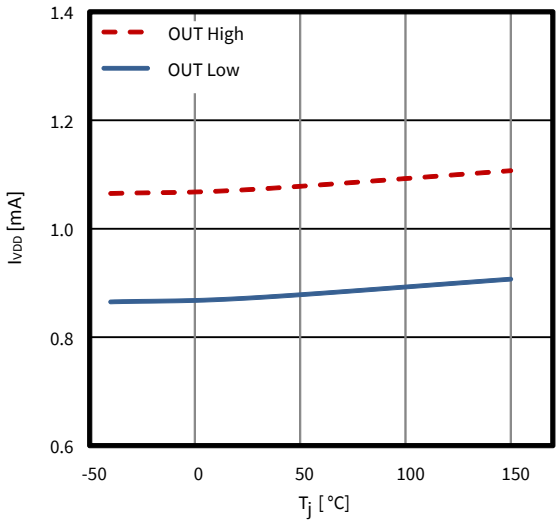

Figure 10 Typical quiescent current vs temperature

Typical characteristics

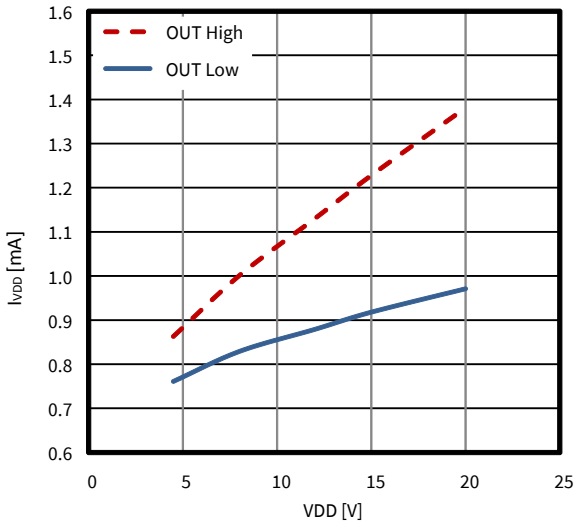

Figure 11 Typical quiescent current vs supply voltage

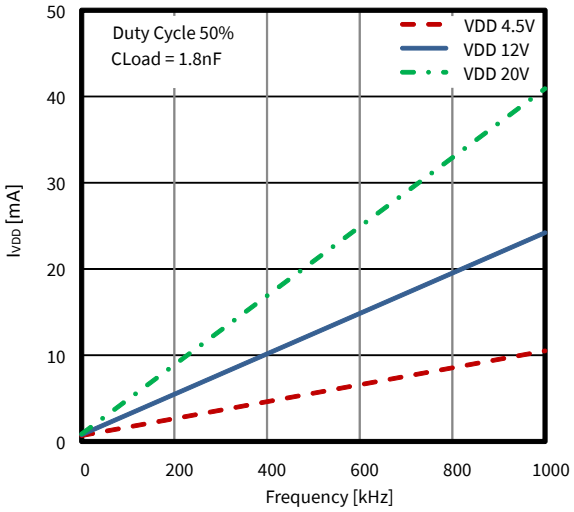

Figure 12 Total operating current consumption with capacitive load vs frequency

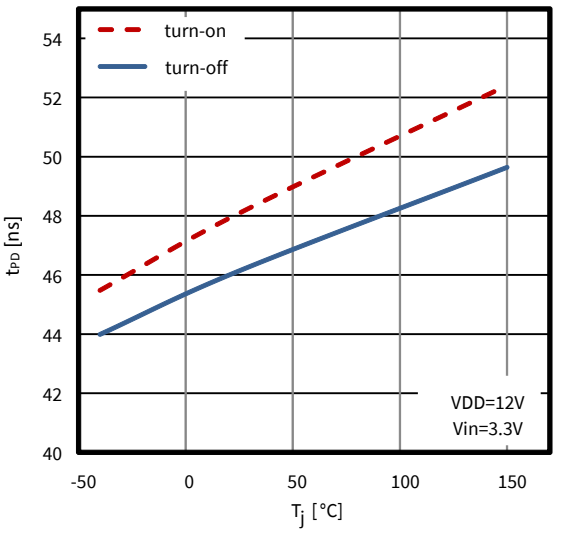

Figure 13 Typical propagation delay vs temperature

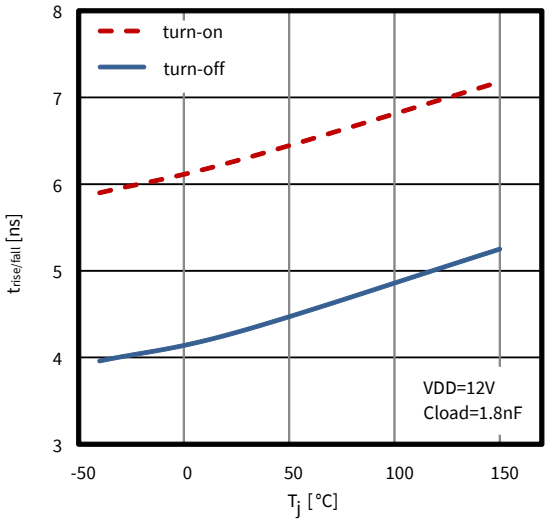

Figure 14 Typical rise and fall time vs temperature

6 Typical applications

6.1 Switches with Kelvin source connection (4-pin packages)

This is one of the key target applications of 1EDNx550. The 4-pin configuration depicted in ***Figure 15*** is a very effective measure to improve the switching performance of transistors in packages with high source inductance L_S as is typical for the widely used TO-packages. Although the Kelvin Source connection SS solves the problem of the largely increased switching losses due to L_S, it is evident, that the gate driver reference potential is moving by the inductive voltage drop v_{LS} with respect to the system ground SGND. In fast-switching applications at high current, v_{LS} can reach 100 V and above. This is why 4-pin systems so far either used isolated drivers or external filters with relatively low corner frequency that add significant signal delay. Now, however, 1EDNx550 provides an optimum solution for this case.

Figure 15 also indicates that the usually SGND-related VDD cannot be used directly as the driver supply. But due to the high frequency of v_{LS} (> 100 MHz), a filter composed of impedance Z_{VDD} together with the blocking cap C_{VDD} is well suited to generate a sufficiently stable driver supply. Z_{VDD} can be either a resistor (e.g. 22 Ω with a typical C_{VDD} of 1 µF) or, even better, a proper ferrite bead.

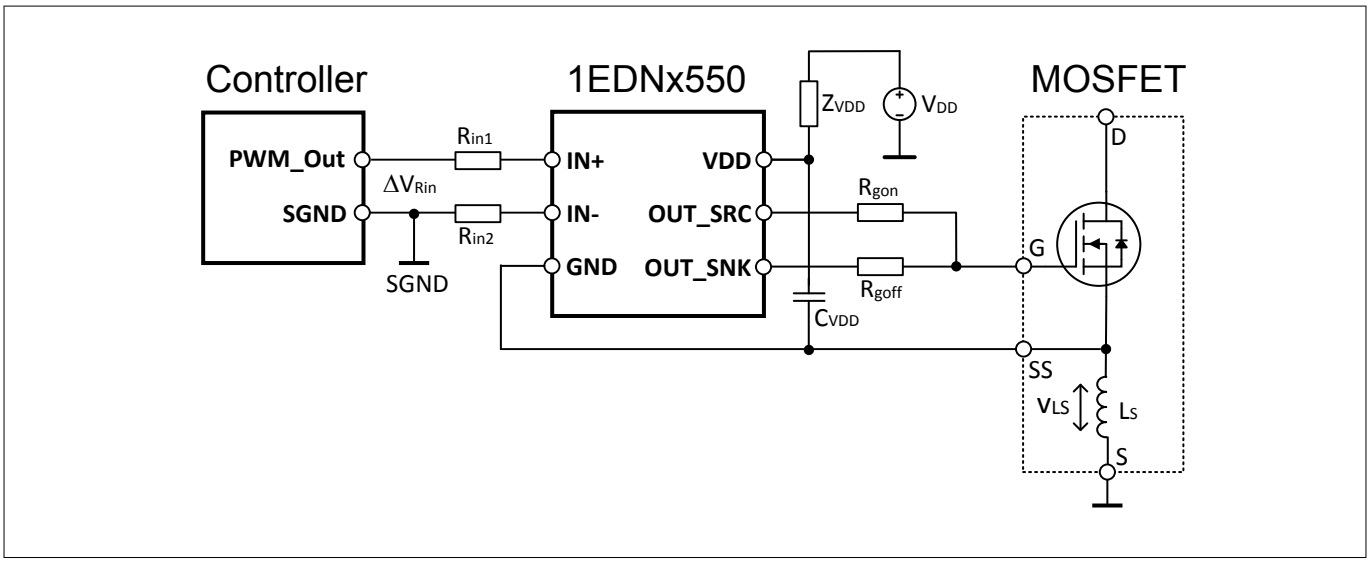

Figure 15 1EDN driving 4-pin MOSFET

6.2 Applications with significant parasitic PCB-inductances

In fast switching power systems the unavoidable parasitic inductance associated with any electrical connection may cause significant inductive voltage drops, particularly if the PCB-layout cannot be optimized, the most common reasons being limitations in the number of PCB-layers, geometric restrictions or also the lack of specific experience. In such situations the high robustness of 1EDNx550 with respect to “switching noise” (high-frequency voltage between reference potential of driver and controller) is extremely valuable and allows good performance even in systems with formerly critical layout. ***Figure 16*** indicates a respective example, indicating the most relevant parasitic PCB-inductances.

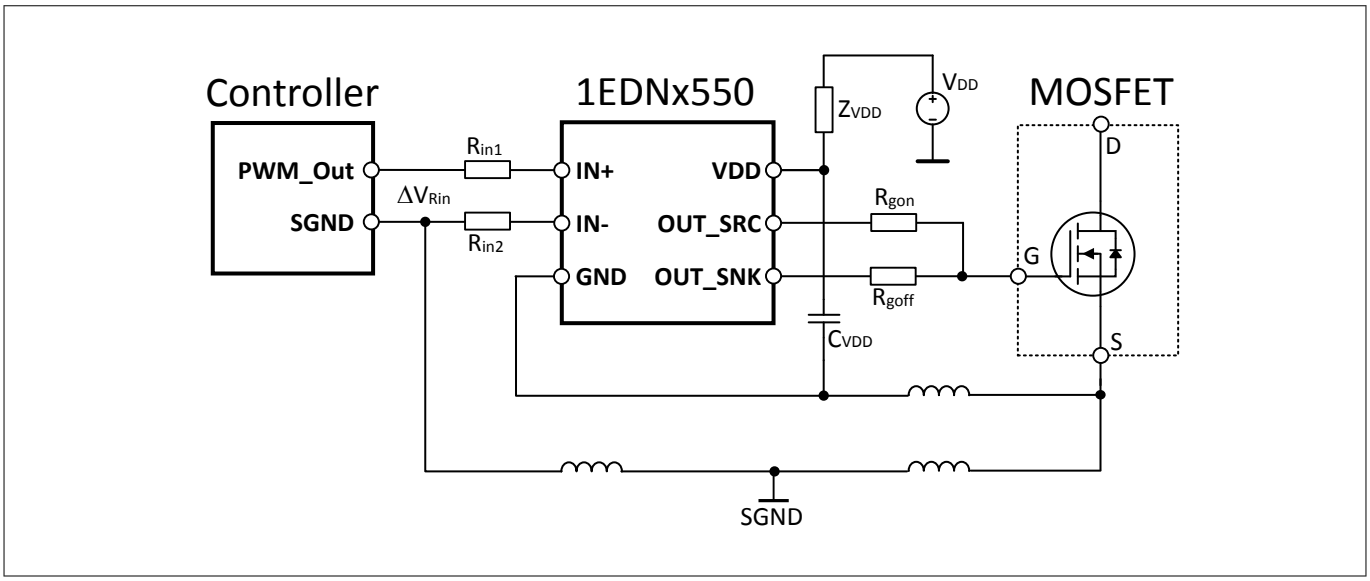

Figure 16 Application with significant PCB inductance

6.3 Switches with bipolar gate drive

Another application 1EDNx550 is tailored for, is driving power switches that require a negative gate-to-source voltage to safely hold them in the “off” state. Although MOSFETs are usually operated at zero “off” voltage, in certain situations a negative gate drive voltage can be very helpful. Particularly the fast switching “off” of high current when using switches with large common source inductance (e.g. in 3-pin TO-packages) may become critical in terms of losses and stability with a zero “off” level. In such cases a negative gate drive voltage is able to significantly improve switching performance. As depicted in ***Figure 17***, this kind of application is completely uncritical and handled easily with 1EDNx550, while standard drivers cannot be applied directly without adaptations.

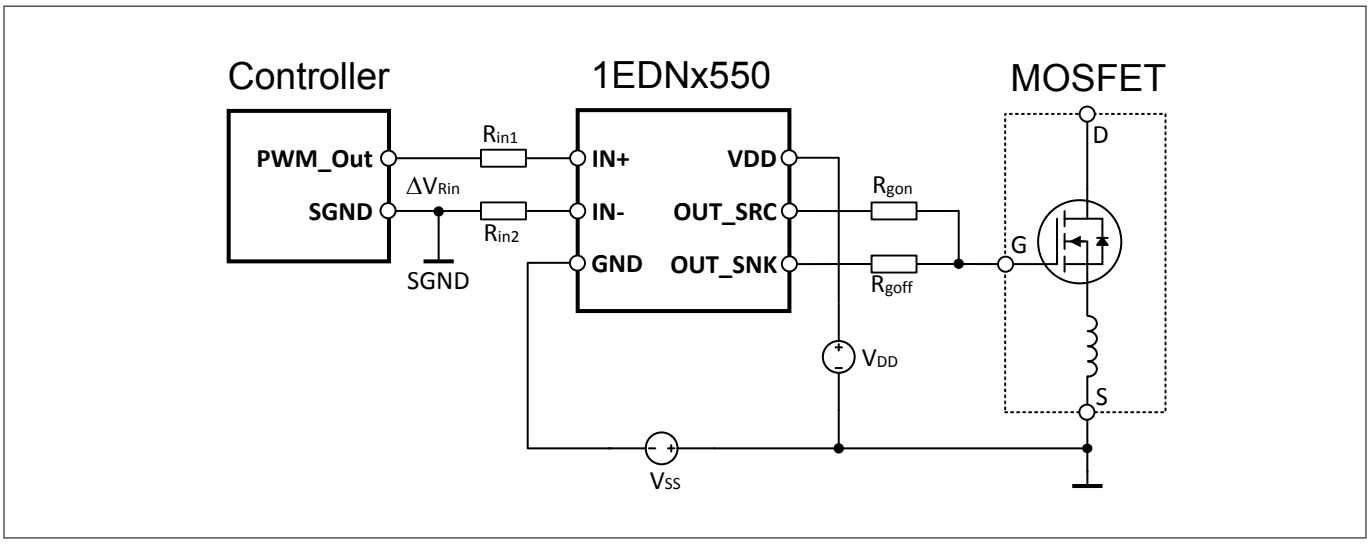

Figure 17 Bipolar gate drive for 3-pin MOSFET

6.4 High-side switches

Due to the large static input common-mode range, even driving high-side switches is an interesting application field for 1EDNx550. Although not providing galvanic isolation, 1EDNx550 can functionally be used as a high-side driver, as long as the power-loop voltage VP does not cause a violation of the allowed common-mode range.

In high-side operation as depicted in ***Figure 18***, the driver ground GND switches between zero (“off” state) and VP (“on" state) with respect to SGND; the resulting common-mode voltage at the driver input pins

(0 and –VP / 12, resp.) is restricted to - 7 V (***Table 5***) and by that limits VP to 84 V. In many applications the driver supply voltage can be generated by means of the well-known bootstrapping method also indicated in ***Figure 18***.

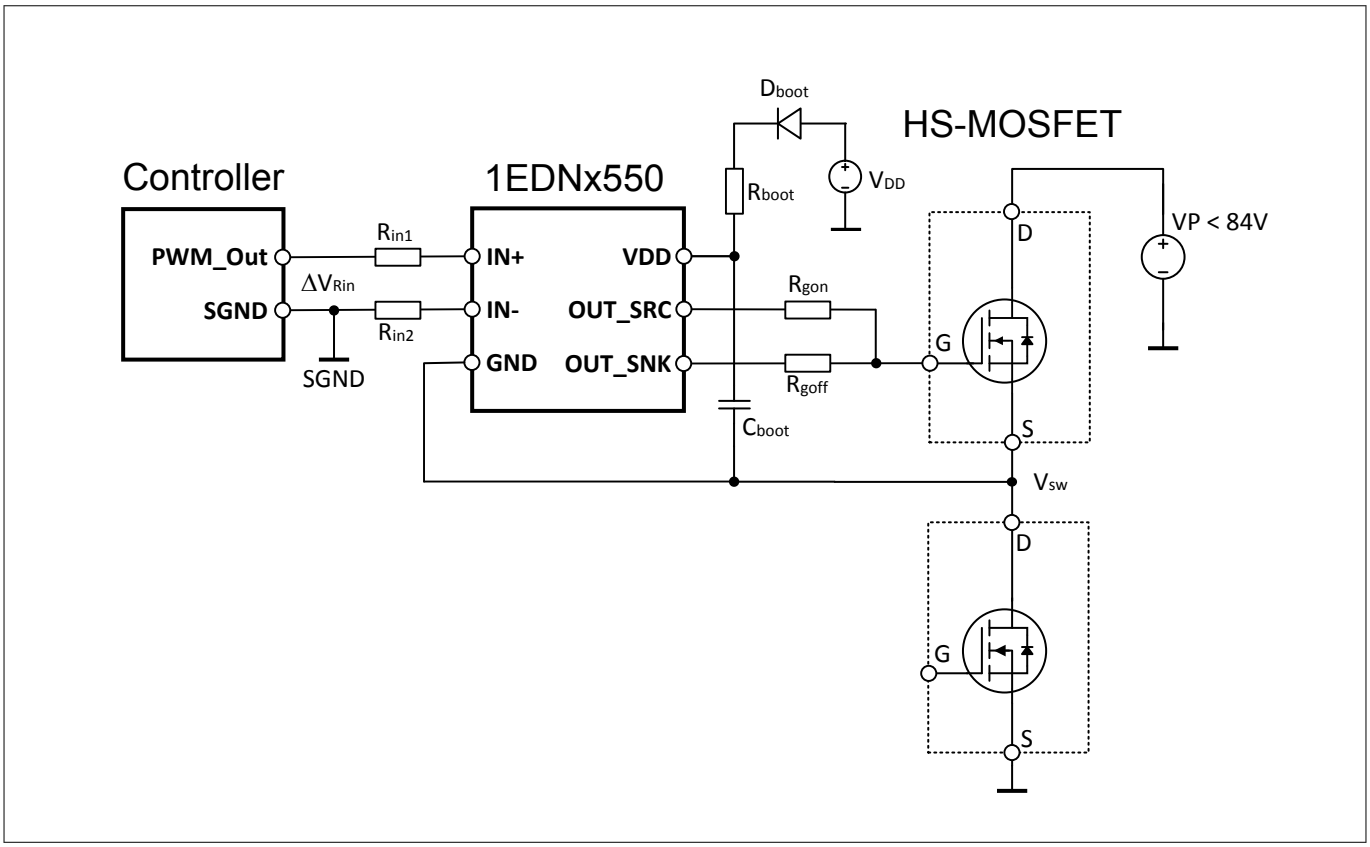

Figure 18 1EDNx550 as a high-side driver

7 Layout guidelines

It is well-known that the layout of a fast-switching power system is a critical task with strong influence on the overall performance. This is why there exists a huge number of rules, recommendations, guidelines, tips and tricks exist that should help to finally end up with a proper system layout.

With 1EDNx550 one of the central layout problems, namely the design of the grounding network, has become much less critical due to the highly reduced sensitivity of the differential concept with respect to ground voltage differences. So layout rules can be restricted to the following rather simple and evident ones:

- place input resistors R_{in} close to the driver and make layout of input signal path as symmetric and as compact as possible
- use a low-ESR decoupling capacitance for the VDD supply and place it as close as possible to the driver
- minimize power loop inductance as the most critical limitation of switching speed due to the resulting unavoidable voltage overshoots

A layout recommendation for the input path is given in ***Figure 19***.

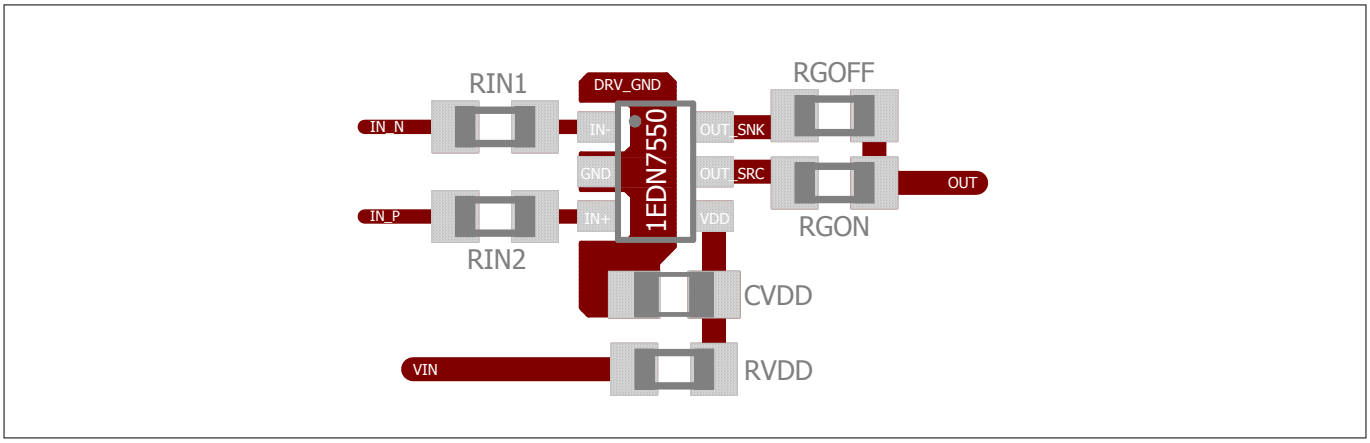

Figure 19 Layout recommendation

8 Package dimensions

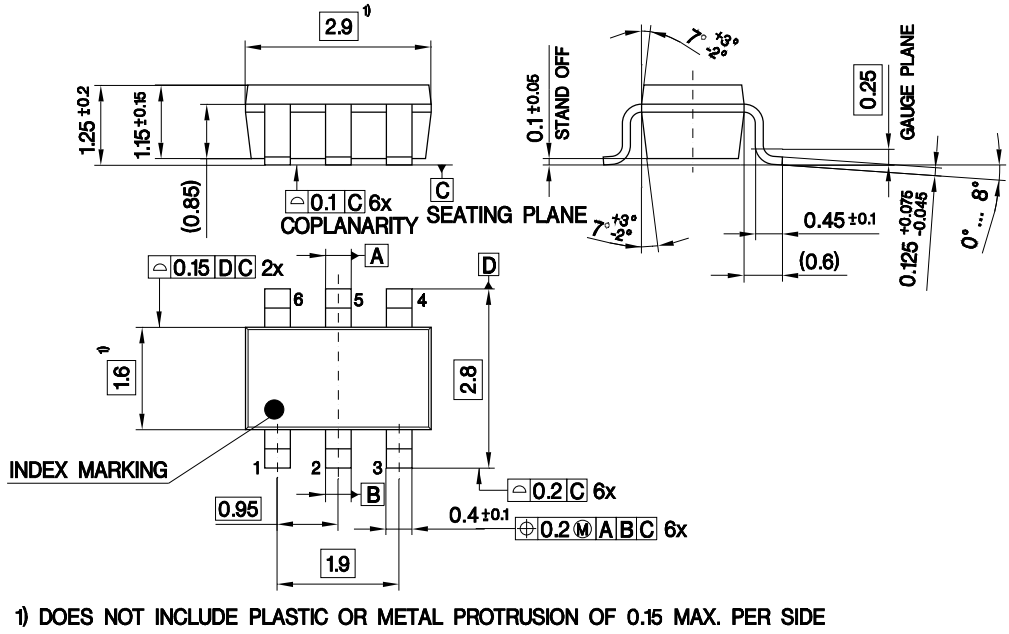

Figure 20 SOT23 6-pin outline dimensions

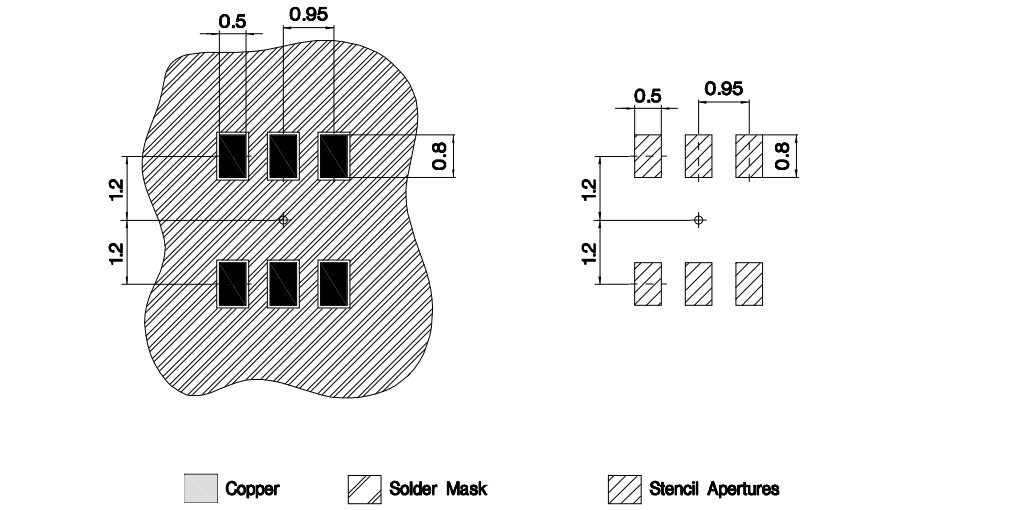

Figure 21 SOT23 6-pin footprint dimension

Package dimensions

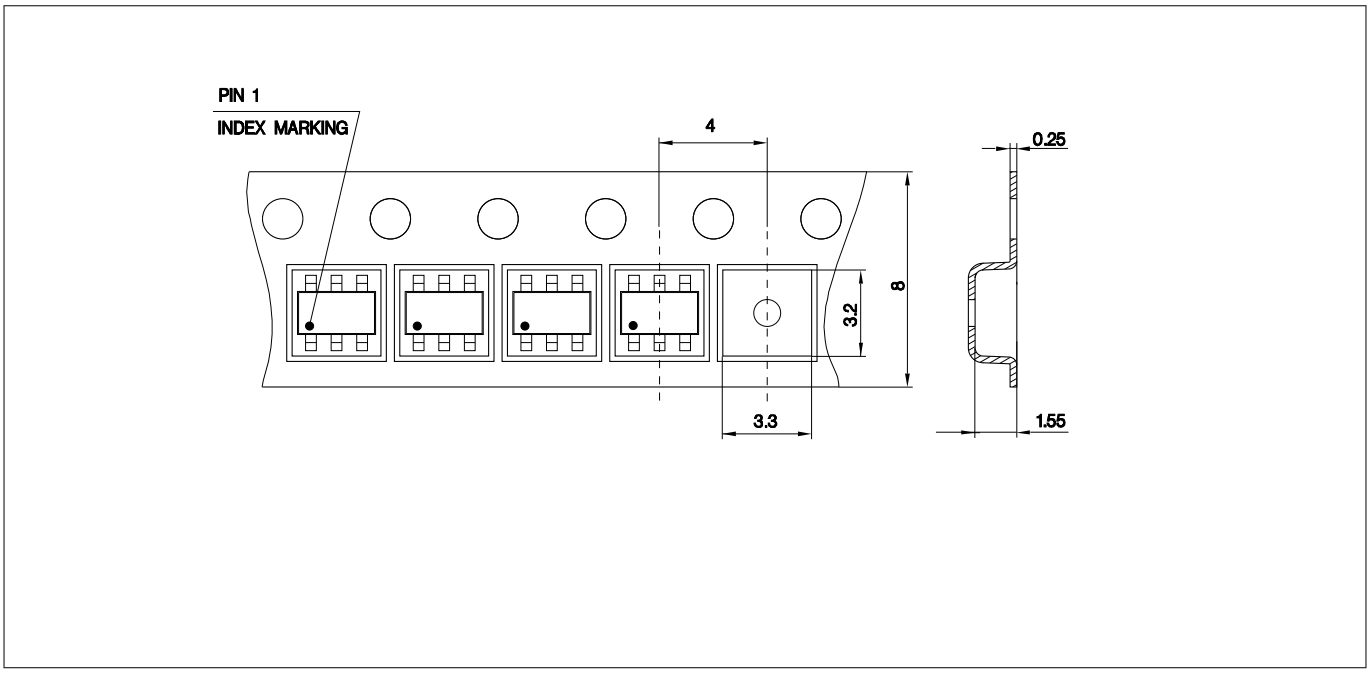

Figure 22 SOT23 6-pin packaging dimensions

Notes:

1. *For further details, please visit www.infineon.com/packages*

Revision history

Document version	Date of release	Description of changes
Rev. 2.0	2018-05-14	Final Datasheet created

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