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38V_{IN} Boost µModule Regulator for LED Drive with 10A Switch

FEATURES

- **Wide Input Voltage Range: 5V to 38V**
- **Supports Boost or SEPIC Power Topologies**
- **Adjustable LED Current Up to 1.6A**
- **40V 10A Internal Power Switch**
- **Wide Temperature Range: –40°C to 150°C**
- **Input and Output Current Reporting**
- **Internal Switch for PWM and Output Disconnect**
- **Internal Spread Spectrum Frequency Modulation**
- **3000:1 True Color PWM™ Dimming**
- Open LED Protection with OPENLED Flag
- Short-Circuit Protection and SHORTLED Flag
- Soft-Start with Programmable Fault Restart Timer
- 9mm × 11.25mm × 2.22mm BGA

APPLICATIONS

- High Power LED, High Voltage LED
- Accurate Current-Limited Voltage Regulators

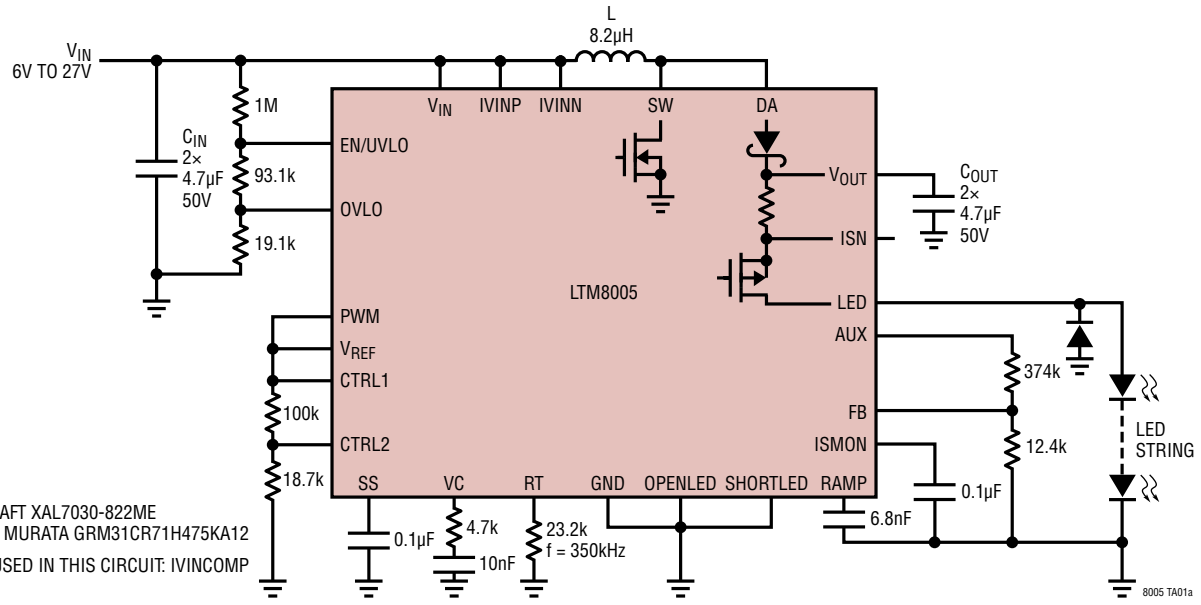
DESCRIPTION

The LTM®8005 is a 38V_{IN}, 38V_{OUT} boost µModule (power micromodule) LED driver designed to regulate current or voltage and is ideal for driving LEDs. The fixed frequency and current mode architecture result in stable operation over a wide range of supply and output voltages. Spread spectrum frequency modulation (SSFM) can be activated for improved electromagnetic compatibility (EMC) performance. The ground-referred voltage FB pin serves as the input for several LED protection features, and also allows the converter to operate as a constant voltage source. The PWM input provides LED dimming ratios of up to 3000:1, and the CTRL inputs provide additional analog dimming capability.

The low profile package enables utilization of unused space on the bottom of PC boards. The LTM8005 is packaged in thermally enhanced, compact over-molded Ball Grid Array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM8005 is RoHS compliant.

TYPICAL APPLICATION

350mA at 30.5V to 35.5V LED String from 6V to 27V V_{IN} (Boost) with Spread Spectrum



L: COILCRAFT XAL7030-822ME
C_{IN}, C_{OUT}: MURATA GRM31CR71H475KA12
PIN NOT USED IN THIS CIRCUIT: IVINCOMP

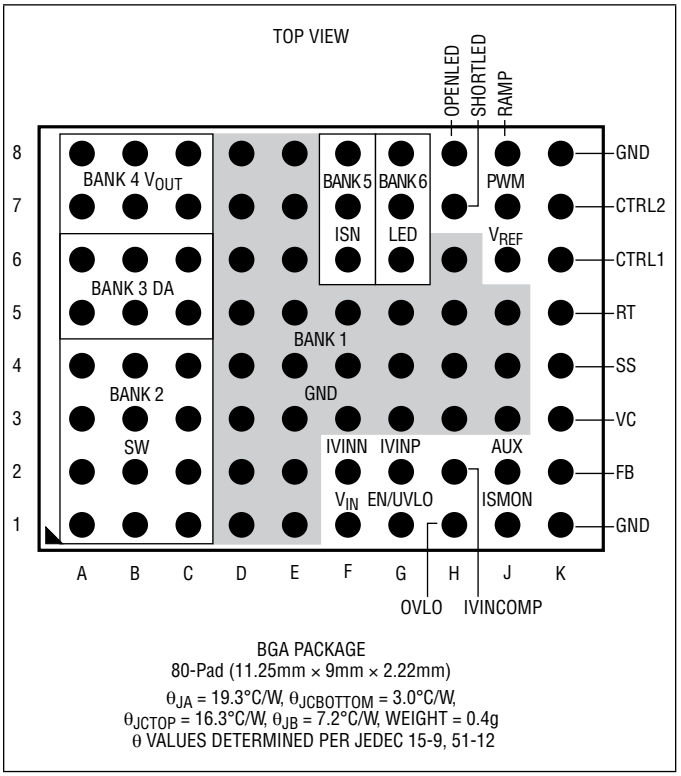
Rev A

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, EN/UVLO, IVINN, IVINP 50V
ISN Above LED.....40V
SW, ISN, LED, V_{OUT}, VOUT-DA.....40V
SW, ISN, LED, V_{OUT}, $V_{OUT} – D_A$..... 45V Transient
CTRL1, CTRL2 .....15V
PWM, SHORTLED, OPENLED 12V
FB, OVLO 8V
Maximum Junction Temperature
(E-Grade, I-Grade, MP-Grade) ..... 125°C
Maximum Junction Temperature (H-Grade)..... 150°C
Storage Temperature..... 150°C
Peak Solder Reflow Body Temperature ..... 260°C

PIN CONFIGURATION



BGA PACKAGE
80-Pad (11.25mm × 9mm × 2.22mm)
θ_{JA} = 19.3°C/W, $\theta_{JCBOTTOM}$ = 3.0°C/W,
θ_{JCTOP} = 16.3°C/W, θ_{JB} = 7.2°C/W, WEIGHT = 0.4g
θ VALUES DETERMINED PER JEDEC 15-9, 51-12

ORDER INFORMATION

Part Number	Terminal Finish	Part Marking*		Package Type	MSL Rating	Temperature Range
		Device	Finish Code			
LTM8005EY#PBF	SAC305 (RoHS)	LTM8005	e1	BGA	3	–40°C to 125°C
LTM8005IY#PBF	SAC305 (RoHS)	LTM8005	e1	BGA	3	–40°C to 125°C
LTM8005HY#PBF	SAC305 (RoHS)	LTM8005	e1	BGA	3	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *Device temperature grade is identified by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. CTRL1 = CTRL2 = PWM = 5V, unless otherwise noted (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●			5	V
LED DC Current	CTRL1 = 1.5V CTRL1 = 0.6V CTRL1 = 0.2V			1.65 0.8 0.16		A A A
SW Current Limit			10	12	14	A
SW $R_{DS(ON)}$				19		mΩ
ISMON Voltage	I_{LED} = 1.5A		0.88		0.96	V
Quiescent Current into V_{IN}	EN/UVLO = 0V (Disabled), PWM = 0V EN/UVLO = 1.15V, PWM = 0V RT = 82.5K to GND, FB = 1.5V (Not Switching)				35 40 3.5	µA µA mA
V_{REF} Voltage	I_{REF} = –100µA	●	1.95	2.00	2.08	V
V_{REF} Line Regulation	5V < V_{IN} < 48V			0.1		%
V_{REF} Load Regulation	–100µA < I_{REF} < 0µA			1		%
SS Current	Sourcing, SS = 0V Sinking, I_{LED} Overcurrent			28 2.8		µA µA
I_{LED} Overcurrent Threshold				2.4		A
ISN-LED $R_{DS(ON)}$				53		mΩ
VC Output Impedance				2000		kΩ
VC Standby Input Bias Current	PWM = 0V		–20		20	nA
VC Pin Current	VC = 1.2V, Sourcing VC = 1.2V, Sinking			10 30		µA µA
Voltage at FB pin		●	1.23	1.25	1.27	V
FB Amplifier g_m				500		µS
FB Pin Input Bias Current	Current Out of Pin, FB = V_{FB}				200	nA
FB OPENLED Threshold	OPENLED Falling		1.176		1.222	V
FB Overvoltage Threshold			1.26		1.34	V
FB SHORTLED Threshold	SHORTLED Falling			300	350	mV
LED Current C/10 Threshold				0.16		A
Input Current Limit Threshold	IVINP – IVINN		53		67	mV
IVINCOMP Voltage	IVINP – IVINN = 60mV			1.2		V
Switching Frequency	RT = 82.5k RT = 26.1k RT = 6.65k		85 240 800	105 300 1000	125 360 1200	kHz kHz kHz
Switching Frequency Modulation	RAMP = 2V			70		%
RAMP Input Low Threshold				1		V
RAMP Input High Threshold				2		V
RAMP Pin Source Current	RAMP = 0.4V			12		µA
RAMP Pin Sink Current	RAMP = 1.6V			12		µA
CTRL1, CTRL2 Pin Current	CTRL1, CTRL2 = 1V				200	nA
PWM Input Threshold Rising				1		V
PWM Pin Bias Current				10		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. CTRL1 = CTRL2 = PWM = 5V, unless otherwise noted (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
EN/UVLO Threshold Voltage Falling				1.22		V
EN/UVLO Threshold Voltage Rising				1.24		V
EN/UVLO Pin Bias Current	EN/UVLO = 1.15V, V_{IN} = 12V			19		µA
OPENLED Output Low	$I_{OPENLED}$ = 0.5mA				0.3	V
SHORTLED Output Low	$I_{SHORTLED}$ = 0.5mA				0.3	V
OVLO Threshold Voltage	Rising Falling		1.21 1.17		1.30 1.26	V V

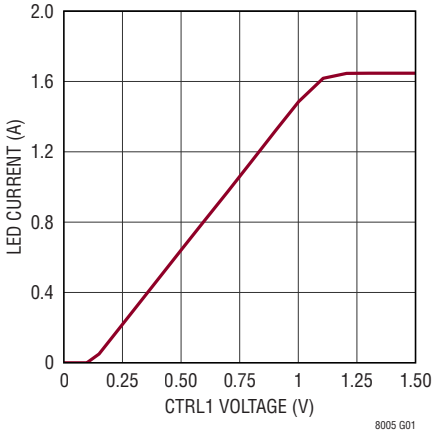
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM8005E is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8005I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM8005MP is guaranteed to meet specifications over the full –55°C to 125°C internal operating temperature range. The LTM8005H is guaranteed to meet specifications over the full –40°C to 150°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

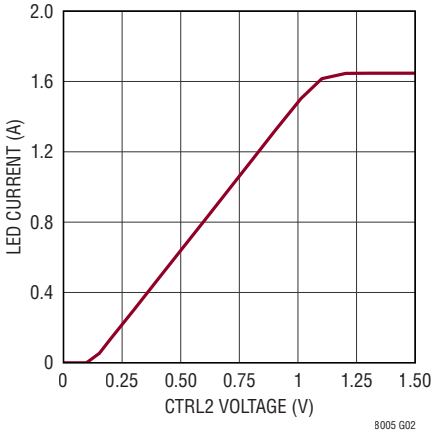
Note 3: The LTM8005 contains over-temperature protection that is intended to protect the device during momentary overload conditions. The internal temperature exceeds the maximum operating junction temperature when the over-temperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

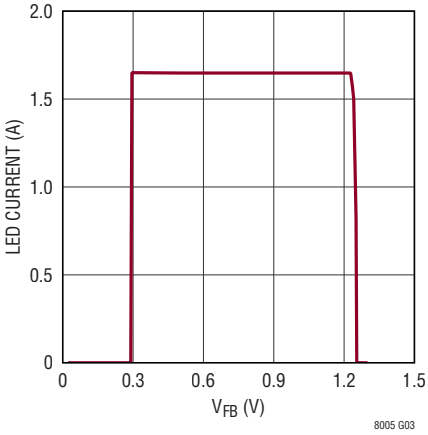
LED Current vs CTRL1



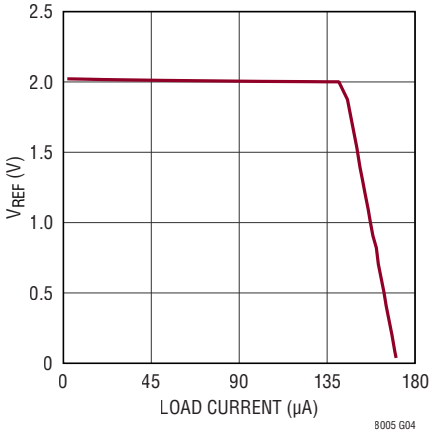
LED Current vs CTRL2



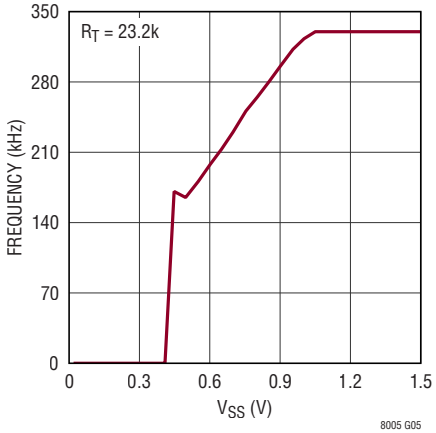
LED Current vs FB (CTRL1 = CTRL2 = V_{REF})



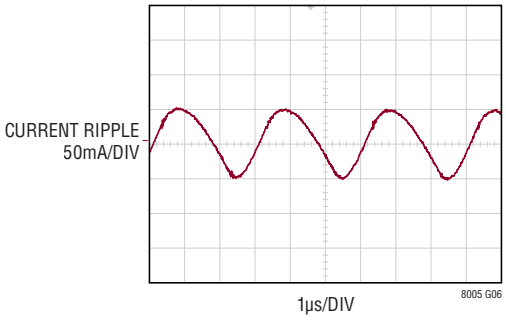
V_{REF} vs Load



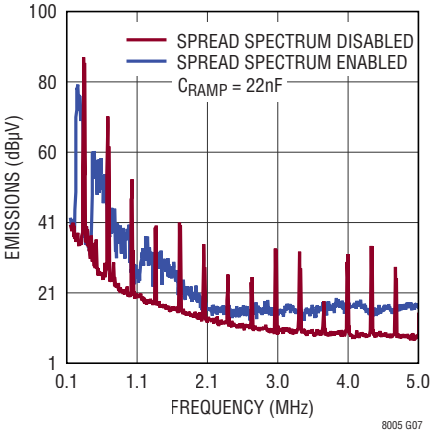
Switching Frequency vs SS Voltage



Demonstration Circuit DC2257A Output Current Ripple 34V at 1.2A LED, 12V_{IN}

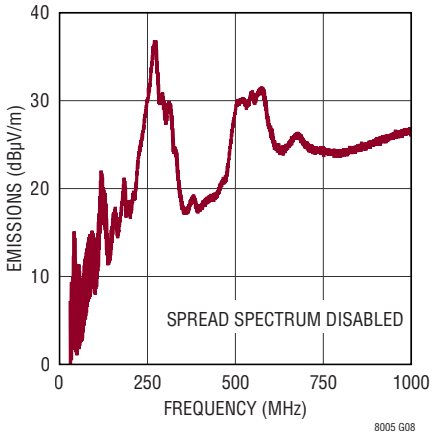


DC2257A Conducted EMI with and without Spread Spectrum Enabled

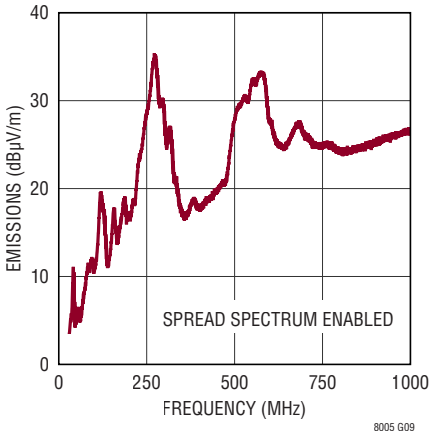


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

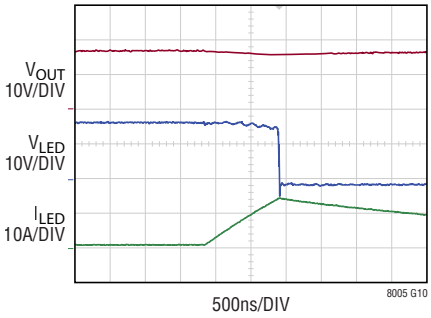
DC2257A CISPR 22 Radiated Results Without Spread Spectrum



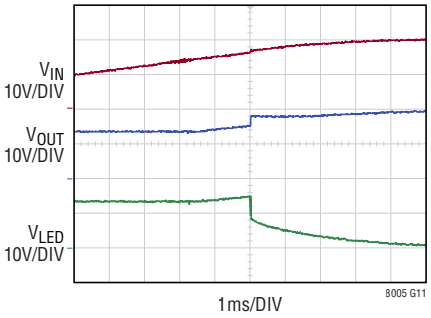
DC2257A CISPR 22 Radiated Results With Spread Spectrum



Output Disconnect Response (Short Circuit)



Output Disconnect Response (Input > Output)



PIN FUNCTIONS

GND (Bank 1, Pin K1, Pin K8): Tie these GND pins to a local ground plane below the LTM8005 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8005 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Return the feedback divider to this net.

SW (Bank 2): Power Switch Node. This is the drain of the internal power switching MOSFET. For boost, buck-boost mode and buck mode topologies, connect this bank to the inductor and the DA bank. For a SEPIC, connect this bank to an inductor winding and the positive coupling capacitor terminal.

DA (Bank 3): Power Diode Anode. For boost, buck-boost mode and buck mode topologies, connect this bank to the inductor and the SW bank. For a SEPIC, connect this bank to an inductor winding and the negative coupling capacitor terminal.

V_{OUT} (Bank 4): Power Output Pins. Apply the output filter capacitor between these pins and the GND pins.

ISN (Bank 5): Output Current Sense Resistor. The LTM8005 incorporates a sense resistor between V_{OUT} and ISN to set the output current regulation point and for output current monitoring. If a larger output current is required, apply an external resistor between V_{OUT} and ISN. Keep this pin voltage within 0.3V of V_{OUT}.

LED (Bank 6): LED Current Output. Connect the anode of the LED string to this bank.

V_{IN} (Pin F1): Input Power. The V_{IN} pin supplies current to the LTM8005's internal regulators and circuitry, and must be bypassed with a 0.22µF (or larger) capacitor placed close to the LTM8005.

IVINN (Pin F2): Input Sense Resistor Signal. Apply an external sense resistor between IVINP and IVINN to set the maximum input current and for input current monitoring. If this function is not required, tie both IVINP and IVINN to V_{IN}. Keep this pin voltage within 0.3V of V_{IN}.

EN/UVLO (Pin G1): Enable and Precision UVLO. An accurate 1.22V falling threshold with externally programmable hysteresis detects when power is OK to enable switching. Rising hysteresis is generated by the external resistor divider, an internal 499kΩ resistor between EN/UVLO and V_{IN} and an accurate internal 3µA pull-down current. Above the threshold, EN/UVLO input bias current is sub-µA. Below the falling threshold, a 3µA pull-down current is enabled so the user can optimize the hysteresis with the external resistor selection. An undervoltage condition resets soft-start. The EN/UVLO pin may be connected directly to V_{IN}, but do not drive this pin directly from another low impedance voltage source. If EN/UVLO must be driven from a voltage source, do so with at least a 50Ω series resistor.

IVINP (Pin G2): Input Sense Resistor Signal. Apply an external sense resistor between IVINP and IVINN to set the maximum input current and for input current monitoring. If this function is not required, tie both IVINP and IVINN to V_{IN}. Keep this pin voltage within 0.3V of V_{IN}.

OVLO (Pin H1): Input Overvoltage Lockout Pin. An accurate 1.25V rising threshold detects when power is OK to enable switching. If not used, tie this pin to GND.

IVINCOMP (Pin H2): Input Current Sense Amplifier Output Pin. The voltage at IVINCOMP pin is proportional to I_{IN} as $V_{IVINCOMP} = I_{IN} \bullet R_{INSNS} \bullet 20$. A 10nF capacitor to GND is provided internally at this pin to compensate the input current loop. Do not load this pin with a current and do not drive this pin with an external source, although additional capacitance may be added externally.

SHORTLED (Pin H7): An open-collector pull-down on SHORTLED asserts when any of the following conditions happen:

1. FB < 0.3V after SS pin reaches 1.7V at start-up.

2. LED overcurrent (I_{LED} > 2.4A).

To function, the pin requires an external pull-up resistor. SHORTLED status is only updated during PWM high state and latched during PWM low state. SHORTLED remains asserted until the SS pin is discharged below 0.2V. If not used, leave floating or tie to GND.

OPENLED (Pin H8): Fault Indicator. An open-collector pull-down on OPENLED asserts if the FB input is above 1.20V (typical), and the LED current is less than 0.16A (typical). To function, the pin requires an external pull-up

PIN FUNCTIONS

resistor. OPENLED status is updated only during PWM high state and latched during PWM low state. If not used, leave floating or tie to GND.

ISMON (Pin J1): LED Current Report Pin. The LED current is reported as V_{ISMON} = (LED current)/1.6. Leave the ISMON pin unconnected if not used. When PWM is low, ISMON is driven to ground. Bypass with a 47nF capacitor or higher if needed. Do not drive this pin with an external source.

AUX (Pin J2): Auxiliary Pin. This pin is internally connected to V_{OUT} to ease layout. Conveniently located next to FB, it is provided to simplify layout of the output voltage feedback network.

V_{REF} (Pin J6): Voltage Reference Output Pin. Typically 2.015V. This pin drives a resistor divider for the CTRL pins, either for analog dimming or for temperature limit/compensation of the LED load. It can supply up to 100µA. Do not drive this pin with an external source.

PWM (Pin J7): PWM Input Signal Pin. A low signal turns off switching, idles the oscillator, disconnects the VC pin from all internal loads, and disconnects the output load from V_{OUT}. PWM has an internal 500kΩ pull-down resistor. If not used, connect to V_{REF}.

RAMP (Pin J8): The RAMP pin is used for spread spectrum frequency modulation. The internal switching frequency is spread out to 70% of the original value, where the modulation frequency is set by 12µA/(2 • 1V • C_{RAMP}). If not used, tie this pin to GND.

FB (Pin K2): Voltage Loop Feedback Pin. FB is intended for constant-voltage regulation or for LED protection/open LED detection. The internal transconductance amplifier with output VC regulates FB to 1.25V (nominal) through the DC/DC converter. If the FB input is regulating the loop, and LED current is less than 0.15A (typical), the OPENLED pull-down is asserted. This action may signal an open LED fault. If FB is driven above 1.3V (by an external power supply spike, for example), the internal N-Channel MOSFET is turned off and the load is disconnected from V_{OUT} to protect the LEDs from an overcurrent event. Do not tie this pin to GND as the SHORTLED will be asserted and the part will be shut down.

VC (Pin K3): Transconductance Error Amplifier Output Pin. Used to stabilize the control loop with an RC network. This pin is high impedance when PWM is low, a feature that stores the demanded current state variable for the next PWM high transition. Connect a capacitor between this pin and GND; a resistor in series with the capacitor is recommended for fast transient response. Do not leave this pin open, and do not drive this pin with an external source.

SS (Pin K4): Soft-Start Pin. This pin modulates oscillator frequency and compensation pin voltage (VC). The soft-start interval is set with an external capacitor. The pin has a 28µA (typical) pull-up current source to an internal 2.5V rail. This pin can be used as fault timer. Provided the SS pin has exceeded 1.7V to complete a blanking period at start-up, the pull-up current source is disabled and a 2.8µA pull-down current is enabled when any one of the following fault conditions happen:

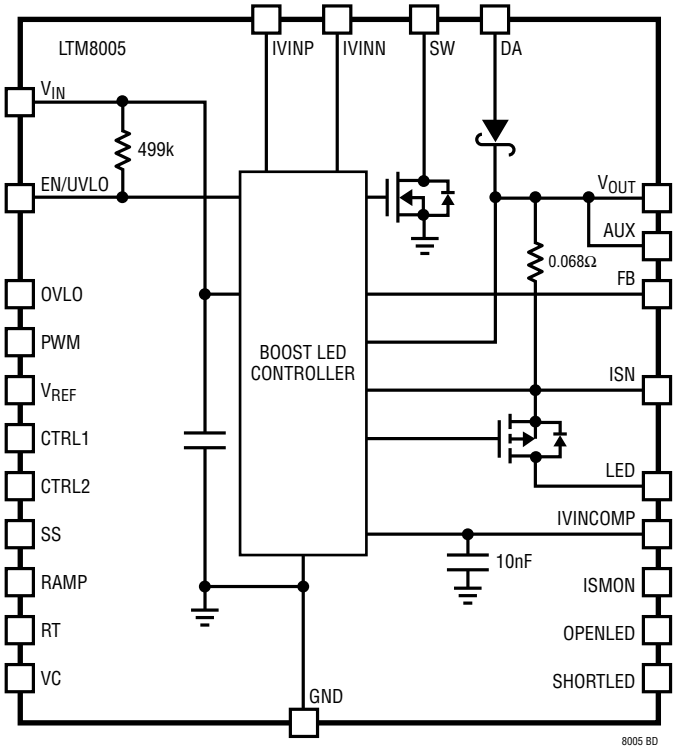
1. LED overcurrent (I_{LED} > 2.4A)
2. Output short (FB < 0.3V after start-up)
3. Thermal limit

The SS pin must be discharged below 0.2V to re-initiate a soft-start cycle. Switching is disabled until SS begins to recharge. It is important to select a capacitor large enough that FB can exceed 0.3V under normal load conditions before SS exceeds 1.7V. Do not leave this pin open and do not drive this pin with an external source.

RT (Pin K5): Switching Frequency Adjustment Pin. Set the frequency using a resistor to GND. Do not leave the RT pin open. Do not drive this pin with an external source.

CTRL1, CTRL2 (Pin K6, K7): Current Sense Threshold Adjustment. CTRL1 and CTRL2 have identical functions. The output current is regulated by CTRL1 or CTRL2. The pin with the lowest voltage takes precedence. For 0.1V < V_{CTRLx} < 1V the LED current is V_{CTRLx} • 1.5A less an offset. For V_{CTRLx} > 1.2V the current sense threshold is constant at the full-scale value of 1.6A. For 1V < V_{CTRLx} < 1.2V, the dependence of the current sense threshold upon V_{CTRLx} transitions from a linear function to a constant value, reaching 98% of full-scale value by V_{CTRLx} = 1.1V. Do not leave this pin open. If not used, tie to V_{REF}. Connect either CTRL pin to GND for zero LED current.

BLOCK DIAGRAM



OPERATION

The LTM8005 is a stand-alone non-isolated switching DC/DC regulator intended for LED driver applications. This µModule power converter provides a regulated current from an input voltage range of 5V to 38V, and up to 38V output. A simplified block diagram is provided in the previous section.

The LTM8005 is equipped with a ground referred power switch and a power rectifier. Connect external power devices, such as an inductor, to these pins to implement boost, buck-boost mode, buck mode or SEPIC topologies to drive a string of LEDs.

The LTM8005 features an integrated sense resistor to control the LED current. The maximum regulated current is 1.6A, and this can be reduced by applying a voltage less than 1.2V to the CTRL1 or CTRL2 pins. The output current is reported by the voltage on the ISMON pin.

The LTM8005 also features an integrated PMOS disconnect switch to implement PWM dimming that is controlled by a signal on the PWM pin. The PMOS also disconnects the LEDs during fault conditions.

If input current limiting is desired, apply an external sense resistor to the IVINP and IVINN pins. The full input current will flow through this external sense resistor, so choose a resistor with an appropriate power rating. The LTM8005 will start to decrease the power if the voltage between the IVINP and INVINN pins exceeds 60mV. A 10nF capacitor is provided internally to compensate the input current regulation loop, but additional capacitance may be added externally to further filter the voltage at the IVINCOMP pin.

The LTM8005 features spread spectrum frequency modulation, which causes the switching frequency to modulate to a frequency that is approximately 70% of the programmed value set by the RT resistor. This modulation decreases the energy emitted at a single frequency, reducing the EMI amplitude. The modulation behavior is set by a capacitor on the RAMP pin to GND.

Input voltage turn-on and turn-off thresholds are set by resistor networks at the EN/UVLO and OVLO pins. Applying a voltage of greater than 1.24V to the EN/UVLO pin enables the part.

OPENLED and SHORTLED are active low open drain status bits that indicate an open LED or shorted LED condition. OPENLED transitions to a logic low when the FB pin rises above 1.2V and the LED current decreases below 160mA. SHORTLED transitions to a logic low when the FB pin falls below 300mV or the LED current exceeds 2.4A. Further details on these and other functions are given in the Applications Information section.

An external soft start capacitor at the SS pin minimizes the current spike that occurs at start up and the SS pin also programs hiccup or latchoff mode fault protection.

The LTM8005 is equipped with a thermal shutdown that inhibits power switching at high junction temperatures. The activation threshold of this function is above the absolute maximum temperature rating to avoid interfering with normal operation, so prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the reliability of the device.

APPLICATIONS INFORMATION

Programming the Turn-On and Turn-Off Thresholds with the EN/UVLO Pin

The falling under-voltage lockout (UVLO) value can be accurately set by the resistor divider, as shown in Figure 1. A small 3µA pull-down current is active when EN/UVLO is below the threshold. The purpose of this current is to allow the user to program the rising hysteresis. The following equations should be used to determine the values of the resistors:

$$V_{IN(FALLING)} = 1.22 \bullet \frac{R1 \| 499k + R2}{R2}$$

$$V_{IN(RISING)} = V_{IN(FALLING)} + (3\mu A \bullet R1 \| 499k)$$

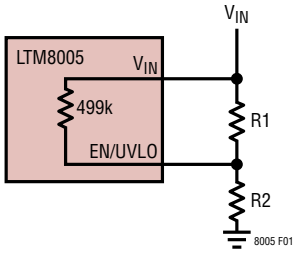


Figure 1. Set an Accurate UVLO with a Resistor Divider

Programming the Overvoltage Lockout Threshold with the OVLO Pin

The input overvoltage lockout protection feature can be implemented by a resistor from the V_{IN} to OVLO pins as shown in Figure 2. The following equations should be used to determine the values of the resistors:

$$V_{IN,OVLO} = 1.25 \bullet \frac{R3 + R4}{R4}$$

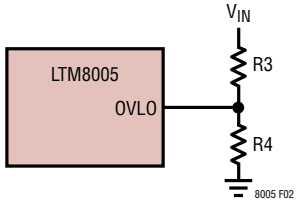


Figure 2. Set an Overvoltage Lockout Threshold with a Resistive Divider

LED Current Adjustment

The maximum output LED current is internally set to 1.6A, typical. If both CTRL pins are tied to a voltage higher than 1.2V, maximum current is available. If a voltage less than 1.2V is applied to either CTRL1 or CTRL2, the LED current will decrease. The two CTRL pins have identical functions. Whichever is the lowest takes precedence. Either CTRL pin can also be used to dim the LED current to zero, although relative accuracy decreases with the decreasing applied voltage sense threshold.

The CTRL pins should not be left open (tie to V_{REF} if not used). Either CTRL pin can also be used in conjunction with a thermistor to provide overtemperature protection for the LED load, or with a resistor divider to V_{IN} to reduce output power and switching current when V_{IN} is low.

Internal Power Switch Voltage Stress

The LTM8005 is equipped with an integrated ground referred N-channel power MOSFET whose drain is connected to the SW bank. The absolute maximum rating of the SW bank is 40V continuous, 45V transient. When using the LTM8005 in a boost power topology, the voltage stress on the SW bank is nominally a diode drop above V_{OUT}. In the SEPIC or buck-boost topologies, however, the voltage stress on the SW bank is substantially higher than V_{OUT}, nominally $V_{IN} + V_{OUT}$. Do not exceed the absolute maximum voltage of the SW bank under any operating condition.

Programming Output Voltage (Constant-Voltage Regulation) and Output Voltage Open LED and Shorted LED Thresholds

The LTM8005 has a voltage feedback pin FB that can be used to program a constant-voltage output. In addition, FB programming determines the output voltage that will cause OPENLED and SHORTLED to assert. For a boost

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LED driver, the output voltage can be programmed by selecting the values of R5 and R6 (see Figure 3) according to the following equation:

$$V_{OUT} = 1.25 \bullet \frac{R5 + R6}{R6}$$

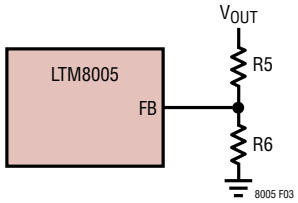

Figure 3. Set the OPENLED and SHORTLED Voltage Thresholds with Two Resistors

For a LED driver in buck-boost mode or buck mode configuration, the FB voltage is typically level shifted to a signal with respect to GND as illustrated in Figure 4. The output can be expressed as:

$$V_{OUT} = 1.25 \bullet \frac{R7}{R8} + V_{BE(Q1)}$$

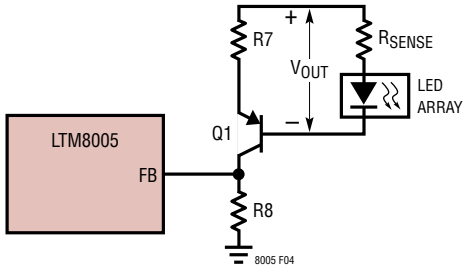

Figure 4. Level Shifting the FB Voltage is Commonly Used in Buck-Boost Mode or Buck Mode Configurations

If the open LED clamp voltage is programmed correctly using the resistor divider, then the FB pin should never exceed 1.2V when LEDs are connected. To detect both open-circuit and short-circuit conditions at the output, the LTM8005 monitors both output voltage and current. When FB exceeds 1.2V, OPENLED is asserted if the output current is less than about 160mA. OPENLED is deasserted when the output current increases above about 0.45A or FB drops below 1.19V (typical). The SHORTLED pin is asserted if the output current is about 2.4A or the FB pin falls below 300mV (typical) after initial start-up and SS reaches about 1.7V. The ratio between the FB OPENLED threshold of 1.2V and the SHORTLED threshold of 0.3V can limit the range of V_{OUT}. The range of V_{OUT} using the maximum SHORTLED threshold of 0.35V is about 3.5:1. The range of V_{OUT} can be made wider using the circuits shown in Figure 5 and Figure 6. For a V_{OUT} range that is greater than 8:1, consult factory applications.

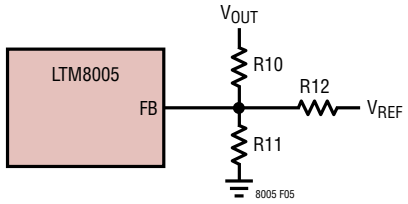

Figure 5. Feedback Resistor Connection for Wide Range Output in Boost and SEPIC Applications

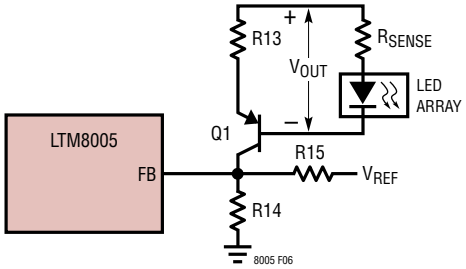

Figure 6. Feedback Resistor Connection for Wide Range Output in Buck-Boost Mode or Buck Mode Applications

The equations to widen the range of V_{OUT} are derived using a SHORTLED threshold of 0.35V, an OPENLED threshold of 1.2V and a reference voltage V_{REF} of 2V. The resistor values for R11 and R12 in Figure 5 can be calculated as shown below. See the example that follows for a suggested R10 value.

$$R11 = \frac{1.7 \bullet R10}{\left(1.65 \bullet V_{OUTMAX}\right) - \left(0.8 \bullet V_{OUTMIN}\right) - 1.7}$$

$$R12 = \frac{1.7 \bullet R10}{\left(0.35 \bullet V_{OUTMAX}\right) - \left(1.2 \bullet V_{OUTMIN}\right)}$$

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Example: Calculate the resistor values required to increase the V_{OUT} range of a boost LED driver to 7.5:1 and have OPENLED occur when V_{OUT} is 38V:

Step 1: Choose R10 = 374k

Step 2: V_{OUTMIN} = 38/7.5 = 5.1

Step 3:

$$R11 = \frac{1.7 \bullet 374k\Omega}{(1.65 \bullet 38) - (0.8 \bullet 5.1) - 1.7} = 11.2k\Omega$$

Use R11 = 11.3kΩ.

$$R12 = \frac{1.7 \bullet 374k\Omega}{(0.35 \bullet 38) - (1.2 \bullet 5.1)} = 88.6k\Omega$$

Use R12 = 88.7K.

The resistor values for R14 and R15 in Figure 6 can be calculated as shown below. See the example that follows for a suggested R13 value.

$$R14 = \frac{1.7 \bullet R13}{(1.65 \bullet V_{OUTMAX}) - (0.8 \bullet V_{OUTMIN}) - (0.85 \bullet V_{BE(Q1)})}$$

$$R15 = \frac{1.7 \bullet R13}{(0.35 \bullet V_{OUTMAX}) - (1.2 \bullet V_{OUTMIN}) - (0.85 \bullet V_{BE(Q1)})}$$

Example: Calculate the resistor values required to increase the V_{OUT} range of a buck-boost mode LED driver to 5:1 and have OPENLED occur when V_{OUT} is 17V. Use $V_{BE(Q1)}$ = 0.7V:

Step 1: Choose R13 = 187k

Step 2: V_{OUTMIN} = 17/5 = 3.4

Step 3:

$$R14 = \frac{1.7 \bullet 187k\Omega}{(1.65 \bullet 17) - (0.8 \bullet 3.4) - (0.85 \bullet 0.7)}$$

$$= 12.9k\Omega$$

Use R14 = 12.7kΩ

$$R15 = \frac{1.7 \bullet 187k\Omega}{(0.35 \bullet 17) - (1.2 \bullet 3.4) - (0.85 \bullet 0.7)}$$

$$= 249k\Omega$$

Use R15 = 249kΩ

LED Overcurrent Protection Feature

The LTM8005 has an overload protection feature independent of the output LED current regulation. This feature prevents the development of excessive switching currents and protects the power components. The overload protection threshold (2.4A typical) is designed to be 50% higher than the default LED current sense threshold. Once the LED overcurrent is detected, the internal power switch is turned off to stop switching, the PWM MOSFET is turned off to disconnect the LED array from the power path, and fault protection is initiated via the SS pin.

An anti-parallel Schottky or ultrafast diode D2 should be connected as shown in Figure 7 to protect the LED node from swinging well below ground when being shorted to ground through a long cable. The internal protection loop takes a finite amount of time to respond to the overload, so the diode is recommended if the system must survive an overload on the LED string.

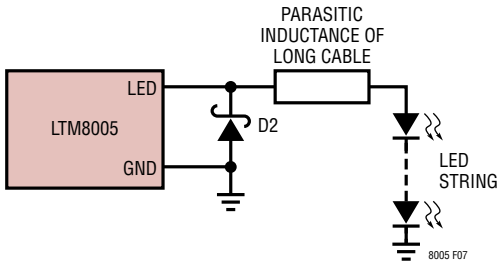

Figure 7. Connect an Anti-Parallel Diode D2 from LED to GND to Protect the LTM8005 from Negative Voltage Swings when the Connecting to a LED String through a Long Cable

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PWM Dimming Control for Brightness

There are two methods to control the LED current for dimming using the LTM8005. One method uses the CTRL pins to adjust the current regulated in the LEDs. A second method uses the PWM pin to modulate the LED current between zero and full current to achieve a precisely programmed average current, without the possibility of color shift that occurs at low current in LEDs. To make PWM dimming more accurate, the switch demand current is stored on the VC node during the quiescent phase when PWM is low. This feature minimizes recovery time when the PWM signal goes high. To further improve the recovery time, a disconnect MOSFET switch has been implemented to open the LED current path to prevent the output capacitor from discharging during the PWM signal low phase. The minimum PWM on or off time depends on the choice of operating frequency set by the RT input. For best current accuracy, the minimum recommended PWM high time should be at least three switching cycles (3µs for f_{SW} = 1MHz).

A low duty cycle PWM signal can cause excessive start-up times if it is allowed to interrupt the soft-start sequence. Therefore, once start-up is initiated by a PWM signal, the LTM8005 will ignore a logical disable by the external PWM input signal. The device will continue to soft-start with switching and TG enabled until either the voltage at SS reaches about 1V or the output current reaches one-fourth of the full-scale current. At this point the device will begin following the dimming control as designated by PWM. If at any time an output overcurrent is detected, the internal MOSFETs will be disabled even as SS continues to charge.

Programming the Switching Frequency

The RT frequency adjust pin allows the user to program the switching frequency from 100kHz to 1MHz to optimize efficiency/performance or external component size. Higher frequency operation yields smaller component size but increases switching losses and gate driving current, and may not allow sufficiently high or low duty cycle operation. Lower frequency operation gives better performance at the cost of larger external component size. For an appropriate RT resistor value see Table 1. An external resistor from the RT pin to GND is required—do not leave this pin open.

Table 1. Typical Switching Frequency vs R_T Value (1% Resistor)

f_{OSC}(kHz)	R_T(kΩ)
1000	6.65
900	7.50
800	8.87
700	10.2
600	12.4
500	15.4
400	19.6
300	26.1
200	39.2
100	82.5

Spread Spectrum Frequency Modulation

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve the EMI performance, the LTM8005 includes a spread spectrum frequency feature. If there is a capacitor (C_{RAMP}) at the RAMP pin, a triangle wave sweeping between about 1V and 2V is generated. This signal is then fed into the internal oscillator to modulate the switching frequency between about 70% of the base frequency and the base frequency, which is set by the RT resistor. The modulation frequency is set by 12µA/(2 • C_{RAMP}). The results of EMI measurements are sensitive to the RAMP frequency selected with the capacitor. 1kHz is a good starting point to optimize peak measurements, but some fine tuning of this selection may be necessary to get the best overall EMI results in a particular system. Consult factory applications for more detailed information about EMI reduction. The Typical Performance Characteristics section contains plots that show the LTM8005 conducted and radiated emissions with and without Spread Spectrum enabled.

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Duty Cycle Considerations

Switching duty cycle is a key variable defining converter operation; therefore, its limits must be considered when programming the switching frequency for a particular application. The fixed minimum on-time and minimum off-time and the switching frequency define the minimum and maximum duty cycle of the switch, respectively. When calculating operating limits, use typical room temperature values of 320ns and 290ns for minimum on-time and off-time, respectively.

Setting Input Current Limit

The LTM8005 has a standalone input current sense amplifier to limit the input current. The input current I_{IN} shown in Figure 8 is converted to a voltage output at the IVINCOMP pin. When the IVINCOMP voltage exceeds 1.2V the internal power switch is turned off, and the converter stops switching. The input current limit is calculated as follows:

$$I_{IN} = \frac{60mV}{R_{INSNS}}$$

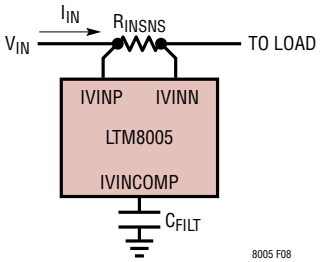

Figure 8. Apply a Current Sense Resistor Between IVINP and IVINN to Limit Input Current

Filter capacitor C_{FILT} shown in Figure 8 filters the voltage at the IVINCOMP pin to minimize ripple due to the input current. C_{FILT} also compensates the input current regulation loop, and is selected based on the loop response in addition to the intended voltage ripple on IVINCOMP. The IVINCOMP pin resistance to ground and C_{FILT} form a second pole in the input current regulation loop in addition to the dominant pole at VC pin. Suggested values for C_{FILT} of 10nF to 0.1µF will usually provide a second pole in the input current regulation loop that results in stable loop response and is equivalent to the second pole in the ISP/ISN regulation loop, which consists of the output capacitance C_{OUT} and the dynamic resistance of the LED load. The minimum C_{FILT} value of 10nF is integrated into the LTM8005.

Loop Compensation

The LTM8005 uses an internal transconductance error amplifier whose VC output compensates the control loop. The external inductor, output capacitor and the compensation resistor and capacitor determine the loop stability. The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor at VC are selected to optimize control loop response and stability. For typical LED applications, a 10nF compensation capacitor at VC is adequate, and a series resistor should always be used to increase the slew rate on the VC pin to maintain tighter regulation of LED current during fast transients on the input supply to the converter.

Soft-Start Capacitor Selection

For many applications, it is important to minimize the inrush current at start-up. The LTM8005 soft-start circuit significantly reduces the start-up current spike and output voltage overshoot. The soft-start interval is set by the soft-start capacitor (C_{SS}) selection according to the equation:

$$T_{SS} = C_{SS} \bullet 2V / 28\mu A$$

A typical value for the soft-start capacitor is 0.1µF. The soft-start pin voltage reduces the oscillator frequency and the maximum current in the switch. Soft-start also operates as fault protection, which forces the converter into hiccup or latchoff mode. Detailed information is provided in the Fault Protection: Hiccup Mode and Latchoff Mode section.

Fault Protection: Hiccup Mode and Latchoff Mode

If an LED overcurrent condition, internal $INTV_{CC}$ undervoltage, output short (FB ≤ 0.3V), or thermal limit happens, the integrated PMOS disconnect switch disconnects the LED array from the power path, and the integrated power switching MOSFET is turned off. If the soft-start pin is charging and still below 1.7V, then it will continue

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to do so with a 28µA source. Once above 1.7V, the pull-up source is disabled and a discharge current of about 2.8µA is activated. While the SS pin is discharging, the integrated switching MOSFET is turned off. When the SS pin is discharged below about 0.2V, a new cycle is initiated. This is hiccup mode operation. If the fault still exists when SS crosses below about 0.2V, then a full SS charge/discharge cycle has to complete before switching is enabled.

If a resistor, typically 402kΩ, is placed between the V_{REF} pin and SS pin to hold SS pin higher than 0.2V during a fault, then the LTM8005 will enter latchoff mode with switching stopped and the load disconnected from V_{OUT}. To exit latchoff mode, the EN/UVLO pin must be toggled low to high.

Capacitor Selection Considerations

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

Another precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8005. A ceramic input capacitor combined with trace or cable inductance forms a high Q (under damped) tank circuit. If the LTM8005 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Input Capacitor Selection

The input capacitor supplies the transient input current for the power inductor of the converter and must be placed and sized according to the transient current requirements. The switching frequency, output current and tolerable input voltage ripple are key inputs to estimating the capacitor value. An X7R type ceramic capacitor is a good choice because it has the least variation with temperature and DC bias. Typically, boost and SEPIC converters require a lower value capacitor than a buck mode converter.

In the buck mode configuration, the input capacitor has large pulsed currents due to the current returned through the Schottky diode when the switch is off. It is important to place the capacitor as close as possible to the Schottky diode and to the GND return of the switch. It is also important to consider the ripple current rating of the capacitor. For best reliability, this capacitor should have low ESR and ESL and have an adequate ripple current rating.

Output Capacitor Selection

The selection of the output capacitor depends on the load and converter configuration, i.e., step-up or step-down and the operating frequency. For LED applications, the equivalent resistance of the LED is typically low and the output filter capacitor should be sized to attenuate the current ripple. Use of an X5R or X7R type ceramic capacitor is recommended.

To achieve the same LED ripple current, the required filter capacitor is larger in the boost and buck-boost mode applications than that in the buck mode applications. Lower operating frequencies will require proportionately higher capacitor values. The component values shown in the data sheet applications are appropriate to drive the specified LED string. The product of the output capacitor and LED string impedance decides the second dominant pole in the LED current regulation loop. It is prudent to validate the power supply with the actual load (or loads).

Inductor Selection

The inductor used with the LTM8005 should have a saturation current rating appropriate to the peak inductor current under all expected operating conditions. Choose an inductor value based on operating frequency to provide a peak-to-peak inductor ripple current appropriate to the 12A (typical) switch current limit and duty cycle.

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PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8005. The LTM8005 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 9 for the suggested layout of a boost topology application and Figure 10 for the suggested layout of a buck-boost mode topology application. Ensure that the grounding and heat sinking are acceptable.

A few rules to keep in mind are:

1. Place the R_{FB}, R_T and V_C components as close as possible to their respective pins.
2. Place the C_{IN} capacitors as close as possible to the V_{IN} and GND connection of the LTM8005.
3. Place the C_{OUT} capacitors as close as possible to the V_{OUT} and GND connection of the LTM8005.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground currents flow directly adjacent to or underneath the LTM8005.

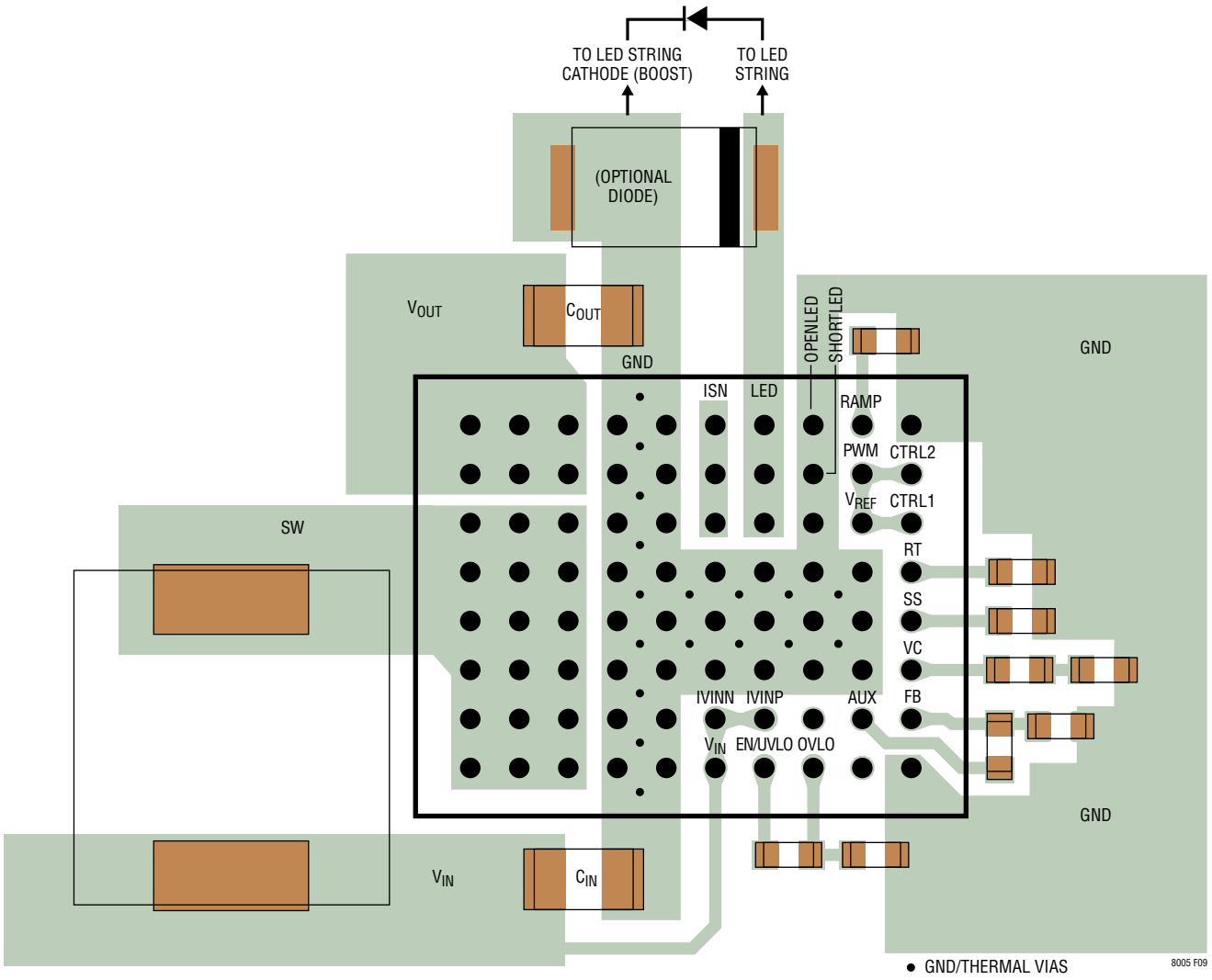

Figure 9. Layout Showing Suggested External Components, GND Plane and Thermal Vias for a Boost Application

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5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8005.

6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figures 9 and 10. The LTM8005 can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

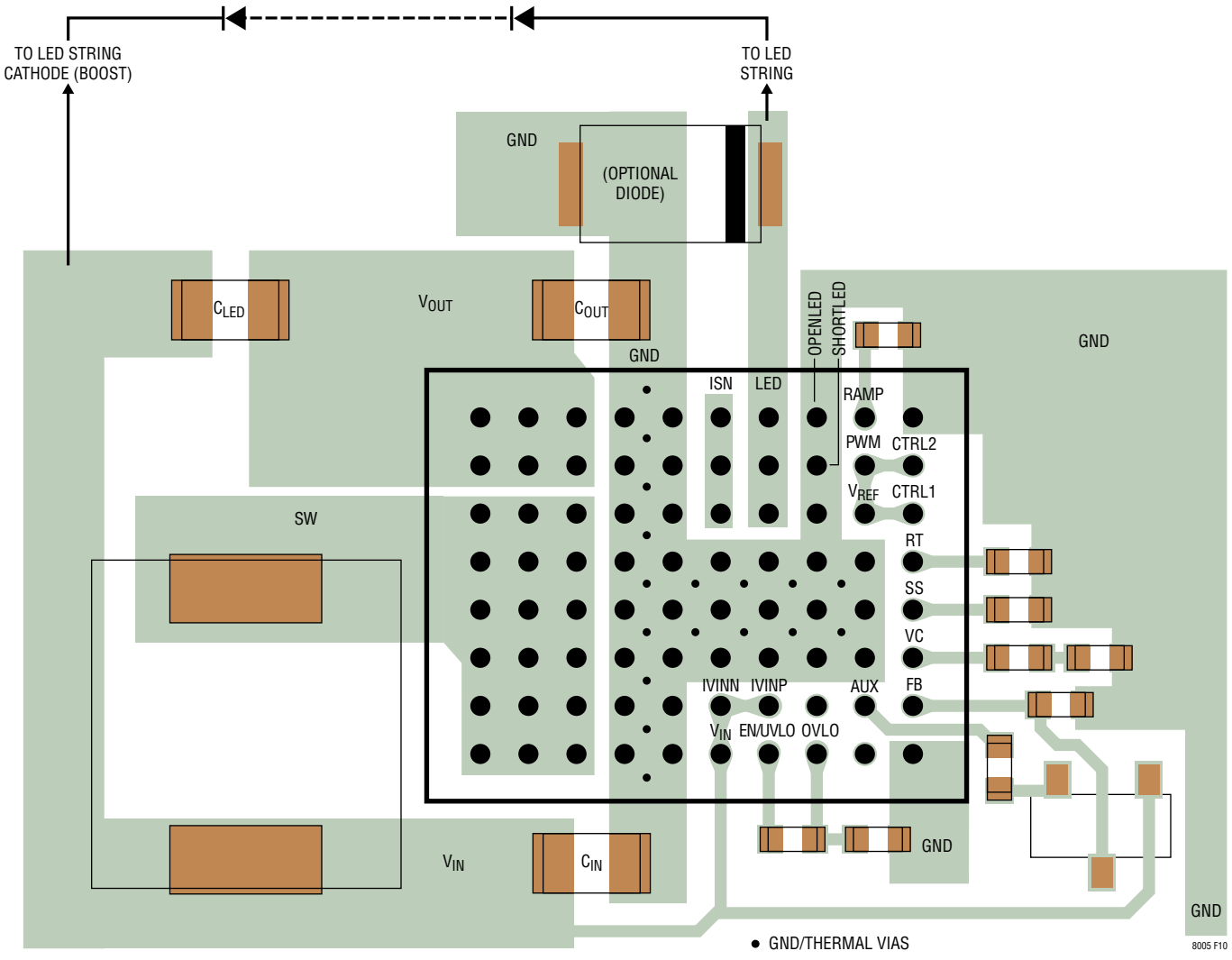

Figure 10. Layout Showing Suggested External Components, GND Plane and Thermal Vias for a Buck-Boost Mode Application

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Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of the LTM8005. However, these capacitors can cause problems if the LTM8005 is plugged into a live supply (see Analog Devices Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8005 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8005's rating and damaging the part. If the input supply is poorly controlled or the LTM8005 is hot-plugged into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is to add an electrolytic bulk cap to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit.

Thermal Considerations

The LTM8005 output current may need to be derated if it is required to operate in a high ambient temperature or deliver a large amount of continuous power. The amount of current derating is dependent upon the input voltage, output power and ambient temperature.

It is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

The thermal resistance numbers listed in Page 2 of the data sheet are based on modeling the µModule package mounted on a test board specified per JESD51-9 ("Test Boards for Area Array Surface Mount Package Thermal Measurements"). The thermal coefficients provided in this page are based on JESD 51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

For increased accuracy and fidelity to the actual application, many designers use FEA to predict thermal performance. To that end, Page 2 of the data sheet typically gives four thermal coefficients:

θ_{JA} – Thermal resistance from junction to ambient

$\theta_{JCBOTTOM}$ – Thermal resistance from junction to the bottom of the product case

θ_{JCTOP} – Thermal resistance from junction to top of the product case

θ_{JB} – Thermal resistance from junction to the printed circuit board.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased below:

> θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
>
> $\theta_{JCBOTTOM}$ is the thermal resistance between the junction and bottom of the package with all of the component power dissipation flowing through the bottom of the package. In the typical µModule converter, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

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θ_{JCTOP} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule converter are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCBOTTOM}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JB} is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule converter and into the board, and is really the sum of the $\theta_{JCBOTTOM}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule converter. Thus, none of them can be individually used to accurately predict the thermal performance of the product. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

A graphical representation of these thermal resistances is given in Figure 11.

The blue resistances are contained within the µModule converter, and the green are outside.

The die temperature of the LTM8005 must be lower than the maximum rating of 150°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8005. The bulk of the heat flow out of the LTM8005 is through the bottom of the µModule converter and the BGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

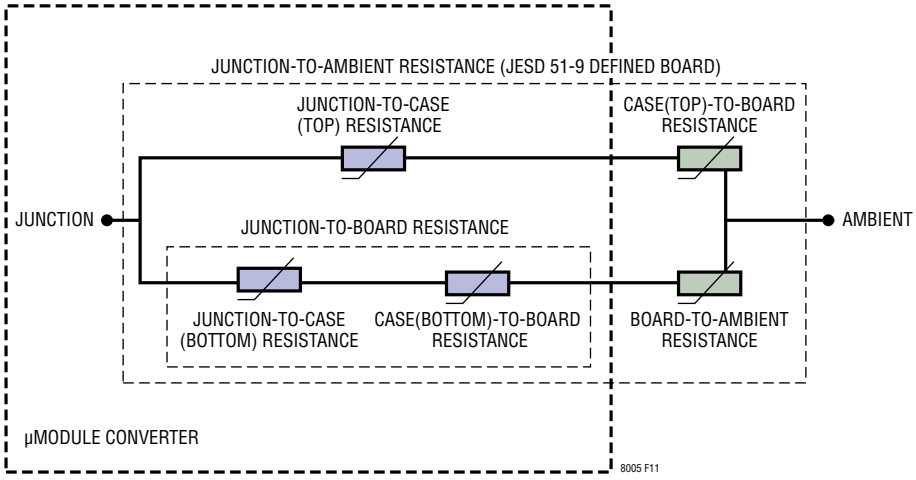
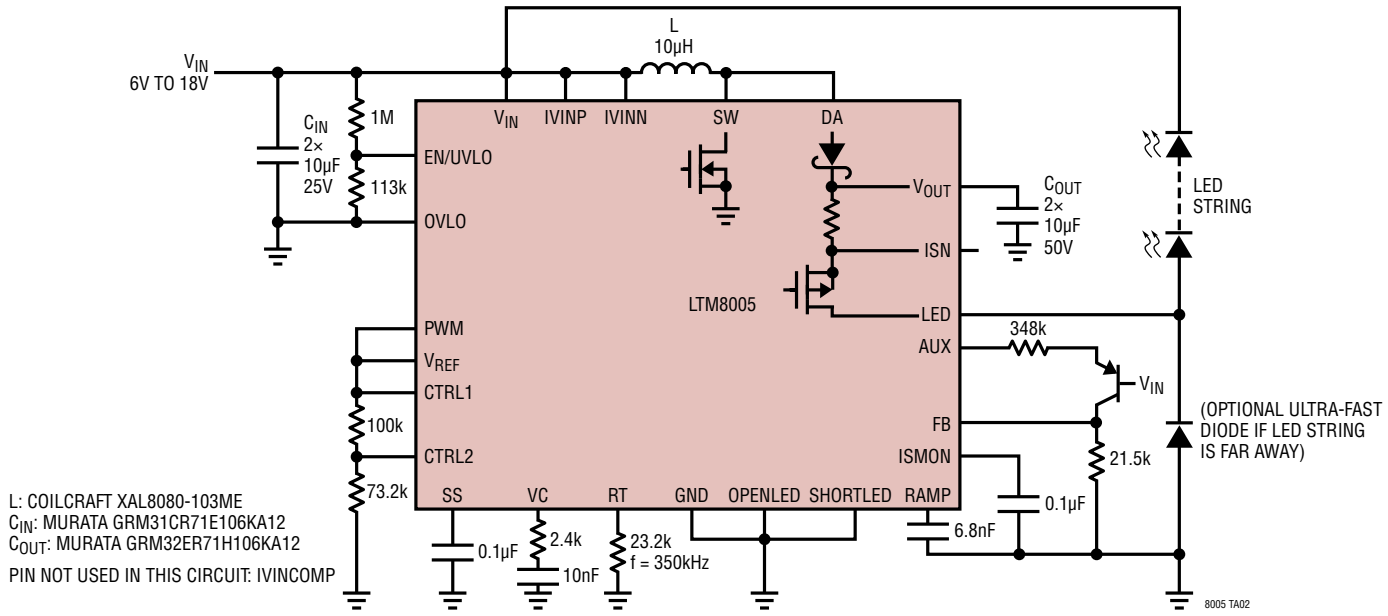


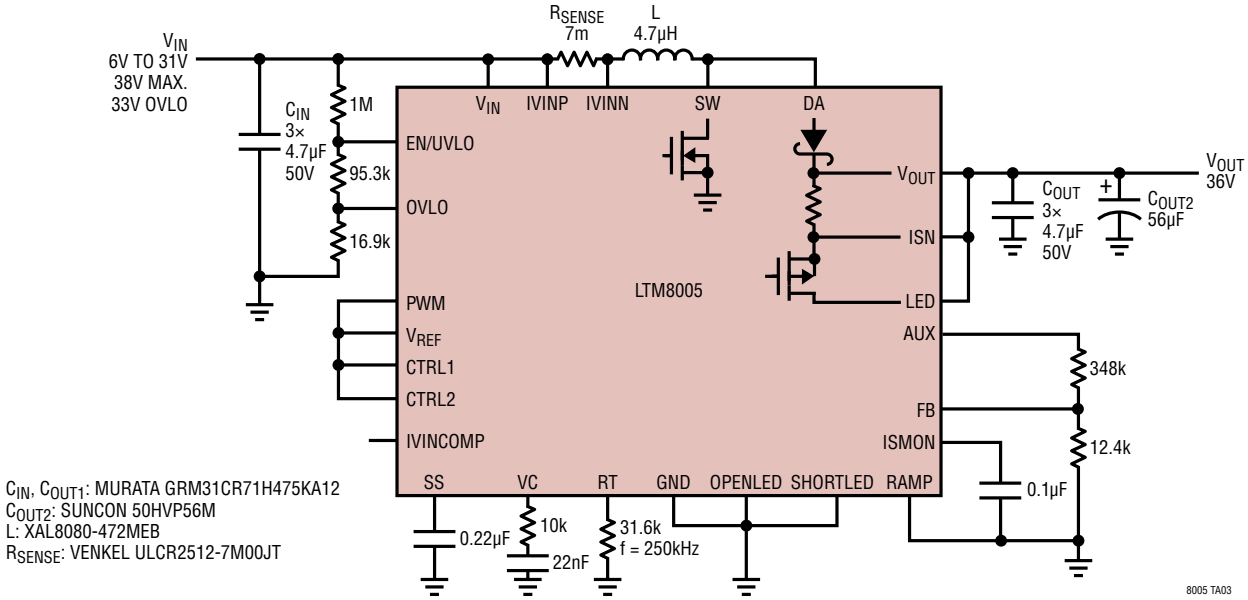
Figure 11.

TYPICAL APPLICATIONS

1.2A at up to 17V LED String from 6V to 18V_{IN} (Buck-Boost Mode) with Spread Spectrum

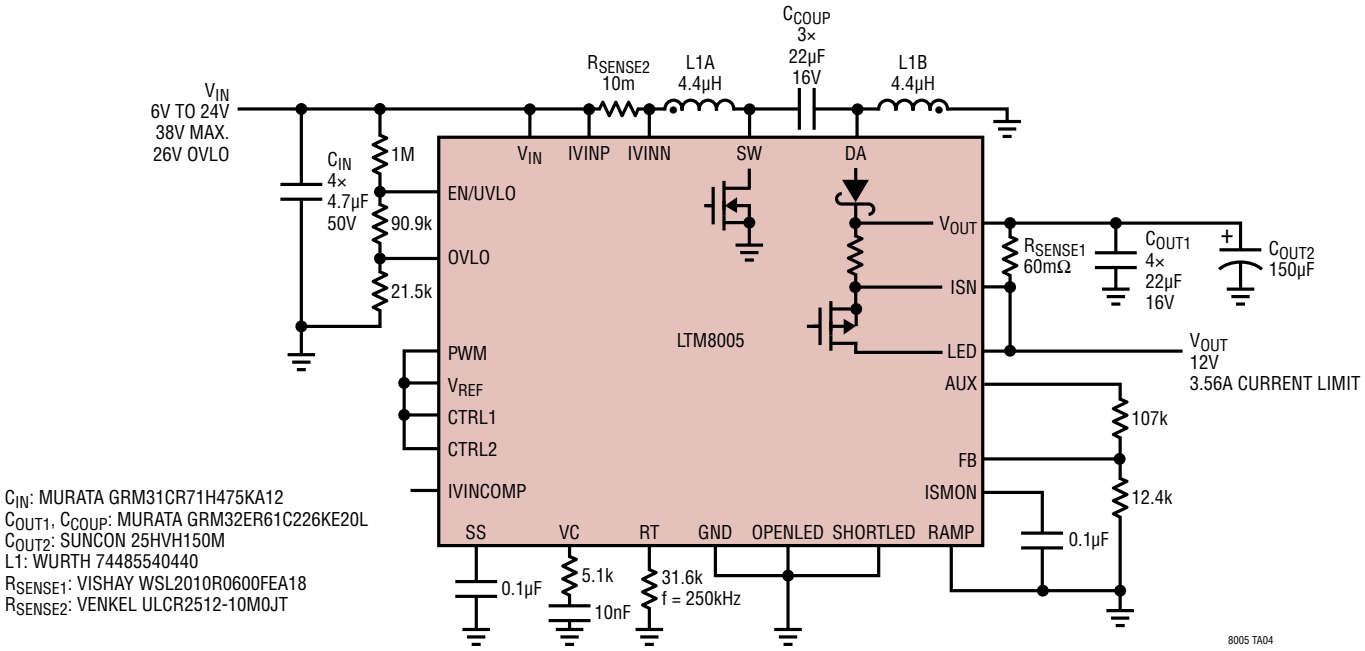


6V_{IN} to 31V_{IN} to 36V_{OUT} Boost Regulator



TYPICAL APPLICATIONS

$6V_{IN}$ to $24V_{IN}$ to $12V_{OUT}$ SEPIC with Current Limit



C_{IN}: MURATA GRM31CR71H475KA12
C_{OUT1}, C_{COUP}: MURATA GRM32ER61C226KE20L
C_{OUT2}: SUNCON 25HVH150M
L1: WURTH 74485540440
R_{SENSE1}: VISHAY WSL2010R0600FEA18
R_{SENSE2}: VENKEL ULCR2512-10M0JT

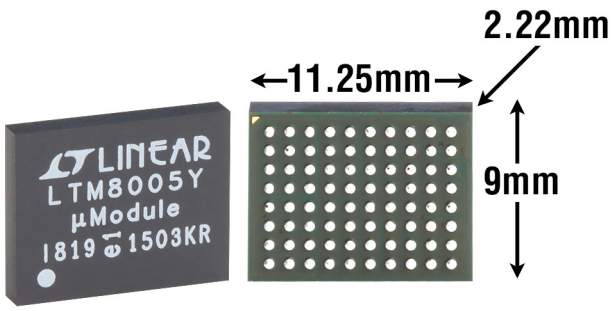
PACKAGE DESCRIPTION

Table 2. LTM8005 Pinout (Sorted by Pin Number)

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	SW	B1	SW	C1	SW	D1	GND	E1	GND
A2	SW	B2	SW	C2	SW	D2	GND	E2	GND
A3	SW	B3	SW	C3	SW	D3	GND	E3	GND
A4	SW	B4	SW	C4	SW	D4	GND	E4	GND
A5	DA	B5	DA	C5	DA	D5	GND	E5	GND
A6	DA	B6	DA	C6	DA	D6	GND	E6	GND
A7	V_{OUT}	B7	V_{OUT}	C7	V_{OUT}	D7	GND	E7	GND
A8	V_{OUT}	B8	V_{OUT}	C8	V_{OUT}	D8	GND	E8	GND

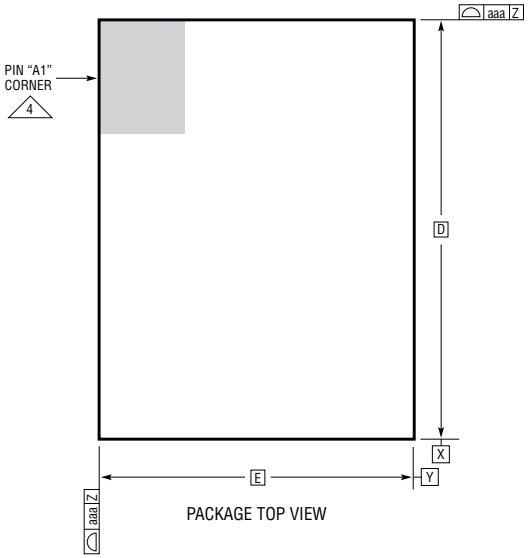
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
F1	V_{IN}	G1	EN/UVLO	H1	OVLO	J1	ISMON	K1	GND
F2	IVINN	G2	IVINP	H2	IVINCOMP	J2	AUX	K2	FB
F3	GND	G3	GND	H3	GND	J3	GND	K3	VC
F4	GND	G4	GND	H4	GND	J4	GND	K4	SS
F5	GND	G5	GND	H5	GND	J5	GND	K5	RT
F6	ISN	G6	LED	H6	GND	J6	V_{REF}	K6	CTRL1
F7	ISN	G7	LED	H7	SHORTLED	J7	PWM	K7	CTRL2
F8	ISN	G8	LED	H8	OPENLED	J8	RAMP	K8	GND

PACKAGE PHOTO

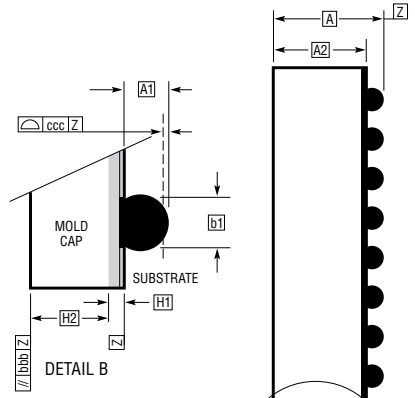


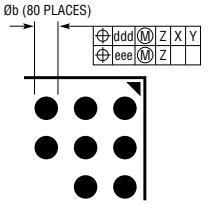
PACKAGE DESCRIPTION

BGA Package
80-Lead (11.25mm × 9mm × 2.22mm)
(Reference LTC DWG # 05-08-1979 Rev Ø)



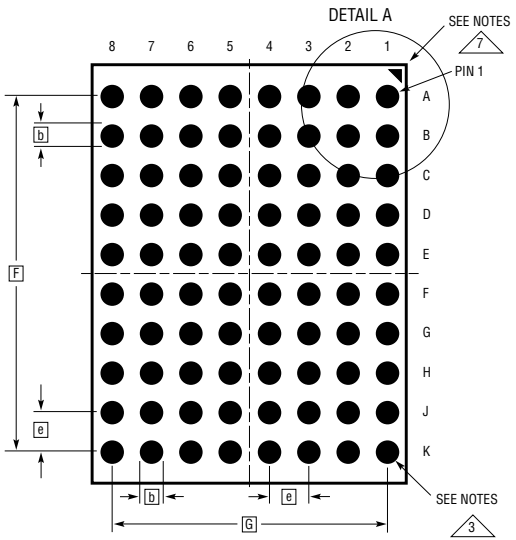
PACKAGE TOP VIEW



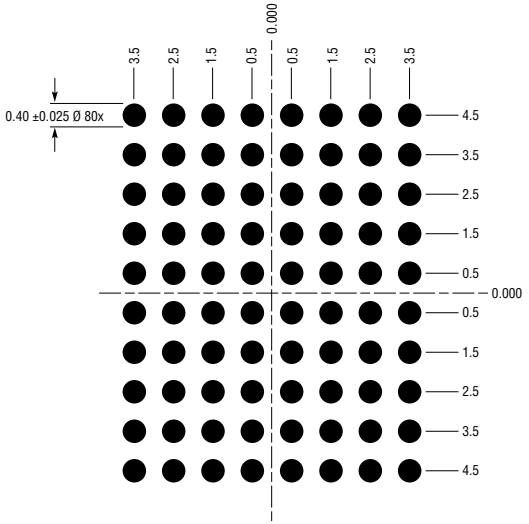


DETAIL A

DETAIL B
PACKAGE SIDE VIEW



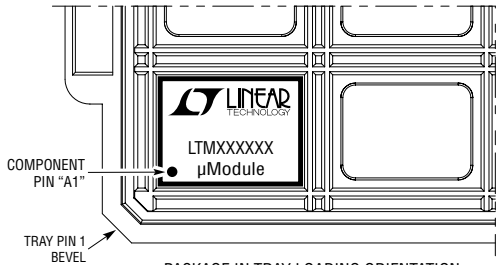
PACKAGE BOTTOM VIEW



SUGGESTED PCB LAYOUT
TOP VIEW

DIMENSIONS				
SYMBOL	**MIN**	**NOM**	**MAX**	**NOTES**
A	2.07	2.22	2.37	
A1	0.35	0.40	0.45	
A2	1.72	1.82	1.92	
b	0.45	0.50	0.55	
b1	0.35	0.40	0.45	
D		11.25		
E		9.00		
e		1.00		
F		9.00		
G		7.00		
H1	0.27	0.32	0.37	
H2	1.45	1.50	1.55	
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 80				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. SOLDER BALL COMPOSITION IS 96.5% Sn/3.0% Ag/0.5% Cu
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



PACKAGE IN TRAY LOADING ORIENTATION

BGA 80 0514 REV Ø

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/18	Deleted LTM8005MPY#PBF from order information table.	2