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16/32-Bit

Architecture

XC2797X

16/32-Bit Single-Chip Microcontroller
with 32-Bit Performance
XC2000 Family / High Line

Data Sheet

V1.3 2011-07

Microcontrollers

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XC2797X Data Sheet
Revision History: V1.3 2011-07

Previous Versions:
V1.2, 2010-09
V1.1, 2010-02 Preliminary

Page	Subjects (major changes since last revision)
11	Clarified available Flash and SRAM memory allocation.
79	USIC “QSPI” protocol shortcut removed due to ambiguity (interpreted as Queued SPI or Quad SPI).
107	Relaxed the conditions for short-term deviation of internal clock source frequency Δf_{INT}.
107	Added startup time from power-on t_{SPO}
110	Removed the 128MHz conditions for N_{WSFLE}
117	Added the minimum PLL free running frequency. Reduced the min/max bandwidth.
142	Thermal resistance values updated.

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Table of Contents

16/32-Bit Single-Chip Microcontroller with 32-Bit Performance

XC2797X (XC2000 Family)

1 Summary of Features

For a quick overview and easy reference, the features of the XC2797X are summarized here.

- High-performance CPU with five-stage pipeline and MPU
  - 10 ns instruction cycle @ 100 MHz CPU clock (single-cycle execution)
  - One-cycle 32-bit addition and subtraction with 40-bit result
  - One-cycle multiplication (16 × 16 bit)
  - Background division (32 / 16 bit) in 21 cycles
  - One-cycle multiply-and-accumulate (MAC) instructions
  - Enhanced Boolean bit manipulation facilities
  - Zero-cycle jump execution
  - Additional instructions to support HLL and operating systems
  - Register-based design with multiple variable register banks
  - Fast context switching support with two additional local register banks
  - 16 Mbytes total linear address space for code and data
  - 1,024 Bytes on-chip special function register area (C166 Family compatible)
  - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels providing 112 interrupt nodes
  - Selectable external inputs for interrupt generation and wake-up
  - Fastest sample-rate 10 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
  - 8 Kbytes on-chip stand-by RAM (SBRAM)
  - 2 Kbytes on-chip dual-port RAM (DPRAM)
  - 24 Kbytes on-chip data SRAM (DSRAM)
  - Up to 112 Kbytes on-chip program/data SRAM (PSRAM)
  - Up to 1600 Kbytes on-chip program memory (Flash memory)
  - Memory content protection through Error Correction Code (ECC)

- On-Chip Peripheral Modules
  - Two synchronizable A/D Converters with up to 30 channels, 10-bit resolution, conversion time below 1 µs, optional data preprocessing (data reduction, range check), broken wire detection
  - Two 16-channel general purpose capture/compare units (CCx)
  - Four capture/compare units for flexible PWM signal generation (CCU6x)
  - Multi-functional general purpose timer unit with 5 timers
  - 8 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
  - On-chip MultiCAN interface (Rev. 2.0B active) with 128 message objects (Full CAN/Basic CAN) on up to 2 CAN nodes and gateway functionality
  - On-chip system timer and on-chip real time clock
- Up to 12 Mbytes external address space for code and data
  - Programmable external bus characteristics for different address ranges
  - Multiplexed or demultiplexed external address/data buses
  - Selectable address bus width
  - 16-bit or 8-bit data bus width
  - Five programmable chip-select signals
- Single power supply from 3.0 V to 5.5 V
- Power reduction and wake-up modes
- Programmable watchdog timer and oscillator watchdog
- Up to 150 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via Device Access Port (DAP) or JTAG interface
- 176-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the temperature range:
  - SAF-…: -40°C to 85°C
  - SAH-…: -40°C to 110°C
  - SAK-…: -40°C to 125°C
- the package and the type of delivery.

For ordering codes for the XC2797X please contact your sales representative or local distributor.

This document describes several derivatives of the XC2797X group:

Basic Device Types are readily available and
Special Device Types are only available on request.

As this document refers to all of these derivatives, some descriptions may not apply to a specific product, in particular to the special device types.

For simplicity the term **XC2797X** is used for all derivatives throughout this document.

1.1 Basic Device Types

Basic device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 1 Synopsis of XC2797X Basic Device Types

Derivative[1]	Flash Memory[2]	PSRAM[3]	Capt./Comp. Modules	ADC[4] Chan.	Interfaces[4]
XC2797X-200FxL	1,600 Kbytes	112 Kbytes	CC1/2 CCU60/1/2/3	16 + 14	2 CAN Nodes, 6 Serial Chan.

1) x is a placeholder for available speed grade in MHz. Can be 100 only.
2) Specific information about the on-chip Flash memory in **Table 3** and **Table 4**.
3) All derivatives additionally provide 8 Kbytes SBRAM, 2 Kbytes DPRAM, and 24 Kbytes DSRAM.
4) Specific information about the available channels in **Table 5**.
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

1.2 Special Device Types

Special device types are only available for high-volume applications on request.

Table 2 Synopsis of XC2797X Special Device Types

Derivative[1]	Flash Memory[2]	PSRAM[3]	Capt./Comp. Modules	ADC[4] Chan.	Interfaces[4]
XC2797X-136FxL	1,088 Kbytes	80 Kbytes	CC1/2 CCU60/1/2/3	16 + 14	2 CAN Nodes 6 Serial Chan.

1) x is a placeholder for available speed grade in MHz. Can be 80 or 100.
2) Specific information about the on-chip Flash memory in **Table 3** and **Table 4**.
3) All derivatives additionally provide 8 Kbytes SBRAM, 2 Kbytes DPRAM, and 24 Kbytes DSRAM.
4) Specific information about the available channels in **Table 5**.
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

1.3 Definition of Feature Variants

The XC2797X types are offered with several Flash memory sizes. **Table 3** and **Table 4** describe the location of the available Flash memory.

Table 3 Continuous Flash Memory Ranges

Total Flash Size	1st Range[1)]	2nd Range	3rd Range
1,600 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $D8'FFFF_H$	n.a.
1,088 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $CF'FFFF_H$	$D8'0000_H$ … $D8'FFFF_H$

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

Table 4 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0[1)]	Flash 1	Flash 2	Flash 3	Flash 4	Flash 5	Flash 6
1,600	256	255	256	256	256	256	64
1,088	256	255	256	256	-	-	64

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XC2797X types are offered with different interface options. **Table 5** lists the available channels for each option.

Table 5 Interface Channel Association

Total Number	Available Channels / Message Objects
16 ADC0 channels	CH0 … CH15
14 ADC1 channels	CH0 … CH7, CH16 … CH21
2 CAN nodes	CAN0, CAN1 128 message objects
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1

The XC2797X types are offered with several PSRAM memory sizes. **Figure 1** shows the allocation rules. For example 80 Kbytes of PSRAM will be allocated at E0’0000h-E1’3FFFh.

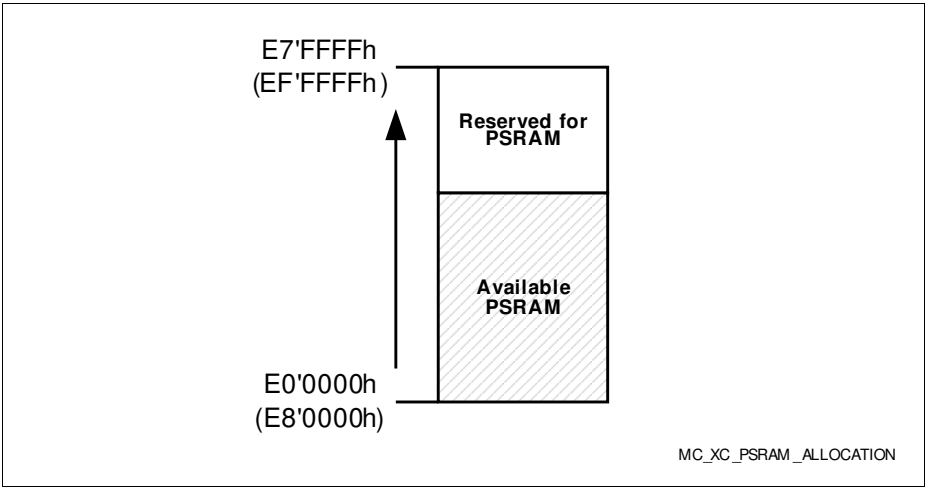

Figure 1 PSRAM Allocation

2 General Device Information

The XC2797X series (16/32-Bit Single-Chip Microcontroller with 32-Bit Performance) is a part of the Infineon XC2000 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 100 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

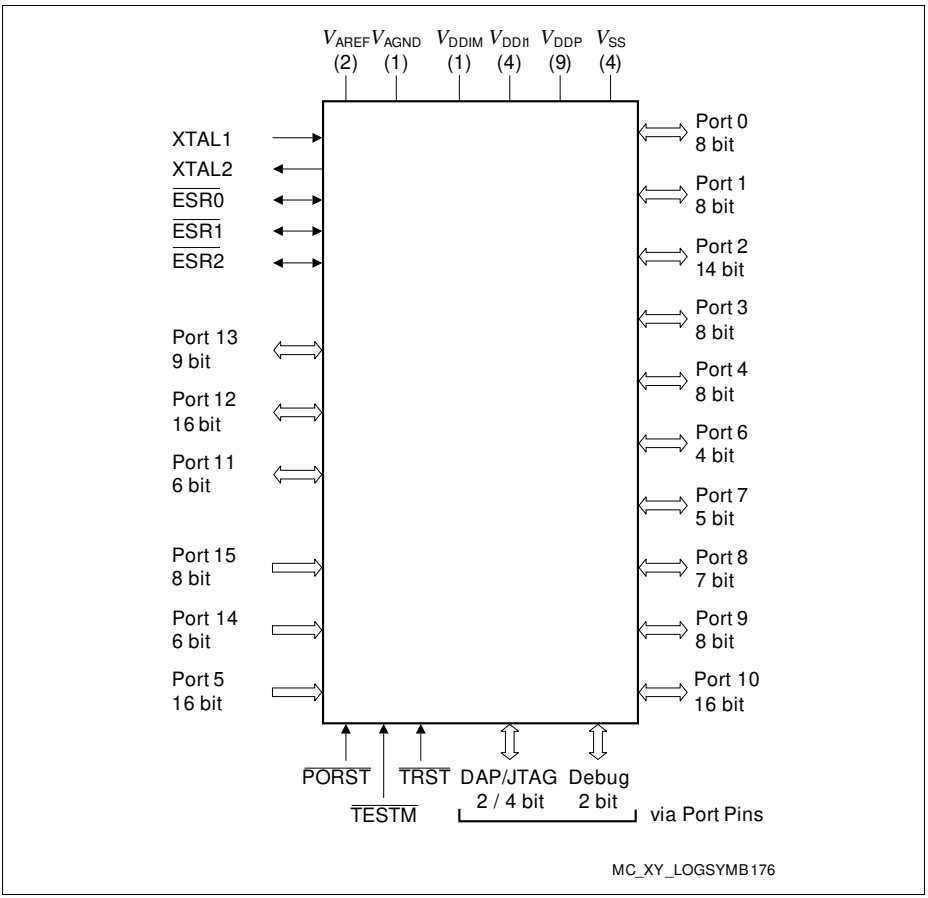

Figure 2 XC2797X Logic Symbol

2.1 Pin Configuration and Definition

The pins of the XC2797X are described in detail in **Table 6**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.

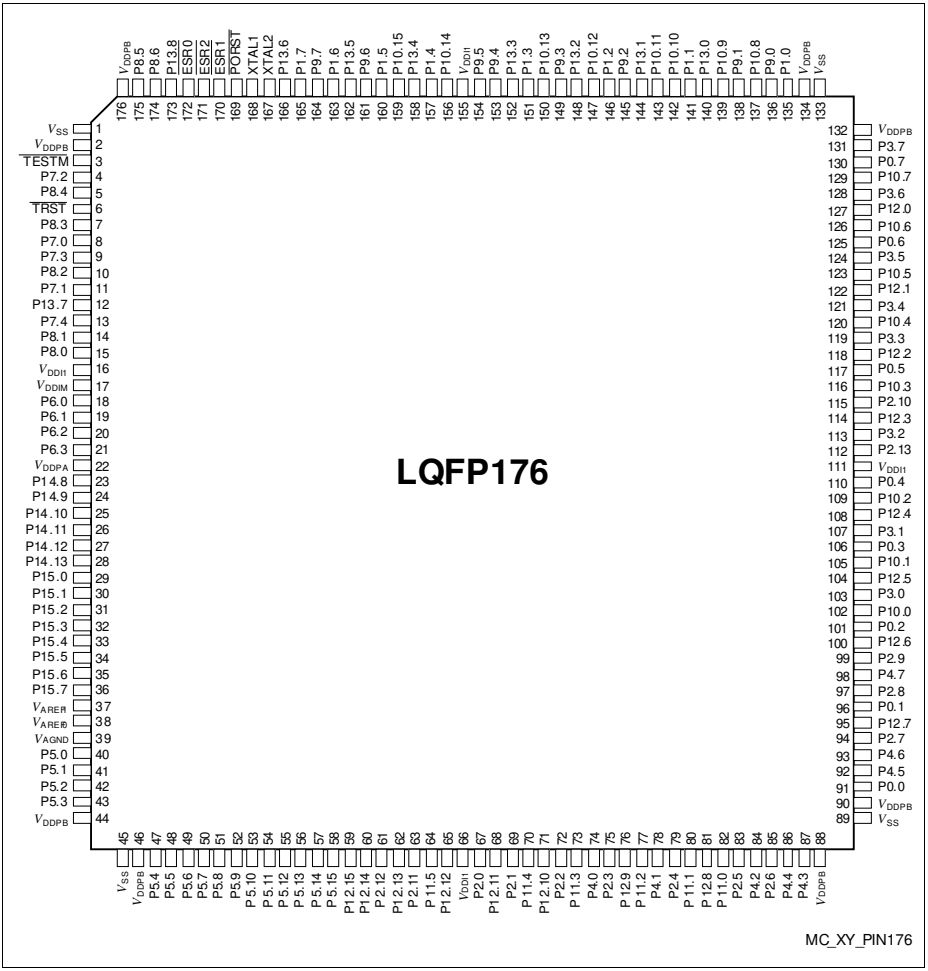

Figure 3 XC2797X Pin Configuration (top view)

Key to Pin Definitions

- **Ctrl.**: The output signal for a port pin is selected by bit field PC in the associated register Px_IOCRy. Output O0 is selected by setting the respective bit field PC to $1x00_B$, output O1 is selected by $1x01_B$, etc.
  Output signal OH is controlled by hardware.
- **Type**: Indicates the pad type and its power supply domain (A, B, M, 1).
  - St: Standard pad
  - Sp: Special pad e.g. XTALx
  - DP: Double pad - can be used as standard or high speed pad
  - In: Input only pad
  - PS: Power supply pad

Table 6 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
3	$\overline{\text{TESTM}}$	I	In/B	**Testmode Enable** Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pull-up device will hold this pin high when nothing is driving it.
4	P7.2	O0 / I	St/B	**Bit 2 of Port 7, General Purpose Input/Output**
	EMUX0	O1	St/B	**External Analog MUX Control Output 0 (ADC1)**
	CCU62_CCPOS0A	I	St/B	**CCU62 Position Input 0**
	TDI_C	IH	St/B	**JTAG Test Data Input** If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
5	P8.4	O0 / I	St/B	**Bit 4 of Port 8, General Purpose Input/Output**
	CCU60_COUT61	O1	St/B	**CCU60 Channel 1 Output**
	CCU62_CC61	O2	St/B	**CCU62 Channel 1 Output**
	CC1_CC2	O3	St/B	**CC1 Channel 2 Output**
	TMS_D	IH	St/B	**JTAG Test Mode Selection Input** If JTAG pos. D is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
	CCU62_CC61INB	I	St/B	**CCU62 Channel 1 Input**
6	$\overline{\text{TRST}}$	I	In/B	**Test-System Reset Input** For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XC2797X's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pull-down device will hold this pin low when nothing is driving it.
7	P8.3	O0 / I	St/B	**Bit 3 of Port 8, General Purpose Input/Output**
	CCU60_COUT60	O1	St/B	**CCU60 Channel 0 Output**
	CCU62_CC60	O2	St/B	**CCU62 Channel 0 Output**
	TDI_D	IH	St/B	**JTAG Test Data Input** If JTAG pos. D is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	CCU62_CC60INB	I	St/B	**CCU62 Channel 0 Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
8	P7.0	O0 / I	St/B	**Bit 0 of Port 7, General Purpose Input/Output**
	T3OUT	O1	St/B	**GPT12E Timer T3 Toggle Latch Output**
	T6OUT	O2	St/B	**GPT12E Timer T6 Toggle Latch Output**
	TDO_A	OH / IH	St/B	**JTAG Test Data Output / DAP1 Input/Output** If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	ESR2_1	I	St/B	**ESR2 Trigger Input 1**
9	P7.3	O0 / I	St/B	**Bit 3 of Port 7, General Purpose Input/Output**
	EMUX1	O1	St/B	**External Analog MUX Control Output 1 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_DOUT	O3	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU62_CCPOS1A	I	St/B	**CCU62 Position Input 1**
	TMS_C	IH	St/B	**JTAG Test Mode Selection Input** If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	U0C1_DX0F	I	St/B	**USIC0 Channel 1 Shift Data Input**
10	P8.2	O0 / I	St/B	**Bit 2 of Port 8, General Purpose Input/Output**
	CCU60_CC62	O1	St/B	**CCU60 Channel 2 Output**
	TxDC1	O2	St/B	**CAN Node 1 Transmit Data Output**
	U1C1_DOUT	O3	St/B	**USIC1 Channel 1 Shift Data output**
	CCU60_CC62INB	I	St/B	**CCU60 Channel 2 Input**
11	P7.1	O0 / I	St/B	**Bit 1 of Port 7, General Purpose Input/Output**
	EXTCLK	O1	St/B	**Programmable Clock Signal Output**
	CCU62_CTRAPA	I	St/B	**CCU62 Emergency Trap Input**
	$\overline{\text{BRKIN\_C}}$	I	St/B	**OCDS Break Signal Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
12	P13.7	O0 / I	St/B	**Bit 7 of Port 13, General Purpose Input/Output**
	T6OUT	O2	St/B	**GPT12E Timer T6 Toggle Latch Output**
	CCU60_T13HRF	I	St/B	**External Run Control Input for T13 of CCU60**
13	P7.4	O0 / I	St/B	**Bit 4 of Port 7, General Purpose Input/Output**
	EMUX2	O1	St/B	**External Analog MUX Control Output 2 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C1_SCLKOUT	O3	St/B	**USIC0 Channel 1 Shift Clock Output**
	CCU62_CCPOS2A	I	St/B	**CCU62 Position Input 2**
	TCK_C	IH	St/B	**DAP0/JTAG Clock Input** If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	U0C0_DX0D	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX1E	I	St/B	**USIC0 Channel 1 Shift Clock Input**
14	P8.1	O0 / I	St/B	**Bit 1 of Port 8, General Purpose Input/Output**
	CCU60_CC61	O1	St/B	**CCU60 Channel 1 Output**
	CC1_CC1	O2	St/B	**CC1 Channel 1 Output**
	CCU60_CC61INB	I	St/B	**CCU60 Channel 1 Input**
	RxDC1F	I	St/B	**CAN Node 1 Receive Data Input**
15	P8.0	O0 / I	St/B	**Bit 0 of Port 8, General Purpose Input/Output**
	CCU60_CC60	O1	St/B	**CCU60 Channel 0 Output**
	CC1_CC0	O2	St/B	**CC1 Channel 0 Output**
	CCU60_CC60INB	I	St/B	**CCU60 Channel 0 Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
18	P6.0	O0 / I	DA/A	**Bit 0 of Port 6, General Purpose Input/Output**
	EMUX0	O1	DA/A	**External Analog MUX Control Output 0 (ADC0)**
	$\overline{\text{BRKOUT}}$	O3	DA/A	**OCDS Break Signal Output**
	ADCx_REQGTyG	I	DA/A	**External Request Gate Input for ADC0/1**
	U1C1_DX0E	I	DA/A	**USIC1 Channel 1 Shift Data Input**
19	P6.1	O0 / I	DA/A	**Bit 1 of Port 6, General Purpose Input/Output**
	EMUX1	O1	DA/A	**External Analog MUX Control Output 1 (ADC0)**
	T3OUT	O2	DA/A	**GPT12E Timer T3 Toggle Latch Output**
	U1C1_DOUT	O3	DA/A	**USIC1 Channel 1 Shift Data Output**
	ADCx_REQTRyE	I	DA/A	**External Request Trigger Input for ADC0/1**
	ESR1_6	I	DA/A	**ESR1 Trigger Input 6**
20	P6.2	O0 / I	DA/A	**Bit 2 of Port 6, General Purpose Input/Output**
	EMUX2	O1	DA/A	**External Analog MUX Control Output 2 (ADC0)**
	T6OUT	O2	DA/A	**GPT12E Timer T6 Toggle Latch Output**
	U1C1_SCLKOUT	O3	DA/A	**USIC1 Channel 1 Shift Clock Output**
	U1C1_DX1C	I	DA/A	**USIC1 Channel 1 Shift Clock Input**
21	P6.3	O0 / I	DA/A	**Bit 3 of Port 6, General Purpose Input/Output**
	T3OUT	O2	DA/A	**GPT12E Timer T3 Toggle Latch Output**
	U1C1_SELO0	O3	DA/A	**USIC1 Channel 1 Select/Control 0 Output**
	U1C1_DX2D	I	DA/A	**USIC1 Channel 1 Shift Control Input**
	ADCx_REQTRyF	I	DA/A	**External Request Trigger Input for ADC0/1**
23	P14.8	I	In/A	**Bit 8 of Port 14, General Purpose Input**
	ADC1_CH16	I	In/A	**Analog Input Channel 16 for ADC1**
	T4INC	I	In/A	**GPT12E Timer T4 Count/Gate Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
24	P14.9	I	In/A	**Bit 9 of Port 14, General Purpose Input**
	ADC1_CH17	I	In/A	**Analog Input Channel 17 for ADC1**
	T4EUDC	I	In/A	**GPT12E Timer T4 External Up/Down Control Input**
25	P14.10	I	In/A	**Bit 10 of Port 14, General Purpose Input**
	ADC1_CH18	I	In/A	**Analog Input Channel 18 for ADC1**
26	P14.11	I	In/A	**Bit 11 of Port 14, General Purpose Input**
	ADC1_CH19	I	In/A	**Analog Input Channel 19 for ADC1**
27	P14.12	I	In/A	**Bit 12 of Port 14, General Purpose Input**
	ADC1_CH20	I	In/A	**Analog Input Channel 20 for ADC1**
28	P14.13	I	In/A	**Bit 13 of Port 14, General Purpose Input**
	ADC1_CH21	I	In/A	**Analog Input Channel 21 for ADC1**
29	P15.0	I	In/A	**Bit 0 of Port 15, General Purpose Input**
	ADC1_CH0	I	In/A	**Analog Input Channel 0 for ADC1**
30	P15.1	I	In/A	**Bit 1 of Port 15, General Purpose Input**
	ADC1_CH1	I	In/A	**Analog Input Channel 1 for ADC1**
31	P15.2	I	In/A	**Bit 2 of Port 15, General Purpose Input**
	ADC1_CH2	I	In/A	**Analog Input Channel 2 for ADC1**
	T5INA	I	In/A	**GPT12E Timer T5 Count/Gate Input**
32	P15.3	I	In/A	**Bit 3 of Port 15, General Purpose Input**
	ADC1_CH3	I	In/A	**Analog Input Channel 3 for ADC1**
	T5EUDA	I	In/A	**GPT12E Timer T5 External Up/Down Control Input**
33	P15.4	I	In/A	**Bit 4 of Port 15, General Purpose Input**
	ADC1_CH4	I	In/A	**Analog Input Channel 4 for ADC1**
	T6INA	I	In/A	**GPT12E Timer T6 Count/Gate Input**
34	P15.5	I	In/A	**Bit 5 of Port 15, General Purpose Input**
	ADC1_CH5	I	In/A	**Analog Input Channel 5 for ADC1**
	T6EUDA	I	In/A	**GPT12E Timer T6 External Up/Down Control Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
35	P15.6	I	In/A	**Bit 6 of Port 15, General Purpose Input**
	ADC1_CH6	I	In/A	**Analog Input Channel 6 for ADC1**
36	P15.7	I	In/A	**Bit 7 of Port 15, General Purpose Input**
	ADC1_CH7	I	In/A	**Analog Input Channel 7 for ADC1**
37	V_{AREF1}	-	PS/A	**Reference Voltage for A/D Converter ADC1**
38	V_{AREF0}	-	PS/A	**Reference Voltage for A/D Converter ADC0**
39	V_{AGND}	-	PS/A	**Reference Ground for A/D Converters ADC0/1**
40	P5.0	I	In/A	**Bit 0 of Port 5, General Purpose Input**
	ADC0_CH0	I	In/A	**Analog Input Channel 0 for ADC0**
41	P5.1	I	In/A	**Bit 1 of Port 5, General Purpose Input**
	ADC0_CH1	I	In/A	**Analog Input Channel 1 for ADC0**
42	P5.2	I	In/A	**Bit 2 of Port 5, General Purpose Input**
	ADC0_CH2	I	In/A	**Analog Input Channel 2 for ADC0**
	TDI_A	I	In/A	**JTAG Test Data Input**
43	P5.3	I	In/A	**Bit 3 of Port 5, General Purpose Input**
	ADC0_CH3	I	In/A	**Analog Input Channel 3 for ADC0**
	T3INA	I	In/A	**GPT12E Timer T3 Count/Gate Input**
47	P5.4	I	In/A	**Bit 4 of Port 5, General Purpose Input**
	ADC0_CH4	I	In/A	**Analog Input Channel 4 for ADC0**
	CCU63_T12HRB	I	In/A	**External Run Control Input for T12 of CCU63**
	T3EUDA	I	In/A	**GPT12E Timer T3 External Up/Down Control Input**
	TMS_A	I	In/A	**JTAG Test Mode Selection Input**
48	P5.5	I	In/A	**Bit 5 of Port 5, General Purpose Input**
	ADC0_CH5	I	In/A	**Analog Input Channel 5 for ADC0**
	CCU60_T12HRB	I	In/A	**External Run Control Input for T12 of CCU60**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
49	P5.6	I	In/A	**Bit 6 of Port 5, General Purpose Input**
	ADC0_CH6	I	In/A	**Analog Input Channel 6 for ADC0**
50	P5.7	I	In/A	**Bit 7 of Port 5, General Purpose Input**
	ADC0_CH7	I	In/A	**Analog Input Channel 7 for ADC0**
51	P5.8	I	In/A	**Bit 8 of Port 5, General Purpose Input**
	ADC0_CH8	I	In/A	**Analog Input Channel 8 for ADC0**
	ADC1_CH8	I	In/A	**Analog Input Channel 8 for ADC1**
	CCU6x_T12HRC	I	In/A	**External Run Control Input for T12 of CCU60/1/2/3**
	CCU6x_T13HRC	I	In/A	**External Run Control Input for T13 of CCU60/1/2/3**
	U2C0_DX0F	I	In/A	**USIC2 Channel 0 Shift Data Input**
52	P5.9	I	In/A	**Bit 9 of Port 5, General Purpose Input**
	ADC0_CH9	I	In/A	**Analog Input Channel 9 for ADC0**
	ADC1_CH9	I	In/A	**Analog Input Channel 9 for ADC1**
	CC2_T7IN	I	In/A	**CAPCOM2 Timer T7 Count Input**
53	P5.10	I	In/A	**Bit 10 of Port 5, General Purpose Input**
	ADC0_CH10	I	In/A	**Analog Input Channel 10 for ADC0**
	ADC1_CH10	I	In/A	**Analog Input Channel 10 for ADC1**
	$\overline{\text{BRKIN\_A}}$	I	In/A	**OCDS Break Signal Input**
	U2C1_DX0F	I	In/A	**USIC2 Channel 1 Shift Data Input**
	CCU61_T13HRA	I	In/A	**External Run Control Input for T13 of CCU61**
54	P5.11	I	In/A	**Bit 11 of Port 5, General Purpose Input**
	ADC0_CH11	I	In/A	**Analog Input Channel 11 for ADC0**
	ADC1_CH11	I	In/A	**Analog Input Channel 11 for ADC1**
55	P5.12	I	In/A	**Bit 12 of Port 5, General Purpose Input**
	ADC0_CH12	I	In/A	**Analog Input Channel 12 for ADC0**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
56	P5.13	I	In/A	**Bit 13 of Port 5, General Purpose Input**
	ADC0_CH13	I	In/A	**Analog Input Channel 13 for ADC0**
	CCU63_T13HRF	I	In/A	**External Run Control Input for T13 of CCU63**
57	P5.14	I	In/A	**Bit 14 of Port 5, General Purpose Input**
	ADC0_CH14	I	In/A	**Analog Input Channel 14 for ADC0**
	CC1_T0IN	I	St/B	**CAPCOM1 Timer T7 Count Input**
58	P5.15	I	In/A	**Bit 15 of Port 5, General Purpose Input**
	ADC0_CH15	I	In/A	**Analog Input Channel 15 for ADC0**
59	P12.15	O0 / I	St/B	**Bit 15 of Port 12, General Purpose Input/Output**
	CC2_CC21	O1	St/B	**CAPCOM2 Channel 21 Compare Output**
	CCU63_CC60	O2	St/B	**CCU63 Channel 0 Output**
	T2INB	I	St/B	**GPT12E Timer T2 Count/Gate Input**
	CCU63_CC60INC	I	St/B	**CCU63 Channel 0 Input**
60	P12.14	O0 / I	St/B	**Bit 14 of Port 12, General Purpose Input/Output**
	CC2_CC20	O1	St/B	**CAPCOM2 Channel 20 Compare Output**
	CCU63_CC61	O2	St/B	**CCU63 Channel 1 Output**
	CCU63_CC61INC	I	St/B	**CCU63 Channel 1 Input**
61	P2.12	O0 / I	St/B	**Bit 12 of Port 2, General Purpose Input/Output**
	U0C0_SELO4	O1	St/B	**USIC0 Channel 0 Select/Control 4 Output**
	U0C1_SELO3	O2	St/B	**USIC0 Channel 1 Select/Control 3 Output**
	READY	IH	St/B	**External Bus Interface READY Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
62	P12.13	O0 / I	St/B	**Bit 13 of Port 12, General Purpose Input/Output**
	CC2_CC19	O1	St/B	**CAPCOM2 Channel 19 Compare Output**
	CCU63_CC62	O2	St/B	**CCU63 Channel 2 Output**
	CCU63_CC62INC	I	St/B	**CCU63 Channel 2 Input**
63	P2.11	O0 / I	St/B	**Bit 11 of Port 2, General Purpose Input/Output**
	U0C0_SELO2	O1	St/B	**USIC0 Channel 0 Select/Control 2 Output**
	U0C1_SELO2	O2	St/B	**USIC0 Channel 1 Select/Control 2 Output**
	U3C1_DOUT	O3	St/B	**USIC3 Channel 1 Shift Data Output**
	$\overline{BHE}$/$\overline{WRH}$	OH	St/B	**External Bus Interf. High-Byte Control Output** Can operate either as Byte High Enable ($\overline{BHE}$) or as Write strobe for High Byte ($\overline{WRH}$).
64	P11.5	O0 / I	St/B	**Bit 5 of Port 11, General Purpose Input/Output**
	CCU61_CC60	O1	St/B	**CCU61 Channel 0 Output**
	CCU61_COUT63	O2	St/B	**CCU61 Channel 3 Output**
	U3C1_SELO1	O3	St/B	**USIC3 Channel 1 Select/Control 1 Output**
	CCU61_CC60INB	I	St/B	**CCU61 Channel 0 Input**
	U3C1_DX2B	I	St/B	**USIC3 Channel 1 Shift Control Input**
65	P12.12	O0 / I	St/B	**Bit 12 of Port 12, General Purpose Input/Output**
	CC2_CC18	O1	St/B	**CAPCOM2 Channel 18 Compare Output**
	CCU63_COUT60	O2	St/B	**CCU63 Channel 0 Output**
	U3C1_MCLKOUT	O3	St/B	**USIC3 Channel 1 Master Clock Output**
	T2EUDB	I	St/B	**GPT12E Timer T2 External Up/Down Control Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
67	P2.0	O0 / I	St/B	**Bit 0 of Port 2, General Purpose Input/Output**
	CCU63_CC60	O2	St/B	**CCU63 Channel 0 Output**
	AD13	OH / IH	St/B	**External Bus Interface Address/Data Line 13**
	RxDC0C	I	St/B	**CAN Node 0 Receive Data Input**
	CCU63_CC60INB	I	St/B	**CCU63 Channel 0 Input**
	T5INB	I	St/B	**GPT12E Timer T5 Count/Gate Input**
68	P12.11	O0 / I	St/B	**Bit 11 of Port 12, General Purpose Input/Output**
	CC2_CC17	O1	St/B	**CAPCOM2 Channel 17 Compare Output**
	CCU63_COUT61	O2	St/B	**CCU63 Channel 1 Output**
	U3C1_DX2C	I	St/B	**USIC3 Channel 1 Shift Control Input**
69	P2.1	O0 / I	St/B	**Bit 1 of Port 2, General Purpose Input/Output**
	TxDC0	O1	St/B	**CAN Node 0 Transmit Data Output**
	CCU63_CC61	O2	St/B	**CCU63 Channel 1 Output**
	AD14	OH / IH	St/B	**External Bus Interface Address/Data Line 14**
	CCU63_CC61INB	I	St/B	**CCU63 Channel 1 Input**
	T5EUDB	I	St/B	**GPT12E Timer T5 External Up/Down Control Input**
	ESR1_5	I	St/B	**ESR1 Trigger Input 5**
70	P11.4	O0 / I	St/B	**Bit 4 of Port 11, General Purpose Input/Output**
	CCU61_CC62	O1	St/B	**CCU61 Channel 2 Output**
	U3C1_DOUT	O2	St/B	**USIC3 Channel 1 Shift Data Output**
	CCU61_CC62INB	I	St/B	**CCU61 Channel 2 Input**
	U3C1_DX0B	I	St/B	**USIC3 Channel 1 Shift Data Input**