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### ADRV-DPD1/PCBZ Small Cell Radio Reference Design with Digital Predistortion

### **FEATURES**

Complete JESD204B to antenna port design with AD9375 DPD and SKY66297-11 PA

- $2\times2$  LTE 20 MHz, 250 mW output power per antenna, Band 7 FDD
- Contains transceiver, 2 PAs, 2 LNAs, duplex filters, and dc power solution

Power consumption of radio board: approximately 10 W Powered from single 12 V supply Evaluation kit connects to baseband subsystem

### **EVALUATION KIT CONTENTS**

ADRV-DPD1/PCBZ radio board ADRV-INTERPOS1/PCBZ interposer board with clock solution One 8 GB SD card RF adapters between series SMP (F) and SMA (F) 12 V, 60 W ac/dc external desktop (Class I) power supply

### **EQUIPMENT NEEDED**

EVAL-TPG-ZYNQ3 evaluation board for Xilinx Zynq-7000 FPGA Ethernet cable IEC C13 ac power cable (not included)

### SOFTWARE NEEDED

AD9375 Small Cell Radio Reference Design Evaluation Software GUI

### **GENERAL DESCRIPTION**

The ADRV-DPD1/PCBZ is a 24 dBm per path, 2 × 2 multiple input, multiple output (MIMO) radio board, which uses the AD9375, a highly integrated radio frequency (RF) transceiver with integrated digital predistortion (DPD). The radio board is designed to be used with the dual connector interposer board to interface with the EVAL-TPG-ZYNQ3 or other Xilinx<sup>®</sup> or Avnet evaluation boards for the Xilinx Zynq<sup>™</sup>-7000 field programmable gate array (FPGA) platform, which has a dual core ARM Cortex<sup>®</sup>-A9 processor running a Linux<sup>®</sup> variant.

The AD9375 small cell evaluation software (SCES), AD9375 Small Cell Radio Reference Design Evaluation Software GUI, can configure and control the ADRV-DPD1/PCBZ board.

Note that the Mykonos transceiver evaluation software (MTES) and DPD graphical user interface (GUI) software are not compatible with the ADRV-DPD1/PCBZ.

Full specifications on the AD9375 are available in the AD9375 data sheet available from Analog Devices, Inc., and must be consulted in conjunction with this user guide when using the evaluation board.

## TABLE OF CONTENTS

Features
Evaluation Kit Contents
Equipment Needed 1
Software Needed 1
General Description
Revision History
ADRV-DPD1/PCBZ Evaluation Kit Photograph
Getting Started 5
Software Installation
SCES Setup Requirements
SCES Setup 5
Evaluation Kit Setup
Hardware Operation9
SCES Quickstart
Basic Receiver Setup10
Basic Transmitter Setup10
Basic DPD Setup11
Evaluation Kit Hardware12
Power Supply Connection
ADRV-DPD1/PCBZ Top and Bottom View Photographs 13
Interposer Board Reference
System Reference Clocks
LED Indicators 15
ADP5054 Enable Jumper
ADP5054 Enable Jumper.16EEPROM Write Protect Enable Headers16Debug Headers.17RF A Header Pins17RF B Header Pins17JTAG Header Pins18SPI Chip Select Lines18Pin Configurations and Function Descriptions20Using the Software for Testing30Graphical User Interface Operation30Starting the AD9375 SCES30Demo Mode30Normal Operation32Software Update32GUI Reference33
ADP5054 Enable Jumper.16ADP5054 Enable Jumper.16EEPROM Write Protect Enable Headers16Debug Headers.17RF A Header Pins17RF B Header Pins17JTAG Header Pins18SPI Chip Select Lines18Pin Configurations and Function Descriptions20Using the Software for Testing30Graphical User Interface Operation.30Starting the AD9375 SCES30Demo Mode32Software Update32GUI Reference.33Configuring the AD937533

ADRV-DPD1	/PCBZ	User	Guide

Calibration Tab	35
JESD204b Setup Tab	36
AGC Tab	37
GPIO Tabs	38
Rx Summary, Tx Summary, and ObsRx/Sniffer Summary Tabs	40
Clock Setup	41
Programming the Evaluation System	42
Other SCES Features	42
Device Dropdown Menu	42
File Dropdown Menu	42
Tools Dropdown Menu	45
Help Dropdown Menu	46
System Status Bar	47
Receiver Setup	48
Receive Data Options	48
Observation Receiver Signal Chain	49
Transmitter Setup	51
Transmit Data Options	52
RF Path and DPD Controls	53
Transmitter RF Path Controls	53
Receiver RF Path Controls	53
DPD Controls	54
Scripting	55
IronPython Script Example	56
Troubleshooting	58
Startup	58
No LED Activity (Zynq)	58
LEDs Active but SCES Reports that Hardware is Not Connected	58
LED 1 and LED 2 (STATUS 1 and STATUS 0) on Interpose	r
Board Do Not Illuminate After Programming	58
Error Handling	58
Typical Performance	59
Electrical Specifications	60
Bill of Materials	61
Interposer Board Schematics	68
Radio Board Schematics	88
Interposer Board PCB Layers 1	02
Radio Board PCB Layers 1	10
Interposer Board Connectors and LEDs 1	14

### **REVISION HISTORY**

7/2018—Rev. 0 to Rev. A
Updated FormatUniversal
Changes to Features Section and General Description Section1
Changes to Figure 1 Caption4
Changed Evaluation Board Software Section to Getting Started
Section5
Added Software Installation Section5
Changes to SCES Setup Requirements Section and SCES Setup
Section
Changes to Figure 6 Caption7
Changed Evaluation Board Hardware Section and Hardware
Setup Section to Evaluation Kit Setup Section
Changes to Evaluation Kit Setup7
Changes to Hardware Operation
Changes to SCES Quickstart Section and Basic Transmitter Setup
Section
Changes to Basic DPD Setup Section11
Added Evaluation Kit Hardware Section, Power Supply Connection
Section, and Figure 11; Renumbered Sequentially
Added Figure 12, ADRV-DPD1/PCBZ Top and Bottom View
Photographs Section, Figure 13 and Figure 1413
Added Figure 15 to Figure 18, Table 1, and Table 2; Renumbered
Sequentially14
Added Interposer Board Reference Section, Figure 19, System
Reference Clocks Section, Figure 20, LED Indicators Section, and
Figure 21
Added Table 3, ADP5054 Enable Jumper Section, Figure 22,
EEPROM Write Protect Enable Headers Section, and
Figure 23
Added Figure 24, Debug Headers Section, RF A Header Pins
Section, Figures 25, RF B Header Pins Section, and Figure 2617
Added JTAG Header Pins Section, Figure 27, and SPI Chip Select
Lines Section
Added Table 4
Added Pin Configurations and Function Descriptions Section,
Figure 28, and Table 520
Added Figure 29 and Table 623
Added Figure 30, Table 7, and Table 827
Added Figure 31, Table 9, and Table 1028
Added Figure 32 and Table 11

Changed AD9375 Small Cell Reference Design Evaluation
Software GUI Operation Section to Using the Software for
Testing Section
Added Graphical User Interface Operation Section
Changes to Figure 33 Caption
Changes to GPIO Tabs Section and Figure 44 Caption
Changed Rx, Tx, and ObsRx/Sniffer Summary Tab Section to Rx
Summary, Tx Summary, and ObsRx/Sniffer Summary Tabs
Section
Changes to Clock Setup Section41
Changed Rx Signal Chain Section to Receive Data Options
Section
Changed Observation Rx Signal Chain Section to Observation
Receiver Signal Chain Section
Changes to Observation Receiver Signal Chain Section
Changed Transmitter Data Options Section to Transmit Data
Options Section
Changes to Transmit Data Options Section
Changes to DPD Controls Section and Figure 62 Caption54
Changes to IronPython Script Example Section56
Changed LED 1 and LED 2 on Interposer Board Do Not Light up
After Programming Section to LED 1 and LED 2 (STATUS 1 and
STATUS 0) on Interposer Board Do Not Illuminate After
Programming Section
Added Typical Performance Section, Figure 66 to Figure 69, and
Table 12 to Table 1559
Added Table 16 to Table 19, Electrical Specifications Section, and
Table 20 to Table 21 60
Added Bill of Materials Section and Table 2261
Added Table 23 to Table 2564
Added Table 26 and Table 2767
Added Interposer Board Schematics Section and Figure 70 to
Figure 97
Added Radio Board Schematics Section and Figure 88 to
Figure 116
Added Interposer Board PCB Layers Section and Figure 117 to
Figure 124 102
Added Radio Board PCB Layers Section Figure 125 to
Figure 133 110

1/2018—Revision 0: Initial Version

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## ADRV-DPD1/PCBZ EVALUATION KIT PHOTOGRAPH



Figure 1. ADRV-DPD1/PCBZ Evaluation Kit with Radio Board Heatsink Removed

### **GETTING STARTED** SOFTWARE INSTALLATION

The AD9375 SCES, when connected to the evaluation kit, reads the hardware identification data and verifies that the AD9375 Small Cell Radio Reference Design Evaluation Software GUI is connected to the appropriate hardware. After the evaluation hardware is connected, the desired operating parameters can be set up with SCES, and the software can program the reference platform.

After the device is configured, the evaluation software can transmit waveforms, observe received waveforms, and initiate correction algorithms. In addition, sequences of application programming interface (API) commands in the form of IronPython scripts can be generated and executed using SCES.

### SCES SETUP REQUIREMENTS

The SCES requires the following:

- An evaluation board for the Xilinx Zynq-7000 system on a chip (SoC) FPGA, such as the EVAL-TPG-ZYNQ3 (not included in the AD9375 evaluation kit). Both the Xilinx EK-Z7-ZC706 Rev 1.2 and Avnet AES-Z7-JESD3-G Rev 1.2 are compatible with the AD9375 evaluation kit.
- The ADRV-DPD1/PCBZ Small Cell Radio Reference design kit.
- Operating system of Windows 7 SP1 or later.
- Free Ethernet port or USB to Ethernet adapter.
- AD9375 SCES installer, available on the ADRV-DPD1 product page.
- Administrative privileges on the controlling PC.

### SCES SETUP

To install the AD9375 Small Cell Radio Reference Design Evaluation Software GUI, complete the following steps:

- After the software zip folder downloads, copy the software to the target system and unzip the files. The extracted files include an executable file named Small Cell Evaluation Software Vx.x.x.exe.
- After running the executable file, a standard installation wizard opens. The wizard, by default, installs optional components, including the Microsoft .NET Framework 4.5 (which is mandatory for the software to operate) and IronPython 2.7.4 (which is optional but recommended), as shown in Figure 3.
- Open the Start > Run window and type ncpa.cpl into the text box, then click OK (see Figure 2).

📼 Run	Image: State Sta	
	Type the name of a program, folder, document, or Internet resource, and Windows will open it for you.	
<u>O</u> pen:	ncpa.cpl 👻	
	OK Cancel <u>B</u> rowse	16493-002

Figure 2. Run Window for Network Connections

🕞 Small Cell Evaluation Software Setup				
Choose Components Choose which features of Small Cell Evaluation Software you want to install.				
Check the components you wai install. Click Next to continue.	nt to install and uncheck the comp	onents you don't want to		
Select components to install:	✓ Microsoft .NET Frameworl ✓ IronPython 2.7.4 ✓ Small Cell Evaluation Soft	Description Position your mouse over a component to see its description,		
Space required: 177.8MB	4 III >			
Nullsoft Install System v2.46 —	< Back	Next > Cancel		

Figure 3. Software Installation Components

## ADRV-DPD1/PCBZ User Guide

- 4. Enable the selected device, right click on the device, and click **Properties**.
- 5. A window appears, as shown in Figure 5. Double click **Internet Protocol Version 4 (TCP/IPv4)**.
- 6. Select **Use the following IP address:** and enter the following values:
  - IP address: **192.168.1.2**.
  - Subnet mask: 255.255.255.0.
- Click OK at the bottom of the Internet Protocol Version 4 (TCP/IPv4) Properties window, then click OK at the bottom of the Local Area Connection x Properties window (where x is the number of local area network (LAN) devices installed on the computer). Close the Network Connections window.
- Create an outbound transmission control protocol (TCP). Create an always allow rule for the firewall for Port 22 and Port 55555 in Windows Firewall or other antivirus programs (such as Avast, Norton, AVG, or Sophos), as shown in Figure 6. Steps for creating these rules in Windows Firewall follow.
- To create an always allow rule in Windows Firewall, open the Start > Run window and type wf.msc into the box. Click OK (see Figure 4). Approve the User Account Control dialog box by clicking Yes.

	Type the name of a program, folder, document, or Internet resource, and Windows will open it for you.
<u>O</u> pen:	wf.msc 👻
	OK Cancel <u>B</u> rowse

Figure 4. **Run** Window for Windows Firewall

- In the Windows Firewall with Advanced Security window, click Outbound Rules in the left pane, and click New Rule... in the right pane.
- 11. Select the following options in the **New Outbound Rule Wizard** (see Figure 7).
  - Under the **Rule Type** section, select **Port**, then click **Next** >.
  - Under the **Protocol and Ports** section, click **TCP**, click **Specific remote ports**, and enter **22**, 555555. Click **Next** >.
  - Under the Action section, click Allow the connection then click Next >.
  - Under the **Profile** section, select the **Domain**, **Private**, and **Public** check boxes, and click **Next** >.
  - Under the **Name** section, enter **SCES** in the **Name** field, then click **Finish**.

Local Area Connection 3 Properties	Internet Protocol Version 4 (TCP/IPv4) Properties
Networking Sharing	General
Connect using: Realtek USB GbE Family Controller Configure This connection uses the following items: Client for Microsoft Networks Client for Microsoft Networks Client for Microsoft Networks File and Printer Sharing for Microsoft Networks File and Printer Sharing for Microsoft Networks Lintemet Protocol Version 6 (TCP/IPv6) Lintemet Protocol Version 4 (TCP/IPv4) Link-Layer Topology Discovery Mapper I/O Driver Link-Layer Topology Discovery Responder	You can get IP settings assigned automatically if your network supports this capability. Otherwise, you need to ask your network administrator for the appropriate IP settings. Obtain an IP address automatically Use the following IP address: IP address: Subnet mask: Default gateway: Obtain DNS conver address automatically
Install Uninstall Properties Description Transmission Control Protocol/Internet Protocol. The default wide area network protocol that provides communication across diverse interconnected networks. OK Cancel	OK Cancel

Figure 5. Internet Protocol (IP) Settings for Ethernet Device Rev. A | Page 6 of 115

Hender Them Them						
• 2 🖬 🖌 🖬 🖬						
Windows Firewall with Advance	Outbound Rules					Actions
Windrow Freenall with Advance Document Reads Outbound Rules Connection Security Rules Monitoring	Dutbound Rules None BranchCache Content Rational (HTTP-O BranchCache Hosted Cache Client (HTT- BranchCache Hosted Cache Stever(HTTP- BranchCache Hosted Cache Stever(HTTP- BranchCache Hosted Cache Stever(HTTP- BranchCache Hosted Cache Stever(HTTP- BranchCache Hosted Projector (ICP-Oul) Connect to a Network Projector (WSD Ev- Connect Networking - Municat Listerner Rep- Conne Networking - Municat Listerner Rep- Connect Networking - Municat Listerner Rep- Cone Networking - Municat Listerner Rep- Cone Net	Group BranchCache - ContentBetr BranchCache - Hosted Jach BranchCache - Hosted Jach BranchCache - Perel Bacve Connect to a Network Proje Connect to a Network Proje Con Networking Core Networking Cre Networking	Profile All All All Domain Private Private Private Private All Domain All Domain All All All All All All All All All Al	Enabled No No No No No No No No No No No No No	4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	Actions Outbound Rules New Rule V Filter by Porfile Filter by State Filter by State Rafresh Filter by Group View Rafresh Filter by Group View Rafresh Filter by Group Composition Findels Rule Cot Properties Help Help
	Core Networking - Parameter Problem (L. Core Networking - Router Advertisement Core Networking - Router Solicitation (IC Core Networking - Teredo (UDP-Out)	Cire Networking Cire Networking Cire Networking	All All All	Yes Yes Yes		

Figure 6. Windows Firewall with Advanced Security Window



Figure 7. New Outbound Rule Wizard Window

## **ADRV-DPD1/PCBZ** User Guide

### **EVALUATION KIT SETUP**

The hardware setup is shown in Figure 8. The Xilinx ZC706 Zyng evaluation board, shown in Figure 8 and Figure 9, is an older model of the EVAL-TPG-ZYNQ3, but the two boards are otherwise identical in terms of connections and compatibility.

To set up the hardware, complete the following steps:

- Connect the PC and the EVAL-TPG-ZYNQ3 evaluation 1. board with an Ethernet cable.
- 2. Ensure that all jumpers on the EVAL-TPG-ZYNQ3 are configured as shown in Figure 9, and Switch 1, Switch 2, and Switch 5 are set to the A position and that SW1 is set as shown in Figure 9.
- 3. Insert the secure digital (SD) card into the EVAL-TPG-ZYNQ3 and connect the interposer board to the connectors on the EVAL-TPG-ZYNQ3, and the radio board to the interposer board using the high pin count (HPC) FPGA mezzanine card (FMC) connectors, as shown in Figure 8. Ensure that the connectors are properly aligned.

- Ensure that the interposer board Header J16 is set to short the 4. middle two pins, Pin 3 to Pin 4, which is the automatic position (see Figure 133 for the location of these pins).
- Connect a reference clock signal to the interposer board at 5. J8 (REF\_A, default 10 MHz) or J13 (REF\_B, default 30.72 MHz). After SCES programs the system, two green light emitting diodes (LEDs) on the interposer board, Status 0 and Status 1, turn on. Lit LEDs indicate that the correct reference clock is provided and the phase locked loops (PLLs) in the AD9528 are locked. The Status 0 LED (PLL1 lock) remains unlit if no reference signal is present. The Status 1 LED (PLL2 lock) is always lit. A suitable input level for the reference signals at J8 or J13 is 380 mVp-p to 1200 mVp-p into 100  $\Omega$  (-7 dBm to +3 dBm from a 50  $\Omega$ sine wave generator). A square wave is preferred but a sine wave is acceptable. See the System Reference Clocks section for more details
- Connect the 12 V, 5 A power supply to the EVAL-TPG-6. ZYNQ3 at the J22 power input.
- Connect the 12 V, 5 A radio power supply to the interposer 7. board at J14.



Figure 8. Hardware Connection Diagram



Figure 9. Xilinx ZC706 Zynq Evaluation Board with Jumper Settings and Switch Position Configured to Work with the ADRV-DPD1/PCBZ (Identical to the EVAL-TPG-ZYNQ3)

### Hardware Operation

To operate the evaluation hardware, complete the following steps:

- Turn on the evaluation system by switching on both 12 V, 5 A power supplies connected to the EVAL-TPG-ZYNQ3 and the interposer board, then switch the EVAL-TPG-ZYNQ3 power switch, SW1, to the on position.
- 2. The EVAL-TPG-ZYNQ3 evaluation system uses a Linux operating system. It takes approximately 30 sec before the system is ready for operation and can accept commands from PC software. Boot status can be observed on the EVAL-TPG-ZYNQ3 general-purpose input/output (GPIO) LEDs (L, C, R, and O).

The following is the startup sequence that can be observed when booting the evaluation kit:

- a. After turning on SW1, all four LEDs are on for approximately 15 sec. During this time, the Linux boot image is copied from the SD card into the FPGA memory.
- The LEDs begin flashing (moving the single on light), indicating the Linux operating system is starting up. This startup takes another 15 sec.
- c. When the LEDs stop flashing, the system is ready for normal operation and awaits connection with the PC over the Ethernet local area network (LAN), which can be established using the SCES.

## ADRV-DPD1/PCBZ User Guide

- d. LED status during normal operation is represented on the EVAL-TPG-ZYNQ3 by the following (see Figure 9):
  - GPIO LED L is the RF receiver (Rx) JESD SYNC.
  - GPIO LED C is the RF sniffer (Sn)/observation (ObsRx) receiver JESD SYNC.
  - GPIO LED R is the RF transmitter (Tx) JESD SYNC.
  - GPIO LED O is the FPGA PLLs lock.
- e. When shutdown is executed using the SCES, the Linux operating system starts the power-down procedure. The power-down procedure takes a few seconds to finish. All four LEDs blinking simultaneously indicates that the user can safely power off the system using SW1 on the EVAL-TPG-ZYNQ3, and the power supplies for both boards can be powered down safely.
- 3. For receiver testing on the ADRV-DPD1/PCBZ evaluation kit, use a high quality signal generator with low phase noise to provide an input signal to the selected RF input. Use a low loss  $50 \Omega$  SMA coaxial cable and keep the cable as short as possible to reduce cable losses and interference pickup from local base stations. The SMA cable attaches the SMA F to SMP F adapter and into either Antenna Connection 1 or Antenna Connection 2 on the radio board.
  - a. To set the input level near the receiver full scale, it is recommended to set the generator level (for a single tone signal) to approximately –15 dBm. This level depends on the input frequency and the gain settings through the receiver path (see the RF Path and DPD Controls section). Do not apply an input signal to the receiver inputs when performing an initial calibration.
  - b. The observation receiver input level depends on the transmitter output power and the loss of the RF feedback path. When the transmitter output is transmitting at full power, the observation receiver signal peaks must not reach full scale. For correct DPD operation, reduce the gain if the observation receiver comes close to clipping.
  - c. The sniffer receivers are not connected on the ADRV-DPD1/PCBZ and cannot be used.
- 4. For transmitter testing, connect a spectrum analyzer to either transmitter output on the ADRV-DPD1/PCBZ. Use a low loss  $50 \Omega$  SMA coaxial cable to connect the spectrum analyzer. It is recommended that the power amplifier (PA) be disabled while initial calibrations are running to prevent high power test tones from appearing at the antenna. The SMA cable attaches to the SMA F to SMP F adapter and into either Antenna Connection 1 or Antenna Connection 2 on the radio board.
- Shutdown must be executed using the SCES software. Alternatively, the user can shut down the Zynq system using the SW9 push button (see Figure 9). These shutdown

methods prevent corruption of the SD card. The shutdown takes 25 sec. When the EVAL-TPG-ZYNQ3 LEDs blink simultaneously, the user can safely turn off the evaluation system by switching SW1 off (see Figure 9), and turn off the interposer board by switching the power supply off.

### SCES QUICKSTART

After the user follows the steps in the Normal Operation section, the software is fully connected to the device. Complete the following steps to create a basic setup of the different modes.

For all basic setups, the attached reference clock must be set by completing the following steps:

- 1. Connect the reference clock source to SMA Connector A or SMA Connector B on the interposer board with the frequency that matches that of the reference signal. Other frequencies can also be used. If other frequencies are used, attach the reference signal to either clock input.
- 2. In the evaluation software under the **Config** tab, select **Interposer** in the tree diagram on the left under **DaughterCard**.
- 3. Select the reference frequency for the attached clock signal on the left and the connector that is connected on the right.

### **Basic Receiver Setup**

For a basic receiver setup, complete the following steps:

- In the evaluation software, select AD9375 Radio under the DaughterCard tree in the Config tab and select the Configuration tab. For Rx Chnl, select RX1\_RX2.
- 2. Select an **Rx Profile** to receive from the signal generator or leave it at the default value.
- 3. Ensure that the frequency of **Rx PLL** matches that of the signal generator carrier frequency.
- 4. Click **Program** in the menu bar. The programming progress is located in the bottom right of the window. Wait for this progress bar to finish before proceeding to the next step.
- 5. Click the **Receive Data** tab (see the Receive Data Options section for more information).
- 6. Click the **Play** button in the toolbar. Observe the waveform transmitted from the signal generator output attached to the subminiature push on (SMP) connectors on the radio board.

### **Basic Transmitter Setup**

For a basic transmitter setup, complete the following steps:

- In the evaluation software, select AD9375 Radio under the DaughterCard tree in the Config tab and select the Configuration tab. For Tx Chnl, select TX1\_TX2.
- 2. Select a **Tx Profile**. Any profile is operable, but select a profile that matches the signal received on a spectrum analyzer.
- 3. Set the **Tx PLL** frequency to the carrier frequency received at the spectrum analyzer.

- 4. Click **Program** in the menu bar. The programming progress can be seen in the bottom right of the window. Wait for the progress bar to finish before proceeding to the next step.
- 5. Click the **Transmit Data** tab (see the Transmitter Setup section and Figure 59 for more information).
- 6. Load waveforms onto Tx1 and Tx2 with the Load Waveform buttons, labeled Load TX1 and Load TX2. There are several waveforms included with the software. Note that the software scales the waveform to full scale 0 dBFS if Scaling required is selected in the Select a file window. Alternatively, tone parameters can be set to generate basic waveforms.
- 7. Set the Tx RF attenuation and waveform digital attenuation for each Tx channel.
- 8. Click **Run Cals.** This process takes a few seconds and the button becomes clickable again once the process is completed.
- 9. Click **Play** in the **Transmit Data** tab toolbar. After a few seconds, the waveform that is sent to the gain amplifier appears.
- 10. Switch on the gain amplifier in the **RF Control** tab for the antenna or antennas that have spectrum analyzers connected to them.
- 11. Switch on the corresponding power amplifiers for the same antennas.
- 12. When powering down, power down the amplifiers in reverse order. Then the user can then stop or change the waveform in the **Transmit Data** tab to avoid sending unwanted power to the spectrum analyzer.

### **Basic DPD Setup**

For a basic DPD setup, complete the following steps:

- After following the steps in the Basic Transmitter Setup section, return to the **Config** tab and ensure that a TxDPD profile is set in the **Tx Profile** dropdown menu (see Figure 39).
- 2. In the **Calibration** tab, enable all the internal transmitter local oscillator leakage (LOL) and quadrature error correction (QEC) options.
- 3. Click **Program** to program the device and wait for the programming to complete.
- 4. Ensure that all the transmitter LOL and QEC tracking options are enabled on the left of the **Transmit Data** tab.
- 5. Click **Run Cals**. This calibration takes a few seconds; the button becomes clickable when calibration is completed.
- 6. Click the **Play** button in the **Transmit Data** toolbar. After a few seconds, the waveform that is being sent to the gain amplifier appears.
- 7. Switch on the gain amplifier for the antenna or desired antenna ports.
- 8. Switch on the corresponding power amplifiers for the antenna ports.
- 9. Click the **DPD Control** tab.
- 10. Select the checkboxes for the desired outputs to enable DPD.
- 11. Click **Start DPD** (see Figure 62). Note that the adjacent channel leakage drops on the spectrum analyzer.
- 12. When powering down, disable the DPD by clicking Reset DPD (see Figure 62), and power off the amplifiers in reverse order. The user can then stop or change the waveform in the Transmit Data tab.

## **EVALUATION KIT HARDWARE**

This section documents both the interposer board (ADRV-INTERPOS1/PCBZ) and the radio board (ADRV-DPD1/PCBZ) reference design. Figure 10 shows the radio board reference design block diagram. The radio board connects to the interposer board, which interfaces the radio board with the EVAL-TPG-ZYNQ3 for controlling it with the SCES.



Figure 10. AD9375 SCRD Radio Board Receiver and Transmitter RF Paths

### **POWER SUPPLY CONNECTION**

There are three power supply connectors on the interposer board: J14, J15, and J26. The power for the interposer board typically comes from J14 with a 2-wire CUI PJ-102BH power supply connector at 12 V. The provided universal ac to dc power adaptor is recommended for powering the interposer board. A laboratory power supply can be used if desired. When using a laboratory power supply, it must supply a nominal dc input voltage of 12 V  $\pm$ 5% and supply 2.0 A for a single radio board or 3.5 A for two simultaneously connected to the interposer board. The DCPP2 series FC6814671 plug (5.5 mm barrel plug to fit a connector with a 2.5 mm center pin) crimped with 16 AWG wire is recommended for use with a laboratory power supply.

The universal ac to dc power adaptor included in this evaluation kit requires an IEC C13 cord to connect to the local ac power outlet. The IEC C13 power cord is not included as part of the evaluation kit.

The J15 and J26 power terminal connectors are labeled as external 5.1 V input, but the connectors are not necessary to power attached radio boards. This voltage is also not recommended to power the radio board using these connectors because the power is provided from the on-board power distribution when the interposer board is switched on. The J15 and J26 connectors can be used for probing the radio board supply voltages when desired. The other points that can be probed are the not-fitted header Pin J27 and Pin J32. These pins can provide a more accurate reading of the 5.1 V supply, as shown in Figure 72 and Figure 73.

The interposer board is designed with a Schottky diode to protect against accidental connection of reverse polarity dc power and a transient voltage suppressor (TVS) diode to protect against overvoltage.

Take care to avoid applying voltages below -0.3 V or above +14.5 V. Applying voltages below -0.3 V or above +14.5 V can cause one or more of these protective diode clamps to conduct, resulting in large current flow that could blow the fuse. Prolonged application of reverse voltage or overvoltage at high currents can also damage the protection circuitry or blow the on-board fuse.



Figure 11. 12 V DC Barrel Power Connector



Figure 12. Power Supply Diagram

## ADRV-DPD1/PCBZ TOP AND BOTTOM VIEW PHOTOGRAPHS



Figure 13. ADRV-DPD1/PCBZ Top View with Heatsink Removed

The top side of the ADRV-DPD1/PCBZ interfaces with the heatsink using a thermal gasket. It is possible but not recommended to remove the heatsink by removing three screws on the rear side of the board (as shown in Figure 13).



Figure 14. ADRV-DPD1/PCBZ Bottom View

The bottom side of the PCB directly interfaces with the interposer board via the SAMTEC 100-way 0.8 mm pitch system connector. For more information, see Table 25.

UG-1238



Figure 16. Thermal Gasket and Heatsink Mechanical Drawing Side View

## ADRV-DPD1/PCBZ User Guide



Figure 17. 3D CAD Drawing of Reference Design



Figure 18. 3D CAD Drawing of Reference Design with Heatsink Removed

### Table 1. LTE Band 7 Configuration<sup>1</sup>

	Frequ		
Frequency Band	Up-Link (MHz)	Down-Link (MHz)	Duplex
7	2500 to 2570	2620 to 2690	FDD

<sup>1</sup> Other LTE bands hardware customizations are available upon request.

### Table 2. Power Consumption

		Value			
Parameter	Min	Тур	Max	Unit	Test Conditions
Total Current		2060	2100	mA	$V_{DD} = 5 V$ , VDD_IF = 2.5 V, 2T2R, LTE 20 MHz BW, 24 dBm output power (O/P), DPD enabled
Total Power Consumption		10.3	10.5	W	V <sub>DD</sub> = 5 V, VDD_IF = 2.5 V, 2T2R, LTE 20 MHz BW, 24 dBm O/P, DPD enabled
Total Power Dissipation		9.8	10	W	$V_{DD}$ = 5 V, VDD_IF = 2.5 V, 2T2R, LTE 20 MHz BW, 24 dBm O/P, DPD enabled

### **INTERPOSER BOARD REFERENCE**



Figure 19. Interposer Board Attached to Radio Board, Heatsink Removed (Top View)

### SYSTEM REFERENCE CLOCKS

Two system reference clock options are available to provide a reference clock input to the AD9528 JESD204B clock generator. Reference A is the default 10.00 MHz input. Reference B is the default 30.72 MHz input.

It is recommended to use only one input at a time so that the system operates correctly. The selection of the clock source is modified using the SCES (see the Clock Setup section for more details).



Figure 20. Reference Clock Inputs and Outputs

The input impedance on both clock inputs is 1 M\Omega dc and 100  $\Omega$  ac.

Clock input signals are ideally in the form of a square wave input in the range of -7 dBm to +3 dBm, although a sine wave input is also acceptable.

In addition, there is an option to fit Resistor R45, Resistor R46, Resistor R52, and Resistor R53 (51  $\Omega$ , 0402 size) to the interposer board to give REF\_A and REF\_B a 50  $\Omega$  input impedance.

The system reference clock frequencies mentioned previously are default options. However, the hardware is compatible with reference frequencies from 10 MHz to 80 MHz. Consult the product data sheet for further details on AD9528 PLL operation.

### LED INDICATORS

There are eight LED indicators in the interposer to show the status of the board.



Figure 21. LED Indicators

LED Order <sup>1</sup>	LED Name	Color	Function
1	LED 5	Green	+12 VDC (VIN_DC) present.
2	LED 8	Green	+3.9 VDC (VCC_3V9) present from ADP5054ACPZ-R7 (SW3).
3	LED 9	Green	+3.3 VDC (VCC_3V3) present from ADM7154ARDZ-3.3-27.
4	LED 12	Red	ADP5054 PWRGD output. Illuminates when ADP5054 Channel 1 (VCC_5V1_A) voltage is not correct.
5	LED 11	Green	+5.1 VDC for RF Module B (VCC_5V1_B). Present from ADP5054ACPZ-R7 (SW2)
6	LED 7	Green	+5.1 VDC for RF Module A (VCC_5V1_A). Present from ADP5054ACPZ-R7 (SW1).
7	LED 1	Green	AD9528 STATUS_1 output. Normally programmed as PLL2 lock indicator.
8	LED 2	Green	AD9528 STATUS_0 output. Normally programmed as PLL1 lock indicator.

### Table 3. List of LEDs and Associated Functions

<sup>1</sup> The order of LEDs here is not sequential to how they are listed on the card. See Figure 21 for order of LEDs.

### ADP5054 ENABLE JUMPER

The ADP5054 enable jumper, labeled J16, is used to select the mode of operation for the ADP5054 power regulator. The modes are as follows:

- Always off: ADP5054 is disabled.
- Automatic: ADP5054 is enabled upon detection of PGOOD signal from EVAL-TPG-ZYNQ3.
- Always on: ADP5054 is enabled whenever 12 V is present on the dc power connector.

For typical operation, place a jumper in the automatic position, shorting Pin 3 and Pin 4. Pin 1 is indicated by a white dot on the board.

### **EEPROM WRITE PROTECT ENABLE HEADERS**

There are two electronical erasable program memory (EEPROM) write protect enable headers provided on the interposer board, one per RF card. These headers enable or disable write operations to the RF calibration data serial peripheral interface (SPI) EEPROM accessible via the SPI bus and located on the RF card. Note that the SPI EEPROM is currently unsupported in the GUI (SCES), API, and interposer board.



Figure 23. EEPROM Write Protect Header RF A



Figure 22. ADP5054 Enable Jumper



Figure 24. EEPROM Write Protect Header RF B

16493-224

Placement of the jumper ensures that the write protect line is enabled and write operations to the EEPROM are disabled. Removing the header allows write operations to be carried out on the EEPROM over the SPI interface, controlled from the EVAL-TPG-ZYNQ3.

### **DEBUG HEADERS**

There are three sets of headers intended as a debug aid to probe signals required for interfacing the RF card and interposer board with the EVAL-TPG-ZYNQ3 platform. The main RF headers have 16-way IDC type connectors that are recommended to be used as protection from shorting pins together accidentally. The 16-way 28 American wire gauge (AWG) ribbon cable can be crimped into these connectors for probing the pins with a logic analyzer or multimeter. A single white dot on the silkscreen indicates Pin 1. Subsequent pins can be then be determined from the schematic in Figure 89.

### **RF A Header Pins**

The RF A headers are located adjacent to where the RF A card fits on the interposer board, as shown in Figure 25. For a complete listing of RF A pin functions and descriptions, see Table 7 and Table 8.



Figure 25. RF A Debug Header Pins

### **RF B Header Pins**

The headers for RF B are located near the interposer board LEDs, as shown in Figure 26. The RF B signals are accessible on the J1 and J9 connectors. For a complete listing of RF B pin functions and descriptions, see Table 9 and Table 10.



Figure 26. RF B Debug Header Pins

### JTAG Header Pins

The JTAG interface can be probed using the JTAG headers (Figure 27) at J7 with a 2 × 10, 20-way, 0.05 inch pitch rectangular connector that is not included in the evaluation kit. The SAMTEC cable assembly with the FFSD-10-S-12.00-01-N part number is recommended for connecting to these header pins. Note that this JTAG cable connector does not fit if the J2 connector is also attached at the J2 header pins. As such, only the J2 connector or the JTAG interface must be connected at any one time. Take care when connectors are removed from header pins because there is a danger of shorting pins. Insulating tape is recommended to cover the J2 headers when the JTAG headers are in use.

For JTAG boundary scan, refer to the AD9375 System Development User Guide for more information. For a complete list of JTAG pins and descriptions, see Table 11.

### SPI CHIP SELECT LINES

The chip select (CS) lines from the EVAL-TPG-ZYNQ3 card via the FMC are encoded and are decoded by the CS decoder circuit on the interposer board shown in Figure 82. The chip select codes for each device are detailed in Table 4 with FMC\_SPI\_CS0 being the least significant bit (LSB) and FMC\_SPI\_CS4 the most significant bit (MSB). The codes for each chip select are detailed in Table 4. The Selected Chip Acronym column refers to the name written on the schematics in the interposer board schematics section.

CS0 to CS2 are the device selects, CS3 is the radio board select, and CS4 is for address space expansion. The clock generator on the interposer board appears as an RF A device.



Figure 27. JTAG Debug Header Pins

### Table 4. SPI Encoding Codes

Chip Select Code	Selected Chip Acronym	Description
00000	SPI_DRV1_CS_A	Chip select driver amplifier on Tx1 on RF Card A, active low.
00001	SPI_DRV2_CS_A	Chip select driver amplifier on Tx2 on RF Card A, active low.
00010	SPI_SPARE_CS2	No connect on the ADRV-DPD1/PCBZ.
00011	SPI_EEPROM_CS_A	Selects the SPI EEPROM on RF Card A.
00100	SPI_SPARE_CS0	No connect on the ADRV-DPD1/PCBZ.
00101	SPI_PLL_CS	Selects the AD9528 phase locked loop generator.
00110	SPI_MYK_CS_A	Selects the transceiver device on the RF A Card.
00111, 01111, 1xxxx	NC	No connect.
01000	SPI_DRV1_CS_B	Chip select driver amplifier on Tx1 on RF Card B, active low.
01001	SPI_DRV2_CS_B	Chip select driver amplifier on Tx2 on RF Card B, active low.
01010	SPI_SPARE_CS3	No connect on the ADRV-DPD1/PCBZ.
01011	SPI_EEPROM_CS_B	Selects the SPI EEPROM on RF Card B.
01100	SPI_SPARE_CS1	No connect on the ADRV-DPD1/PCBZ.
01101	NC	No connect.
01110	SPI_MYK_CS_B	Selects the transceiver device on the RF B Card.

## **PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS**

Not all connections are present on the reference design card that are present on the interposer board. These connections are noted in the pin description.



Figure 28. RF Card Pin Configuration

RF Pin No.	Mnemonic	Tvpe <sup>1</sup>	Description	l/O Voltage
1, 2, 7, 8, 13, 14, 19, 20, 25, 26, 32, 38, 44, 49, 50, 56, 61, 66, 75, 76, 85, 89, 90, 91, 92	GND	GND	Connected to Ground.	
3, 5	SYNCINB1–, SYNCINB1+	I	Low Voltage Differential Signaling (LVDS) Sync Signal Associated with Observation Receiver/Sniffer Channel Data on the JESD204B Interface.	LVDS
4, 6	SERDOUT3–, SERDOUT3+	0	RF Current Mode Logic (CML) Differential Output 3. This JESD204B lane can be used by the receiver data or by the sniffer/observation receiver data.	CML
9, 11	SYNCINB0, SYNCINB0+	I	LVDS Sync Signal Associated with Receiver Channel Data on the JESD204B Interface.	LVDS
10, 12	SERDOUT1-, SERDOUT1+	0	RF CML Differential Output 1. This JESD204B lane can be used by receiver data or by sniffer/observation receiver data.	CML
15, 17	SYSREF_IN-, SYSREF_IN+	I	LVDS System Reference Clock Inputs for the JESD204B Interface.	LVDS
16, 18	SERDOUT2-, SERDOUT2+	0	RF CML Differential Output 2. This lane can be used by the receiver data or by the sniffer/observation receiver data.	CML
21, 23	DEV_CLK_IN–, DEV_CLK_IN+	I	Device Clock LVDS Input, AC-Coupled with a 0.10 $\mu\text{F}$ Capacitor.	LVDS
22, 24	SERDOUT0-, SERDOUT0+	0	RF CML Differential Output 0. This JESD204B lane can be used by receiver data or by sniffer/observation receiver data.	CML
27	TX2_ENABLE	I	Enable for Tx2 on the Transceiver Device. On the ADRV-DPD1/PCBZ, this pin is not connected because the TX1_ENABLE pin enables both Tx1 and Tx2 simultaneously.	VDD_IF
28, 30	SERDIN2–, SERDIN2+	I	RF CML Differential Input 2.	CML
29	RX2_ENABLE	I	Enable for Rx2 on the Transceiver Device. On the ADRV-DPD1/PCBZ, this pin is not connected because the RX1_ENABLE pin enables both Rx1 and Rx2 simultaneously.	VDD_IF
31	nPRESENCE RF		Connected to Ground on Radio Board to Indicate Connection to Interposer Board.	
33, 35	TX_DRV1_EN, TX_DRV2_EN	I	Enable Line for Tx1 and Tx2 Drivers. This signal is buffered.	VDD_IF
34, 36	SERDINO-, SERDINO+	I	RF CML Differential Input 0.	CML
37	RX1_RADIO_EN	I	Enables the Rx1 and Rx2 Signal Paths on the AD9375.	VDD_IF
39, 41	RX_LNA1_EN, RX_LNA2_EN	I	Enables the LNA for Rx1 and Rx2 Signal Paths. These lines are buffered.	VDD_IF
40, 42	SERDIN3–, SERDIN3+	I	RF CML Differential Input 3.	CML
43	TX1_RADIO_EN	I	Enables the Tx1 and Tx2 Signal Paths on the AD9375.	VDD_IF
45, 47	TX_PA1_EN, TX_PA2_EN	I	Enable the SKY66297-11 PA for Tx1 and Tx2 Independently.	VDD_IF
46, 48	SERDIN1-, SERDIN1+	I	RF CML Differential Input 1.	CML
51	GPIO17	I/O	General-Purpose Input and Output. This pin is not connected on the ADRV-DPD1/PCBZ.	VDD_IF

Table 5. RF Card Pin Function Descriptions

RF Pin No.	Mnemonic	Type <sup>1</sup>	Description	l/O Voltage
52, 54	SYNCOUTB0–, SYNCOUTB0+	0	LVDS Sync Signal Associated with Transmitter Channel Data on the	LVDS
53	EEPROM_WP	I	Write Protect the SPI EEPROM when Low, Enabled by Jumper on Interposer Board.	GND
55	SPI_EEPROM_CS	I	Select EEPROM for SPI Communication, Active Low. Pull up this pin to 3.3 V when this pin is floating.	GND
57	SPI_DRV2_CS	I	Select Tx2 Driver for SPI Communication, Active Low. Pull up this pin to 3.3 V when this pin floating.	GND
58	GPIO11	I/O	General-Purpose Input and Output. This pin is not connected on the ADRV-DPD1/PCBZ.	VDD_IF
59	SPI_DRV1_CS	I/O	Select Tx1 Driver for SPI Communication, Active Low. Pull up this pin to 3.3 V when this pin is floating.	GND
60	GPIO12	I/O	General-Purpose Input and Output. This pin is not connected on the ADRV-DPD1/PCBZ.	VDD_IF
62	GPIO13	I/O	General-Purpose Input and Output. This pin is not connected on the ADRV-DPD1/PCBZ.	VDD_IF
63	SPI_MYK_CS	I	Chip Select AD9375 (Mykonos) Device for SPI Communication, Active Low. Pull up this pin to VDD_IF when this pin floating.	GND
64	GPIO14	I/O	General-Purpose Input and Output. This pin is not connected on the ADRV-DPD1/PCBZ.	VDD_IF
65	SPI_SCLK	I	Serial Clock for SPI Communication Referenced to VDD_IF.	VDD_IF
67	SPI_MOSI	I/O	Master Output Slave Input for SPI. This pin is used to write to selected device when device uses 4-wire SPI. Pull up this pin to VDD_IF included.	VDD_IF
68	GPIO15	I/O	General-Purpose Input and Output. This pin is not connected on the ADRV-DPD1/PCBZ.	VDD_IF
69	SPI_MISO	0	Master Input Slave Output for SPI. This pin is used to read from selected device when the device is a 4-wire SPI or as a half-duplex line when the device is a 3-wire SPI. See the SPI Chip Select Lines to understand which chip is selected. Pull up this pin to VDD_IF included.	VDD_IF
70	GPIO8	I/O	General-Purpose Input and Output. This pin is not connected on the ADRV-DPD1/PCBZ.	VDD_IF
71	GP_INTERRUPT	0	General-Purpose AD9375 Interrupt Signal Output.	VDD_IF
72	GPIO9	I/O	General-Purpose Input and Output. This pin is not connected on the ADRV-DPD1/PCBZ.	VDD_IF
73	RESET	I	Active Low AD9375 Reset. Pull up this pin to VDD_IF included.	VDD_IF
74	GPIO10	I/O	General-Purpose Input and Output. No pull-up resistor on ADRV- DPD/PCBZ.	VDD_IF
77	GPIO0	I/O	General-Purpose Input and Output. No pull-up resistor on ADRV- DPD/PCBZ.	VDD_IF
78	GPIO4	I/O	General-Purpose Input and Output. Pull-up resistor included on ADRV-DPD1/PCBZ.	VDD_IF
79	GPIO1	I/O	General-Purpose Input and Output. No pull-up resistor on ADRV- DPD/PCBZ.	VDD_IF
80	GPIO5	I/O	General-Purpose Input and Output. Pull-up resistor included on ADRV-DPD1/PCBZ.	VDD_IF
81	GPIO2	I/O	General-Purpose Input and Output. No pull-up resistor on ADRV- DPD/PCBZ.	VDD_IF
82	GPIO6	I/O	General-Purpose Input and Output. Pull-up resistor included on ADRV-DPD1/PCBZ.	VDD_IF
83	GPIO3	I/O	General-Purpose Input and Output. No pull-up resistor on ADRV- DPD/PCBZ.	VDD_IF
84	GPIO7	I/O	General-Purpose Input and Output. Pull-up resistor included on ADRV-DPD1/PCBZ.	VDD_IF
86	GPIO18	I/O	General-Purpose Input and Output. Pull-up resistor included on ADRV-DPD1/PCBZ.	VDD_IF
87	VDD_IF	Р	CMOS/LVDS Interface Supply to Radio Board.	+2.5 V

## ADRV-DPD1/PCBZ User Guide

RF Pin No.	Mnemonic	Type <sup>1</sup>	Description	l/O Voltage
88	TEST	I	See AD9375 User Guide for JTAG Boundary Scan.	VDD_IF
93 to 100	POWER	Ρ	5 V Supply Connection to Power the Board. Pin 100 is used as a sense line on the PAs.	+5 V

<sup>1</sup> P is power, I is input, O is output, I/O is input/output, and GND is ground.

The ground connections are not indicated in the pin configuration detailed in Table 6, as all ground connections are marked in the ANSI/VITA 57.1 FPGA mezzanine card (FMC) standard. These connections are also marked in Figure 92, Figure 93, Figure 94, and Figure 95.

The FMC HPC connector pin configuration consists of the following interfaces:

- JESD204B high speed interface between the host (EVAL-TPG-ZYNQ3) and radio transceiver (AD9375). A detailed Analog Devices interface specification is provided in the AD9528 data sheet.
- A subset of the AD9375 GPIOs routed via the interposer.

- PA and LNA control lines for transmit and receive operations.
- SPI interface for AD9375 radio transceiver, as specified in the AD9528 data sheet.
- SPI interface for EEPROM (ON SEMI CAT25128YI-GT3). The AD9375 system development user guide is available as part of the AD9375 design files zip package.
- SPI interface for ADL5335 PGA.
- VDD\_IF (2.5 V), CMOS, and LVDS signal power. 3P3AUX (3.3 V) for the interposer board I<sup>2</sup>C EEPROM, VCC12\_P (12 V) is unused on the interposer board.



#### Table 6. FMC HPC Connector Pin Function Descriptions

Pin No.	EVAL-TPG-ZYNQ3 Mnemonic	Interposer Board Mnemonic	Description
A2, A3	FMC_HPC_DP1_M2C_P,	SERDOUTO_A+,	JESD204B Serial Data From EVAL-TPG-
	FMC_HPC_DPT_M2C_N	SERDOUTO_A-	ZYNQ3 to RF Card A.
A6, A7	FMC_HPC_DP2_M2C_P, FMC_HPC_DP2_M2C_N	SERDOUT1_A+, SERDOUT1_A–	JESD204B Serial Data From EVAL-TPG- ZYNO3 to RF Card A.
A10, A11	FMC_HPC_DP3_M2C_P,	SERDOUT3_A+,	JESD204B Serial Data From EVAL-TPG-
A14, A15	FMC_HPC_DP4_M2C_P,	SERDOUTO_B+,	JESD204B Serial Data From EVAL-TPG-
A10 A10			LESD204B Carial Data From EVAL TRC
A18, A19	FMC_HPC_DP5_M2C_P, FMC_HPC_DP5_M2C_N	SERDOUT1_B+, SERDOUT1_B-	ZYNQ3 to RF Card B.
A22, A23	FMC_HPC_DP1_C2M_P, FMC_HPC_DP1_C2M_N	SERDIN3_A+, SERDIN3_A–	JESD204B Serial Data From RF Card A to EVAL-TPG-ZYNQ3.
A26, A27	FMC_HPC_DP2_C2M_P, FMC_HPC_DP2_C2M_N	SERDINO_A+, SERDINO_A-	JESD204B Serial Data From RF Card A to EVAL-TPG-ZYNQ3.
A30, A31	FMC_HPC_DP3_C2M_P, FMC_HPC_DP3_C2M_N	SERDIN2_A+, SERDIN2_A–	JESD204B Serial Data From RF Card A to EVAL-TPG-ZYNQ3.
A34, A35	FMC_HPC_DP4_C2M_P, FMC_HPC_DP4_C2M_N	SERDINO_B+, SERDINO_B-	JESD204B Serial Data From RF Card B to EVAL-TPG-ZYNQ3.
A38, A39	FMC_HPC_DP5_C2M_P, FMC_HPC_DP5_C2M_N	SERDIN1_B+, SERDIN1_B–	JESD204B Serial Data From RF Card B to EVAL-TPG-ZYNQ3.
B1, B4, B5, B8, B9	NC	NC	No Connect.
B12, B13	FMC_HPC_DP7_M2C_P, FMC_HPC_DP7_M2C_N	SERDOUT2_B+, SERDOUT2_B–	JESD204B Serial Data From EVAL-TPG- ZYNQ3 to RF Card B.
B16, B17	FMC_HPC_DP6_M2C_P, FMC_HPC_DP6_M2C_N	SERDOUT3_B+, SERDOUT3_B–	JESD204B Serial Data From EVAL-TPG- ZYNQ3 to RF Card B.
B20, B21	FMC_HPC_GBTCLK1_M2C_P, FMC_HPC_GBTCLK1_M2C_N	FPGA_REF_CLK_A+, FPGA_REF_CLK_A–	Reference Clock A from AD9528 to FPGA.
B24, B25, B28, B29	NC	NC	No Connect.
B32, B33	FMC_HPC_DP7_C2M_P, FMC_HPC_DP7_C2M_N	SERDIN2_B+, SERDIN2_B–	JESD204B Serial Data From RF Card B to EVAL-TPG-ZYNQ3.

## ADRV-DPD1/PCBZ User Guide

Pin No.	EVAL-TPG-ZYNQ3 Mnemonic	Interposer Board Mnemonic	Description
B36, B37	FMC_HPC_DP6_C2M_P, FMC_HPC_DP6_C2M_N	SERDIN3_B+, SERDIN3_B–	JESD204B Serial Data From RF Card B to EVAL-TPG-ZYNQ3.
B40	NC	NC	No Connect.
C2, C3	FMC_HPC_DP0_C2M_P, FMC_HPC_DP0_C2M_N	SERDIN1_A+, SERDIN1_A–	JESD204B Serial Data From RF Card A to EVAL-TPG-ZYNQ3.
C6, C7	FMC_HPC_DP0_M2C_P, FMC_HPC_DP0_M2C_N	SERDOUT2_A+, SERDOUT2_A-	JESD204B Serial Data From EVAL-TPG- ZYNO3 to RF Card A.
C10, C11	FMC_HPC_LA06_P, FMC_HPC_LA06_N	FMC_TX1_DRV_EN_A, FMC_TX2_DRV_EN_A	Tx1 and Tx2 Driver Amplifier Enable for RF Card A, Prebuffer.
C14, C15	FMC_HPC_LA10_P, FMC_HPC_LA10_N	FMC_SPI_CS3, FMC_SPI_CS4	SPI Chip Select Multiplex Bits from EVAL- TPG-ZYNQ3 to Interposer Board.
C18, C19	FMC_HPC_LA14_P, FMC_HPC_LA14_N	FMC_TX2_ENABLE_A, FMC_RX2_ENABLE_A	Tx2 and Rx2 Enable on RF Card A Transceiver Device.
C22, C23	FMC_HPC_LA18_CC_P, FMC_HPC_LA18_CC_N	GPIO6_A, GPIO7_A	General-Purpose Input and Output.
C26, C27	FMC_HPC_LA27_P, FMC_HPC_LA27_N	FMC_TDD1_SWITCH_A, FMC_TDD2_SWITCH_A	Time Division Duplex 1 and Duplex 2 Switch on RF Card A. No connect on Rev A interposer board 100-pin connector, prebuffer.
C30	FMC_HPC_IIC_SCL	FMC_I2C_SCL	I <sup>2</sup> C Interface Clock.
C31	FMC_HPC_IIC_SDA	FMC_I2C_SDA	I <sup>2</sup> C Interface Data.
C34	 GA0	EEPROM A0	I <sup>2</sup> C EEPROM Address Bit 0.
C35. C37	VCC12 P	FMCA VCC 12P0V	12 V from EVAL-TPG-ZYNO3 Card.
C39	VCC3V3	3P3V	3 3 V from EVAL-TPG-ZYNO3 Card
D1	PWRCTL1_FMC_PG_C2M	ADP5054_EN	ADP5054 Enabled Signal from Interposer Board to EVAL-TPG-ZYNQ3.
D4, D5	FMC_HPC_GBTCLK0_M2C_P, FMC_HPC_GBTCLK0_M2C_N	FPGA_REF_CLK_B+, FPGA_REF_CLK_B–	Reference Clock B from AD9528 to FPGA.
D8, D9	FMC_HPC_LA01_CC_P, FMC_HPC_LA01_CC_N	SYSREF_FROM_FPGA+, SYSREF_FROM_FPGA-	SYSREF from EVAL-TPG-ZYNQ3 to AD9528 on Interposer Board.
D11	FMC_HPC_LA05_P	FMC_TEST	JTAG Test Signal from EVAL-TPG-ZYNQ3 to Interposer Board.
D12	FMC_HPC_LA05_N	GPIO18_A	General-Purpose Input and Output.
D14, D15	FMC_HPC_LA09_P, FMC_HPC_LA09_N	FMC_SPI_CS0, FMC_SPI_CS1	SPI Chip Select Multiplex Bits from EVAL- TPG-ZYNQ3 to Interposer Board.
D17, D20, D18, D21	FMC_HPC_LA13_P, FMC_HPC_LA17_CC_P, FMC_HPC_LA13_N, FMC_HPC_LA17_CC_N	FMC_TX1_ENABLE_A, FMC_TX2_ENABLE_B, FMC_RX1_ENABLE_A, FMC_RX2_ENABLE_B	Tx1, Tx2, Rx1, and Rx2 Enable to the Indicated RF Card Transceiver Device.
D23, D24	FMC_HPC_LA23_P, FMC_HPC_LA23_N	FMC_RX1_LNA_ENABLE_A, FMC_RX2_LNA_ENABLE_A	Rx1 and Rx2 Low Noise Amplifier Enable on RF Card A, Postbuffer.
D26	FMC_HPC_LA26_P	FMC_CLK_RESET	Reset Signal to AD9528, Prebuffer.
D27	FMC_HPC_LA26_N	FMC_CLK_SYSREF_REQUEST	SYSREF Request Signal to AD9528, Prebuffer.
D29	FMC HPC TCK BUF	NC	No Connect on the Interposer Board.
D30	FMC TDI BUF	JTAG TDI	Loopback to the JTAG TDO Pin.
D31	EMC HPC TDO EMC LPC TDI	ITAG TDO	Loopback to the ITAG TDI Pin
237		3P3VALIX	3 3 V from EVAL-TPG-ZYNO3 Card
532		NC	No Connect on Internoser Board
D34		NC	No Connect on Interposer Board.
D34			12C EEDDOM Addross Bit 1
			-C EEPROM Address Bit 1.
030, 030, 040			S.S V HOILEVAL-IPG-ZINQS Cara.
E2, E3			No Connect.
			No connect.
E6, E7, E9, E10, E12, E13	NC	GPIO10_A, GPIO11_A, GPIO16_A, GPIO17_A, GPIO13_B, GPIO14_B	General-Purpose Input and Output. These pins are not connected on the EVAL-TPG-ZYNQ3.

Pin No.	EVAL-TPG-ZYNQ3 Mnemonic	Interposer Board Mnemonic	Description
E15, E16, E18, E19, E21, E22, E24, E25, E27, E28, E30, E31, E33, F34, F36, F37	NC	NC	No Connect.
E39, F40, G39, H40	VADJ	FMC_VDD_IF	LVDS Supply on EVAL-TPG-ZYNQ3 and CMOS Digital Power Supply for the Radio Board and Interposer Board.
F1	FMC_HPC_PG_M2C	3P3V	3.3 V from EVAL-TPG-ZYNQ3 Card.
F4, F5	NC	NC	No Connect.
F7, F8, F10, F11, F13, F14, F16, F17	NC	GPIO8_A, GPIO9_A, GPIO14_A, GPIO15_A, GPIO11_B, GPIO12_B, GPIO16_B, GPIO17_B	General-Purpose Input and Output. No connect on the EVAL-TPG-ZYNQ3.
F19, F20, F22, F23, F25, F26, F28, F29, F31, F32, F34, F35, F37, F38	NC	NC	No Connect.
G2, G3	FMC_HPC_CLK1_M2C_P, FMC_HPC_CLK1_M2C_N	NC	No Connect on Interposer Board.
G6, G7	FMC_HPC_LA00_CC_P, FMC_HPC_LA00_CC_N	FPGA_SYSREF+, FPGA_SYSREF-	SYSREF from Interposer Board to EVAL- TPG-ZYNQ3.
G9, G10	FMC_HPC_LA03_P, FMC_HPC_LA03_N	SYNCINB0_A+, SYNCINB0_A–	JESD204B SYNCIN Signal to RF Card A.
G12	FMC_HPC_LA08_P	FMC_SPI_MISO	SPI Data from EVAL-TPG-ZYNQ3 to Chip Selected. Also half duplex line for some devices, prebuffer.
G13	FMC_HPC_LA08_N	FMC_SPI_CS2	SPI Chip Select Multiplex Bits from EVAL- TPG-ZYNQ3 to Interposer Board.
G15, G16	FMC_HPC_LA12_P, FMC_HPC_LA12_N	FMC_TX1_ENABLE_B, FMC_RX1_ENABLE_B	Tx1 and Rx1 Enable on RF Card B Transceiver Device, Prebuffer.
G18, G19, G21, G22, G24, G25	FMC_HPC_LA16_P, FMC_HPC_LA16_N, FMC_HPC_LA20_P, FMC_HPC_LA20_N, FMC_HPC_LA22_P, FMC_HPC_LA22_N	GPIO2_A, GPIO3_A, GPIO4_B, GPIO5_B, GPIO0_B, GPIO1_B	General-Purpose Input and Output.
G27, G28	FMC_HPC_LA25_P, FMC_HPC_LA25_N	SYNCINB1_A+, SYNCINB1_A–	JESD204B SYNCIN signal to RF Card A.
G30, G31	FMC_HPC_LA29_P, FMC_HPC_LA29_N	GPIO6_B, GPIO7_B	General-Purpose Input and Output.
G33, G34	FMC_HPC_LA31_P, FMC_HPC_LA31_N	SYNCINB1_B+, SYNCINB1_B–	JESD204B SYNCIN Signal to RF Card B.
G36, G37	FMC_HPC_LA33_P, FMC_HPC_LA33_N	FMC_TX1_PA_ENABLE_B, FMC_TX2_PA_ENABLE_B	Tx1 and Tx2 Power Amplifier Enable on RF Card B, Prebuffer.
H1	NC	NC	No Connect.
H2	FMC_HPC_PRSNT_M2C_B	FMC_RF_PRESENCE	Active Low Presence Signal from Radio Board.
H4, H5	FMC_HPC_CLK0_M2C_P, FMC_HPC_CLK0_M2C_N	NC	No Connect on Interposer Board.
H7, H8	FMC_HPC_LA02_P, FMC_HPC_LA02_N	SYNCOUTB0_A+, SYNCOUTB0_A–	JESD204B SYNCOUT Signal to RF Card A.
H10	FMC_HPC_LA04_P	FMC_RESET_A	Reset Signal to Transceiver Device on RF Card A, Prebuffer.
H11	FMC_HPC_LA04_N	FMC_GP_INTERRUPT_A	General-Purpose Interrupt from the Transceiver Device on RF card A, Postbuffer.
H13	FMC_HPC_LA07_P	FMC_SPI_CLK	SPI Clock Signal from EVAL-TPG-ZYNQ3 to Selected Chip.
H14	FMC_HPC_LA07_N	FMC_SPI_MOSI	SPI Data from Chip Selected to EVAL-TPG- ZYNQ3, Prebuffer.