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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# 100-Tap Digitally Programmable Potentiometer (DPP™)

## FEATURES

- 100-position linear taper potentiometer
- Non-volatile EEPROM wiper storage
- 10 nA ultra-low standby current
- Single supply operation: 2.5 V – 6.0 V
- Increment up/down serial interface
- Resistance values: 1 kΩ, 10 kΩ, 50 kΩ and 100 kΩ
- Available in PDIP, SOIC, TSSOP and MSOP packages

## APPLICATIONS

- Automated product calibration
- Remote control adjustments
- Offset, gain and zero control
- Tamper-proof calibrations
- Contrast, brightness and volume controls
- Motor controls and feedback systems
- Programmable analog functions

**For Ordering Information details, see page 12.**

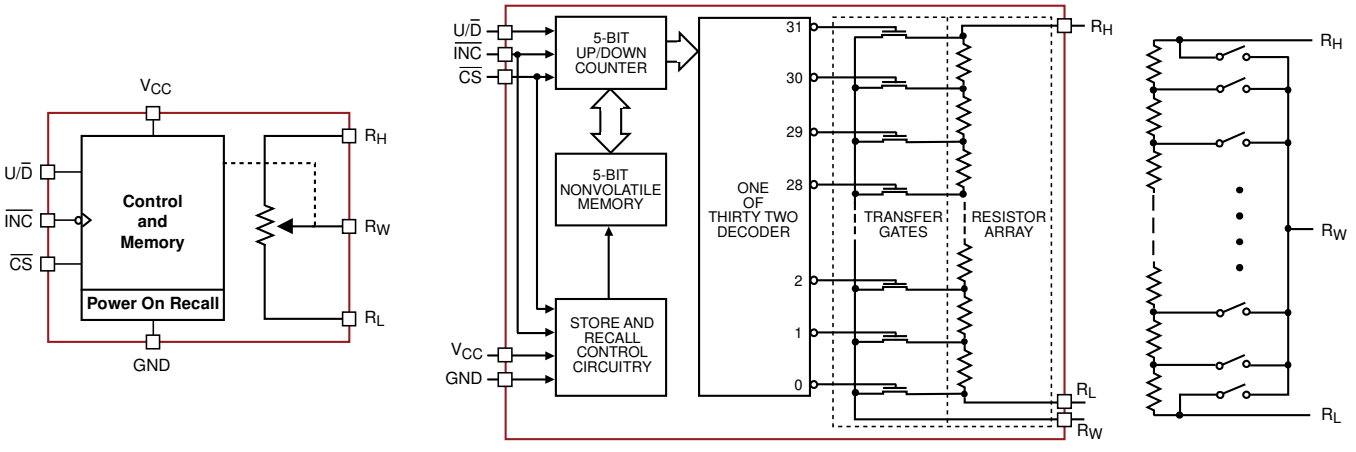
## DESCRIPTION

The CAT5113 is a single digitally programmable potentiometer (DPP™) designed as a electronic replacement for mechanical potentiometers. Ideal for automated adjustments on high volume production lines, they are also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The CAT5113 contains a 100-tap series resistor array connected between two terminals $R_H$ and $R_L$. An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper, $R_W$. The wiper setting, stored in nonvolatile memory, is not lost when the device is powered down and is automatically reinstated when power is returned. The wiper can be adjusted to test new system values without affecting the stored setting. Wiper-control of the CAT5113 is accomplished with three input control pins, $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$. The $\overline{INC}$ input increments the wiper in the direction which is determined by the logic state of the U/$\overline{D}$ input. The $\overline{CS}$ input is used to select the device and also store the wiper position prior to power down.

The digitally programmable potentiometer can be used as a three-terminal resistive divider or as a two-terminal variable resistor.

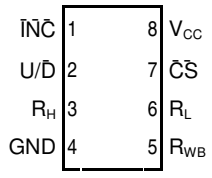
## FUNCTIONAL DIAGRAM



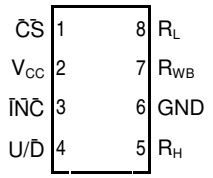

General | Detailed | Electronic Potentiometer Implementation

## PIN CONFIGURATION

**PDIP 8-Lead (L)**
**SOIC 8 Lead (V)**
**MSOP 8 Lead (Z)**




**TSSOP 8 Lead (Y)**




## PIN DESCRIPTIONS

| Name | Function |
|---|---|
| INC | Increment Control |
| U/D | Up/Down Control |
| $R_H$ | Potentiometer High Terminal |
| GND | Ground |
| $R_W$ | Wiper Terminal |
| $R_L$ | Potentiometer Low Terminal |
| CS | Chip Select |
| $V_{CC}$ | Supply Voltage |

## PIN DESCRIPTION

**INC:** Increment Control Input

The INC input moves the wiper in the up or down direction determined by the condition of the U/D input.

**U/D:** Up/Down Control Input

The U/D input controls the direction of the wiper movement. When in a high state and CS is low, any high-to-low transition on INC will cause the wiper to move one increment toward the $R_H$ terminal. When in a low state and CS is low, any high-to-low transition on INC will cause the wiper to move one increment towards the $R_L$ terminal.

**$R_H$:** High End Potentiometer Terminal

$R_H$ is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the $R_L$ terminal. Voltage applied to the $R_H$ terminal cannot exceed the supply voltage, $V_{CC}$ or go below ground, GND.

**$R_W$:** Wiper Potentiometer Terminal

$R_W$ is the wiper terminal of the potentiometer. Its position on the resistor array is controlled by the control inputs, INC, U/D and CS. Voltage applied to the $R_W$ terminal cannot exceed the supply voltage, $V_{CC}$ or go below ground, GND.

**$R_L$:** Low End Potentiometer Terminal

$R_L$ is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the $R_H$ terminal. Voltage applied to the $R_L$ terminal cannot exceed the supply voltage, $V_{CC}$ or go below ground, GND. $R_L$ and $R_H$ are electrically interchangeable.

**CS:** Chip Select

The chip select input is used to activate the control input of the CAT5113 and is active low. When in a high state, activity on the INC and U/D inputs will not affect or change the position of the wiper.

## DEVICE OPERATION

The CAT5113 operates like a digitally controlled potentiometer with $R_H$ and $R_L$ equivalent to the high and low terminals and $R_W$ equivalent to the mecha–nical potentiometer's wiper. There are 100 available tap positions including the resistor end points, $R_H$ and $R_L$. There are 99 resistor elements connected in series between the $R_H$ and RL terminals. The wiper terminal is connected to one of the 100 taps and controlled by three inputs, INC, U/D and CS. These inputs control a seven-bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in non-volatile memory using the INC and CS inputs.

With CS set LOW the CAT5113 is selected and will respond to the U/D and INC inputs. HIGH to LOW transitions on INC wil increment or decrement the wiper (depending on the state of the U/D input and seven-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever CS transitions HIGH while the INC input is also HIGH. When the CAT5113 is powered-down, the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With INC set low, the CAT5113 may be de-selected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in non. volatile memory.

## OPERATION MODES

| $\overline{INC}$ | $\overline{CS}$ | U/$\overline{D}$ | Operation |
|---|---|---|---|
| High to Low | Low | High | Wiper toward H |
| High to Low | Low | Low | Wiper toward L |
| High | Low to High | X | Store Wiper Position |
| Low | Low to High | X | No Store, Return to Standby |
| X | High | X | Standby |

## ABSOLUTE MAXIMUM RATINGS[1]

| Parameters | Ratings | Units |
|---|---|---|
| Supply Voltage | | |
| $V_{CC}$ to GND | -0.5 to +7 | V |
| Inputs | | |
| $\overline{CS}$ to GND | -0.5 to $V_{CC}$ +0.5 | V |
| $\overline{INC}$ to GND | -0.5 to $V_{CC}$ +0.5 | V |
| U/$\overline{D}$ to GND | -0.5 to $V_{CC}$ +0.5 | V |
| H to GND | -0.5 to $V_{CC}$ +0.5 | V |
| L to GND | -0.5 to $V_{CC}$ +0.5 | V |
| W to GND | -0.5 to $V_{CC}$ +0.5 | V |

| Parameters | Ratings | Units |
|---|---|---|
| Operating Ambient Temperature | | |
| Commercial ('C' or Blank suffix) | 0 to 70 | ºC |
| Industrial ('I' suffix) | -40 to +85 | ºC |
| Junction Temperature | +150 | ºC |
| Storage Temperature | -65 to 150 | ºC |
| Lead Soldering (10s max) | +300 | ºC |

## RELIABILITY CHARACTERISTICS

| Symbol | Parameter | Test Method | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{ZAP}$[2] | ESD Susceptibility | MIL-STD-883, Test Method 3015 | 2000 | | | V |
| $I_{LTH}$[2] [3] | Latch-Up | JEDEC Standard 17 | 100 | | | mA |
| $T_{DR}$ | Data Retention | MIL-STD-883, Test Method 1008 | 100 | | | Years |
| $N_{END}$ | Endurance | MIL-STD-883, Test Method 1003 | 1,000,000 | | | Stores |

## DC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = +2.5 V to +6 V unless otherwise specified

### Power Supply

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Operating Voltage Range | | 2.5 | – | 6.0 | V |
| $I_{CC1}$ | Supply Current (Increment) | $V_{CC}$ = 6 V, f = 1 MHz, $I_W$ = 0 | – | – | 100 | µA |
| | | $V_{CC}$ = 6 V, f = 250 kHz, $I_W$ = 0 | – | – | 50 | µA |
| $I_{CC2}$ | Supply Current (Write) | Programming, $V_{CC}$ = 6 V | – | – | 1000 | µA |
| | | $V_{CC}$ = 3 V | – | – | 500 | µA |
| $I_{SB1}$[3] | Supply Current (Standby) | $\overline{CS}$ = $V_{CC}$ - 0.3 V<br>U/$\overline{D}$, $\overline{INC}$ = $V_{CC}$ - 0.3 V or GND | – | 0.01 | 1 | µA |

**Notes:**

(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

(2) This parameter is tested initially and after a design or process change that affects the parameter.

(3) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1 V to $V_{CC}$ + 1 V

(4) $I_W$ = source or sink

(5) These parameters are periodically sampled and are not 100% tested.

**Logic Inputs**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input Leakage Current | $V_{IN} = V_{CC}$ | – | – | 10 | µA |
| $I_{IL}$ | Input Leakage Current | $V_{IN} = 0$ V | – | – | -10 | µA |
| $V_{IH2}$ | CMOS High Level Input Voltage | 2.5 V ≤ $V_{CC}$ ≤ 6 V | $V_{CC}$ x 0.7 | – | $V_{CC}$ + 0.3 | V |
| $V_{IL2}$ | CMOS Low Level Input Voltage | | -0.3 | – | $V_{CC}$ x 0.2 | V |

**Potentiometer Characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{POT}$ | Potentiometer Resistance | -01 Device | | 1 | | kΩ |
| | | -10 Device | | 10 | | |
| | | -50 Device | | 50 | | |
| | | -00 Device | | 100 | | |
| | Pot. Resistance Tolerance | | | | ±20 | % |
| $V_{RH}$ | Voltage on $R_H$ pin | | 0 | | $V_{CC}$ | V |
| $V_{RL}$ | Voltage on $R_L$ pin | | 0 | | $V_{CC}$ | V |
| | Resolution | | | 1 | | % |
| INL | Integral Linearity Error | $I_W$ ≤ 2 µA | | 0.5 | 1 | LSB |
| DNL | Differential Linearity Error | $I_W$ ≤ 2 µA | | 0.25 | 0.5 | LSB |
| $R_{WI}$ | Wiper Resistance | $V_{CC}$ = 5 V, $I_W$ = 1 mA | | | 400 | Ω |
| | | $V_{CC}$ = 2.5 V, $I_W$ = 1 mA | | | 1000 | Ω |
| $I_W$ | Wiper Current | (1) | -4.4 | | 4.4 | mA |
| $TC_{RPOT}$ | TC of Pot Resistance | | | 300 | | ppm/ºC |
| $TC_{RATIO}$ | Ratiometric TC | | | | 20 | ppm/ºC |
| $V_N$ | Noise | 100 kHz / 1 kHz | | 8/24 | | nV/√Hz |
| $C_H/C_L/C_W$ | Potentiometer Capacitances | | | 8/8/25 | | pF |
| fc | Frequency Response | Passive Attenuator, 10 kΩ | | 1.7 | | MHz |

**Notes:**
(1) This parameter is not 100% tested.

### AC CONDITIONS OF TEST

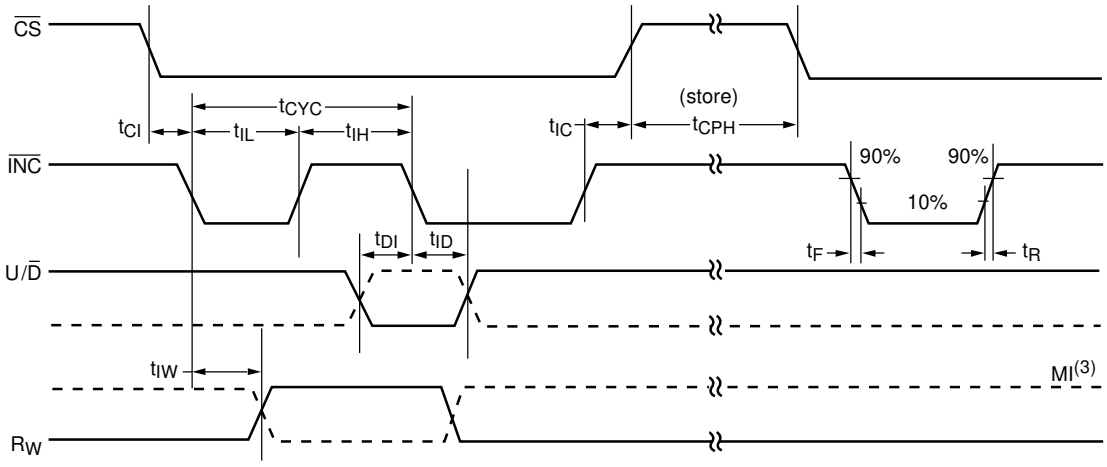
| | |
|---|---|
| $V_{CC}$ Range | 2.5 V ≤ $V_{CC}$ ≤ 6 V |
| Input Pulse Levels | 0.2$V_{CC}$ to 0.7$V_{CC}$ |
| Input Rise and Fall Times | 10 ns |
| Input Reference Levels | 0.5$V_{CC}$ |

### AC OPERATING CHARACTERISTICS

$V_{CC}$ = +2.5 V to +6.0 V, $V_H$ = $V_{CC}$, $V_L$ = 0 V, unless otherwise specified

| Symbol | Parameter | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|
| $t_{CI}$ | $\overline{CS}$ to $\overline{INC}$ Setup | 100 | – | – | ns |
| $t_{DI}$ | U/$\overline{D}$ to $\overline{INC}$ Setup | 50 | – | – | ns |
| $t_{ID}$ | U/$\overline{D}$ to $\overline{INC}$ Hold | 100 | – | – | ns |
| $t_{IL}$ | $\overline{INC}$ LOW Period | 250 | – | – | ns |
| $t_{IH}$ | $\overline{INC}$ HIGH Period | 250 | – | – | ns |
| $t_{IC}$ | $\overline{INC}$ Inactive to $\overline{CS}$ Inactive | 1 | – | – | µs |
| $t_{CPH}$ | $\overline{CS}$ Deselect Time (NO STORE) | 100 | – | – | ns |
| $t_{CPH}$ | $\overline{CS}$ Deselect Time (STORE) | 10 | – | – | ms |
| $t_{IW}$ | $\overline{INC}$ to $V_{OUT}$ Change | – | 1 | 5 | µs |
| $t_{CYC}$ | $\overline{INC}$ Cycle Time | 1 | – | – | µs |
| $t_R$, $t_F$[2] | $\overline{INC}$ Input Rise and Fall Time | – | – | 500 | µs |
| $t_{PU}$[2] | Power-up to Wiper Stable | – | – | 1 | ms |
| $t_{WR}$ | Store Cycle | – | 5 | 10 | ms |

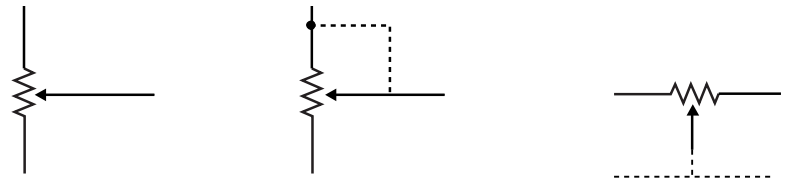
## A.C. TIMING




**Notes:**
(1) Typical values are for $T_A$ = 25ºC and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.
(3) MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

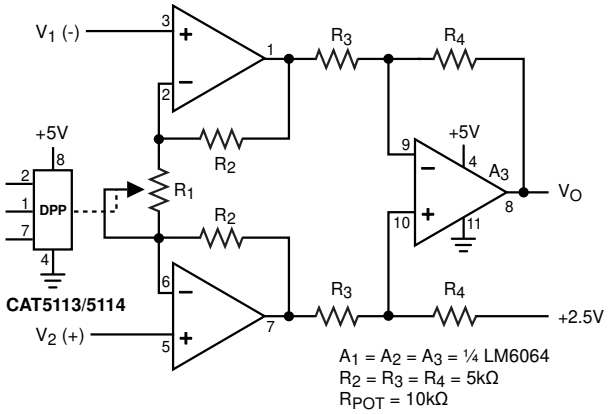
# APPLICATIONS INFORMATION

## Potentiometer Configuration

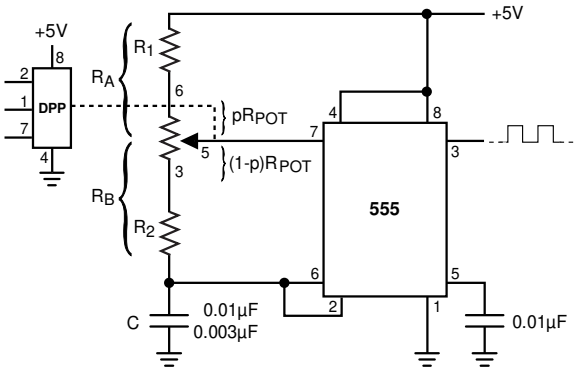


**(a) resistive divider** **(b) variable resistance** **(c) two-port**

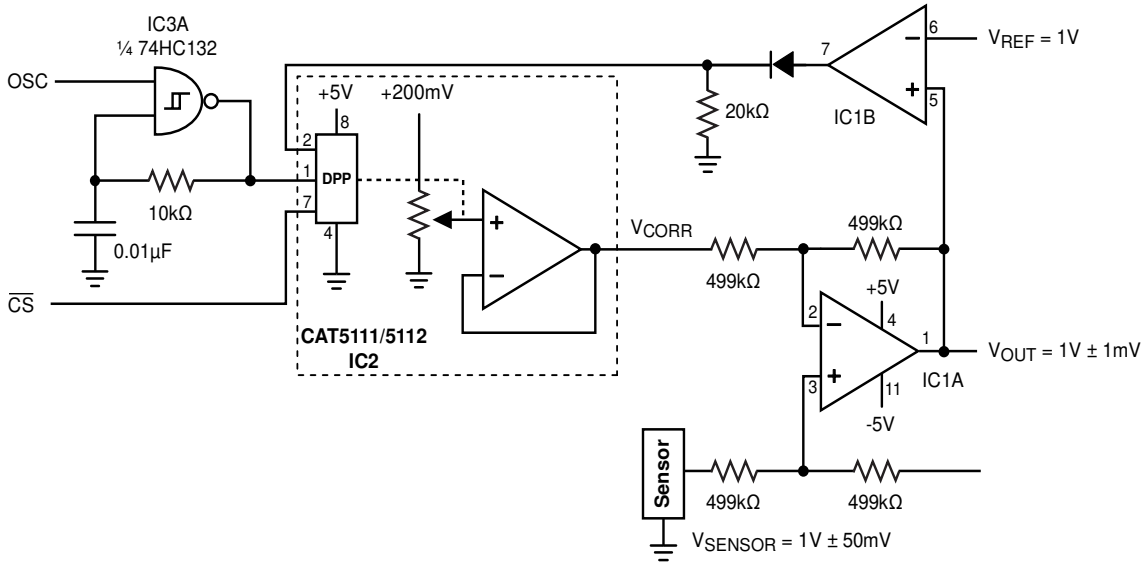
## Applications



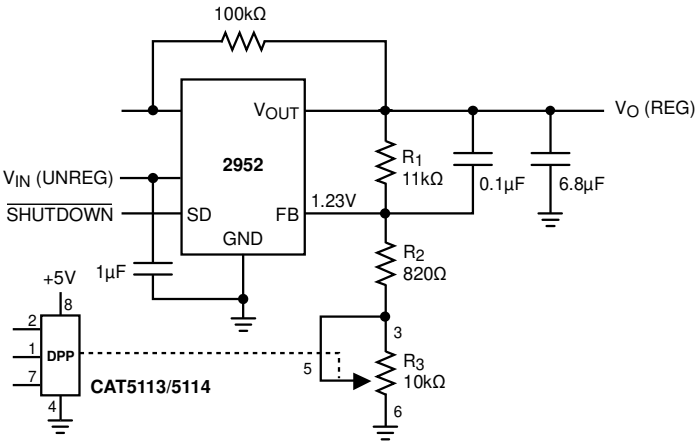

**Programmable Instrumentation Amplifier**



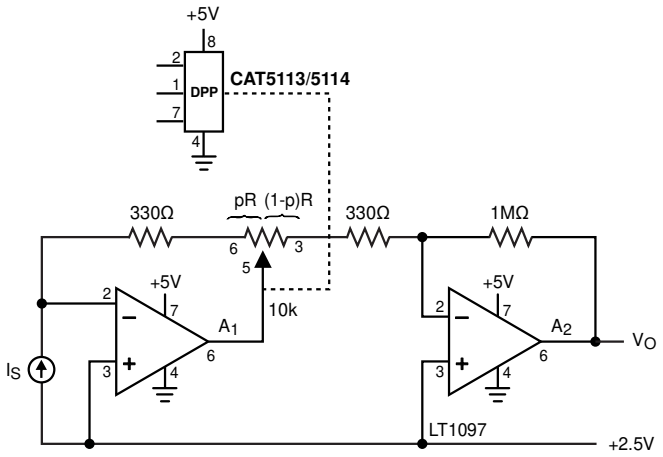

**Programmable Sq. Wave Oscillator (555)**



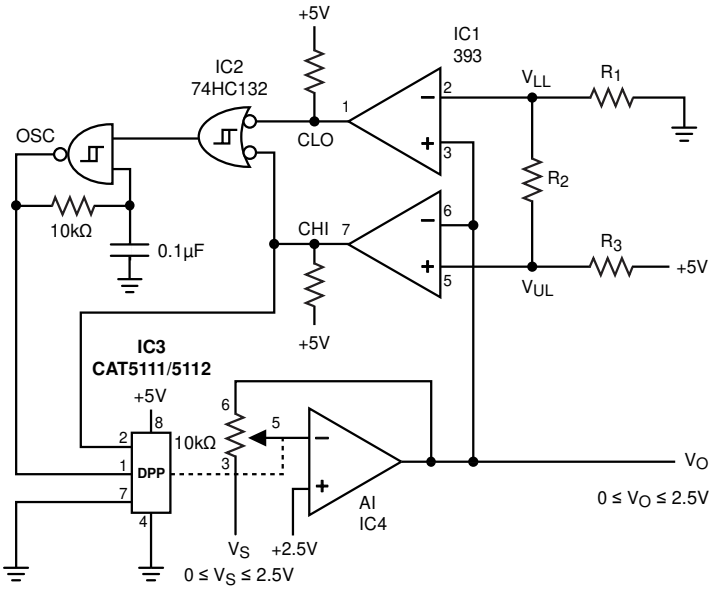

**Sensor Auto Referencing Circuit**



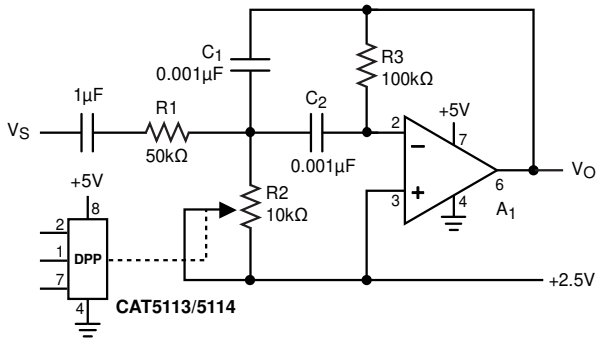

**Programmable Voltage Regulator**



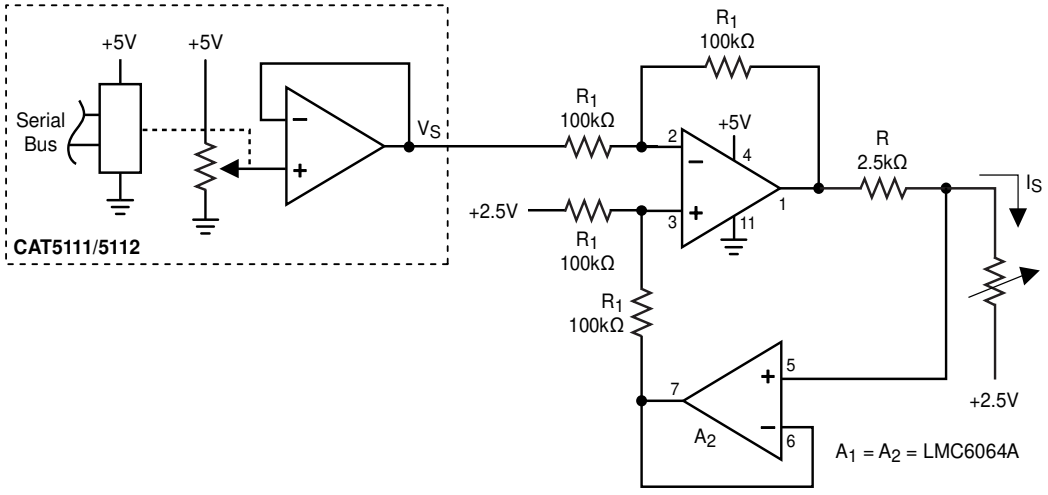

**Programmable I to V Convertor**




**Automatic Gain Control**



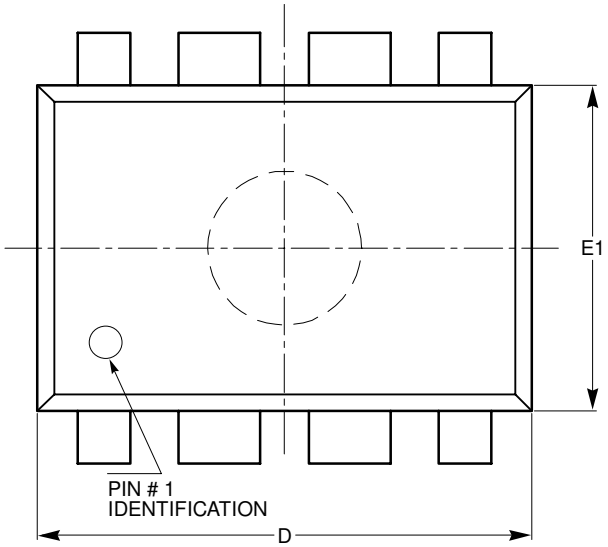

**Programmable Bandpass Filter**




**Programmable Current Source/Sink**

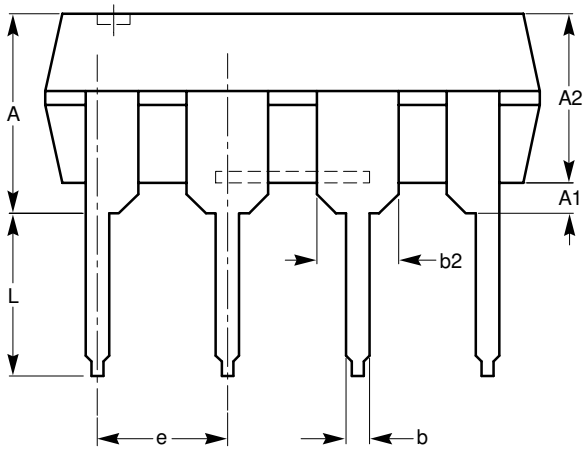
## PACKAGE OUTLINE DRAWINGS

### PDIP 8-Lead 300 mils (L)[1][2]

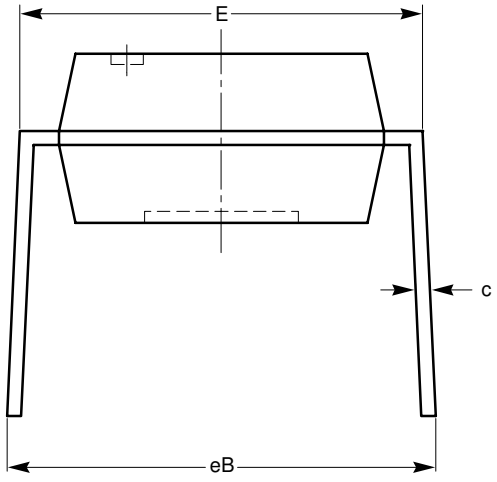



TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | | | 5.33 |
| A1 | 0.38 | | |
| A2 | 2.92 | 3.30 | 4.95 |
| b | 0.36 | 0.46 | 0.56 |
| b2 | 1.14 | 1.52 | 1.78 |
| c | 0.20 | 0.25 | 0.36 |
| D | 9.02 | 9.27 | 10.16 |
| E | 7.62 | 7.87 | 8.25 |
| e | | 2.54 BSC | |
| E1 | 6.10 | 6.35 | 7.11 |
| eB | 7.87 | | 10.92 |
| L | 2.92 | 3.30 | 3.80 |



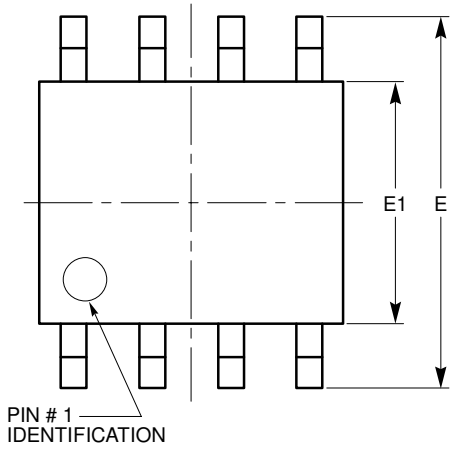

SIDE VIEW




END VIEW

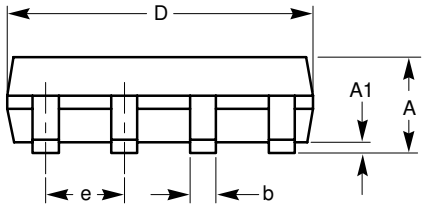
**Notes:**
(1) All dimensions are in millimeters.
(2) Complies with JEDEC Standard MS-001.

## SOIC 8-Lead 150 mils (V) [1][2]

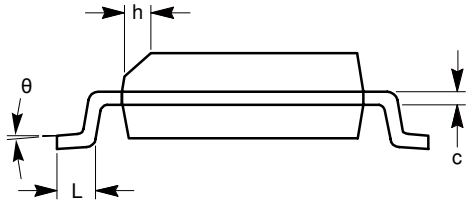



TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 1.35 | | 1.75 |
| A1 | 0.10 | | 0.25 |
| b | 0.33 | | 0.51 |
| c | 0.19 | | 0.25 |
| D | 4.80 | | 5.00 |
| E | 5.80 | | 6.20 |
| E1 | 3.80 | | 4.00 |
| e | | 1.27 BSC | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| θ | 0º | | 8º |



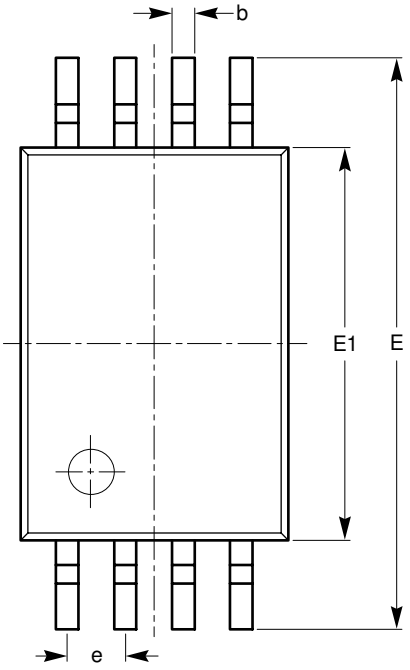

SIDE VIEW




END VIEW

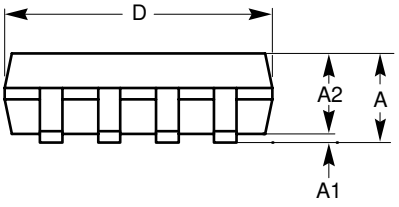
**Notes:**
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC Specification MS-012.

## TSSOP 8-Lead 4.4 mm (Y) [1][2]

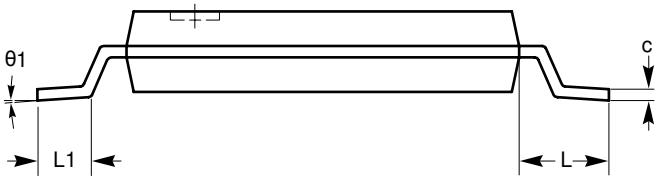



TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | | | 1.20 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.80 | 0.90 | 1.05 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 2.90 | 3.00 | 3.10 |
| E | 6.30 | 6.40 | 6.50 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | | 0.65 BSC | |
| L | | 1.00 REF | |
| L1 | 0.50 | 0.60 | 0.75 |
| θ1 | 0° | | 8° |



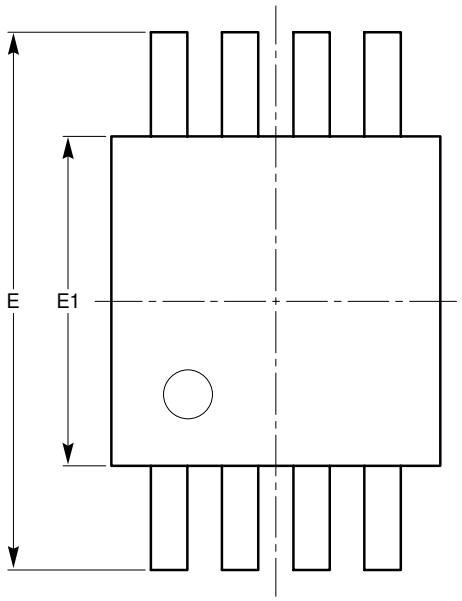

SIDE VIEW




END VIEW

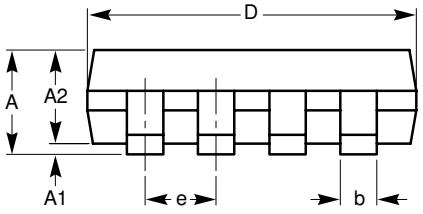
**Notes:**
(1) All dimensions are in millimeters.
(2) Complies with JEDEC Standard MO-153

## MSOP 8-Lead 3.0 x 3.0 mm (Z) [1][2]

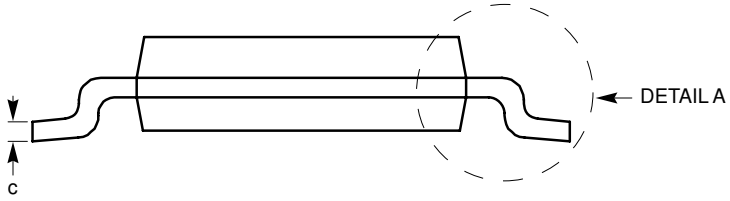



TOP VIEW

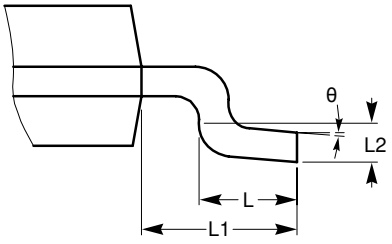
| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | | | 1.10 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | 0.75 | 0.85 | 0.95 |
| b | 0.22 | | 0.38 |
| c | 0.13 | | 0.23 |
| D | 2.90 | 3.00 | 3.10 |
| E | 4.80 | 4.90 | 5.00 |
| E1 | 2.90 | 3.00 | 3.10 |
| e | | 0.65 BSC | |
| L | 0.40 | 0.60 | 0.80 |
| L1 | | 0.95 REF | |
| L2 | | 0.25 BSC | |
| θ | 0º | | 6º |




SIDE VIEW



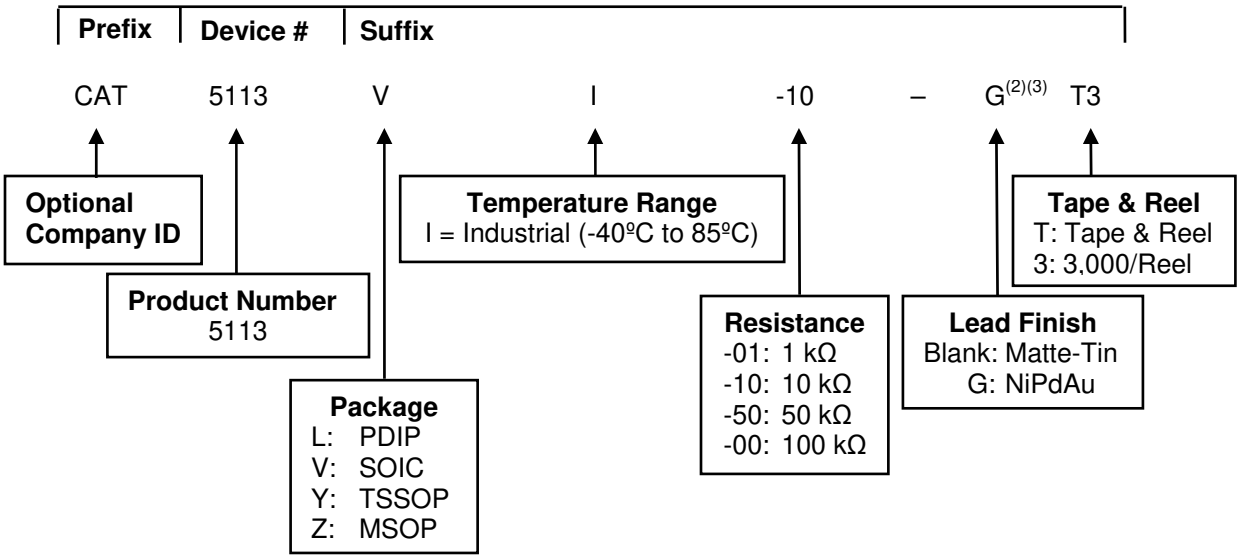

END VIEW




DETAIL A

**Notes:**
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC Specification MS-187.

## EXAMPLE OF ORDERING INFORMATION




**Notes:**

(1) All packages are RoHS-compliant (Lead-free, Halogen-free).
(2) The standard lead finish is NiPdAu, except MSOP package is Matte-Tin.
(3) Contact factory for Matte-Tin finish availability for PDIP, SOIC and TSSOP packages.
(4) This device used in the above example is a CAT5113VI-10-GT3 (SOIC, Industrial Temperature, 10 kΩ, NiPdAu, Tape & Reel, 3,000/Reel).

## ORDERING INFORMATION

| Orderable Part Number | Resistance (kΩ) | Package-Pins | Lead Finish |
|---|---|---|---|
| CAT5113LI-01-G | 1 | PDIP-8 | NiPdAu |
| CAT5113LI-10-G | 10 | | |
| CAT5113LI-50-G | 50 | | |
| CAT5113LI-00-G | 100 | | |
| CAT5113VI-01-GT3 | 1 | SOIC-8 | NiPdAu |
| CAT5113VI-10-GT3 | 10 | | |
| CAT5113VI-50-GT3 | 50 | | |
| CAT5113VI-00-GT3 | 100 | | |
| CAT5113YI-01-GT3 | 1 | TSSOP-8 | NiPdAu |
| CAT5113YI-10-GT3 | 10 | | |
| CAT5113YI-50-GT3 | 50 | | |
| CAT5113YI-00-GT3 | 100 | | |
| CAT5113ZI-01-T3 | 1 | MSOP-8 | Matte-Tin |
| CAT5113ZI-10-T3 | 10 | | |
| CAT5113ZI-50-T3 | 50 | | |
| CAT5113ZI-00-T3 | 100 | | |

## REVISION HISTORY

| Date | Rev. | Description |
|---|---|---|
| 09-Oct-03 | M | Revised Features<br>Revised DC Electrical Characteristics |
| 10-Mar-04 | N | Updated Potentiometer Parameters |
| 29-Mar-04 | O | Changed Green Package marking for SOIC from W to V |
| 02-Apr-04 | P | Add 1kΩ version to data sheet |
| 08-Apr-04 | Q | Eliminated data sheet designation<br>Updated Tape and Reel specs in Ordering Information |
| 25-Jan-05 | R | Updated Potentiometer Parameters |
| 22-Apr-06 | S | Updated Example of Ordering Information |
| 01-Jun-07 | T | Added Package Outline<br>Added MD- in front of Document No. |
| 15-Feb-08 | U | Update Logic Inputs table<br>Update Application Information (Sensor Auto Referencing Circuit and Programmable Current Source/Sink)<br>Update Package Outline Drawings |
| 27-Mar-08 | V | Update Example of Ordering Information<br>Delete MSOP in NiPdAu plated finish<br>Add Top Mark Codes link |
| 20-Nov-08 | X | Change logo and fine print to ON Semiconductor |
| 10-Jul-09 | Y | Update Ordering Information table |



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